



Article Real-Time Control of a Battery Energy Storage System Using a Reconfigurable Synchrophasor-Based Control System [†]

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Abstract: Synchrophasor-driven smart grid applications aiming to orchestrate a diverse set of Distributed Energy Resources (DERs) require extensive infrastructure including substantial instrumentation hardware, communication network extensions and controller installations for coordinated operation. This can make the overall installation expensive. Additionally, due to the computational complexity and data-intensive nature of the PDC functionality, most of the existing PDC implementations are on a purely software level, making them unsuitable for the real-time applications. To address this, the current paper proposes an alternate architecture for the real-time synchrophasorbased control of DER applications (e.g., microgrids) incorporating a centralized synchronization hardware designed to replace aggregation Phasor Data Concentrators (PDCs) and supplementary control algorithms into a singular reconfigurable hardware. This particular hardware is termed a Synchrophasor Synchronization Gateway and Controller (SSGC). The robustness of the proposed architecture is tested by using real-time (RT) Controller Hardware-In-the-Loop (CHIL) simulation-based experiments by manipulating the communication network that connects the SSGC with multiple Phasor Measurement Unit (PMU) streams broadcasting data through the IEEE C37.118.2 protocol in real time. These PMU streams were generated by using a real-time microgrid model running on a Typhoon HIL 604 simulator. To manipulate the communication interface between the proposed SSGC hardware and the PMU streams, a configurable Wide Area Network (WAN) emulator and communication network impairment appliance deployed in the Candela Technologies CT910 external hardware was utilized. The real-time control system was expanded by incorporating a low-pass filter to eliminate the potential overswitching of a Battery Energy Storage System (BESS). The proposed architecture demonstrated a reliable performance under ideal to moderately tampered communication networks. However, under a significantly corrupted network, the performance of this architecture is acutely affected.

Keywords: synchrophasor; Typhoon HIL 604; IEEE C37.118; DER; communication protocols; PMU; PMU-based control; CHIL; HIL; BESS

1. Introduction

1.1. Motivation

In modern interconnected power systems deploying synchrophasor technology, Phasor Data Concentrators (PDCs) are expected to receive, parse, align, store and publish the measurement data received from Phasor Measurement Units (PMUs). As networked devices, PDCs should be compliant with synchronized data transmission standards, i.e., IEEE C37.118.2 [1] While maintaining this compatibility, the existing PDC hardware is inadequate to comply with hard **real-time** control requirements. Currently, most state-of-the-art *real-time compliant* PDC implementations are developed entirely at the software level.



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Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). On the other end, existing industrial PDCs [2–4] are **not** real-time compliant as they are implemented in nondeterministic operating systems (e.g., Windows 10/11 and similar). This gap in engineering development has been studied and reported by the authors of [5–7].

As illustrated in Figure 1, this makes the application of PDCs in the real-time networked control of power systems a challenging problem, with the major drawback of latency build-up if the current approach for real-time synchrophasor control is adopted. In [8], a hardware platform for wide-area control system (WACS) applications that can only function upon a single incoming PMU stream was proposed. To the best of the authors' knowledge, currently, there is no real-time compliant real-time PDC hardware architecture that can operate on multiple PMU streams. This becomes a bottleneck in implementing synchrophasor-driven real-time control systems for microgrid applications that require measurements from diverse Distributed Energy Resources (DERs). To bridge this gap, as illustrated in Figure 2, this paper proposes an alternative real-time control architecture which replaces aggregator PDCs and secondary control functionalities into a singular reconfigurable hardware and demonstrates a microgrid control system featuring the proposed hardware.



Figure 1. Typical infrastructure for real-time control using networked PMUs and PDCs.



Figure 2. Proposed approach for real-time DER control with networked PMUs and SSGC.

1.2. Related Works

Synchrophasor-based networked control architectures for power systems is an emerging field of research. Due to the latency build-up within the network, the computational limitations of various edge devices, and the strict real-time compliance requirement required for designing a control system, the deployment of a fully functional real-time synchrophasorbased networked control architecture becomes extremely challenging. These challenges have been summarized in [9].

Most of the existing research in this domain proposes and utilizes very specific edge devices and software tools to implement such a control system, which is summarized in Table 1. The authors of [10] developed custom PMU hardware (MDPMU) to deploy their proposed fast-load-control system based on synchrophasor measurements retrieved from those custom PMUs. Similar custom PMUs (both on hardware and software levels) were developed by the authors of [11–13] while deploying their custom FNET/GridEye wide-area synchrophasor network. However, these implementations focused on the monitoring and event-detection applications only, leaving open questions related to real-time control. Meanwhile, industrial research laboratories (e.g., SEL) have published hardware developments for PMU-based control applications in [14]. However, these developments did not explore the utilization of concurrent PMU streams coming from different locations and focused on local control application development from local PMU streams. Thus, this development was not tested for robustness under corrupted network conditions, which take into account incoming measurement data from remote PMUs.

Table 1. Summary of existing research related to PMU/PDC-based real-time control.

Reference	Hardware/ Software	RT Compliant	Suitable for control	Available at Production Scale	Comments
[10]	Hardware	Yes	Yes	No	Cannot utilize existing PMUs in the network
[11–13]	Both	Yes	No	Yes	Control applications not tested
[14]	Hardware	Yes	No	Yes	Tested only for local control
[15,16]	Software	No	Yes	No	No major hardware development
[17]	Software	Yes	No	No	Proposed a PDC placement scheme for control

The decentralized nature of DERs coupled with the hierarchical character of the microgrid control system (reported in [18–21]) makes it possible to break up the control system into different networked hardware according to the transient requirements of the control action. Based on the survey presented in [21], it can be hypothesized that the *secondary* and *tertiary* control actions for microgrids can be put into networked devices because these control actions are relatively slow in operation. The current paper only focuses on implementing *secondary* control actions, more specifically the control of active and reactive power flow. The research reported in [22,23] established the theoretical background for controlling BESS in real time.

The authors of [24] reported the architecture for the Synchrophasor Synchronization Gateway (SSG) and introduced the hardware and software associated with the implementation. On the software level, the SSG uses the C-based *Khorjin* library reported in [25] to parse multiple and concurrent PMU data streams. The SSG's Graphical User Interface (GUI) was designed by using LabVIEW; it can be configured to accommodate additional incoming PMU/PDC streams and to apply modifications in communication-network specifications. Because some of the functionalities provided by the proposed hardware are similar to the functionalities offered by a PDC, it is important to take note of the existing standardization efforts in the domains of PDC hardware implementation. The authors of [6] summarized the standard functional blocks and communication interfaces associated with the PDC architecture. A similar study was reported in [26] that also explored the communication protocol between the PMUs and PDCs.

Unlike a conventional PDC, the SSGC enables real-time control functions in addition to the aforementioned PDC functions, and some of the control functions that can be implemented by using synchrophasor-based control were reviewed as part of the literature survey. In the domain of control system design for microgrids, the authors of [21] and [27] surveyed and classified the existing control strategies into three different classes depending on the priorities, time scales and required speed of the various control actions. The primary control class consists of the fastest control actions including voltage and current control algorithms for the individual DERs. The secondary control class evaluates the power flows to and from the different existing DERs and helps the microgrid navigate

between the islanded and grid-tied modes. The secondary control class tackles slower dynamic responses (e.g., power flow) compared to the primary control class. Finally, the tertiary control class consists of supplementary control algorithms sitting on top of both primary and secondary classes of control and enables the microgrid to operate in an economically optimized fashion. The research reported in [28] demonstrated significant efforts of standardization across these three classes of control systems in microgrids. The authors of [29] explored the utilization of synchrophasor data to monitor microgrids and to increase the reliability of measurement data. To this end, this research proposed an Advanced Phasor Data Concentrator (APDC) hardware that is capable of operating under a tampered network and estimating missing data points in the synchrophasor streams. However, this hardware was not time synchronized, and the reported experiments were performed by a programmable voltage source, lacking the testing rigor that can be brought by using Hardware-In-the-Loop experimental testing techniques [30]. The present manuscript addresses both gaps, i.e., time synchronization, and it exploits RT Controller Hardware-In-the-Loop real-time simulations with microgrid models. The experiments reported in [31] illustrated a synchrophasor-based control architecture for microgrids, where the synchrophasor data are used to formulate reduced-order dynamic models for the DERs within the microgrid, and used those models to seamlessly navigate the microgrid between the islanded mode and the grid-tied mode. Meanwhile, Ref. [32] demonstrated the utilization of adaptive network-management tools within the PDC to compensate the network delays between the PDC and the individual PMUs.

In [24], the authors proposed a framework where multiple concurrent instances of the same dynamically linked library (DLL) were used to parse multiple PMU streams in real time. This procedure includes both deciphering the measurement data and extracting the synchrophasor configuration information. The communication link requires bidirectional capabilities as the PMUs send header information, measurement data and configuration information; they also receive a command message to enable or disable the data transmission. The research presented in [24,33] utilizes multiple instances of this *Khorjin* thread to facilitate the real-time reception and parsing of synchrophasor data streamed from multiple sources. Finally, it is important to note that while the current research utilized the same Khorjin-based SSG architecture reported in [24,33], the major contribution of the current paper lies in the extension of the SSG architecture into the domains of secondary control actions and their validation by using real-time CHIL experiments by using a microgrid model with DERs, where the secondary controller drives a Battery Energy Storage System (BESS).

1.3. Contributions

The current paper proposes the following contributions:

- The capabilities of the *Khorjin* library are extended to develop a Synchrophasor Synchronization Gateway and Control (SSGC) architecture, consisting of a synchronization layer and a control layer.
- A new PMU-based approach for control of the DERs is introduced and demonstrated by using real-time Controller Hardware-In-the-Loop (CHIL) including a microgrid model. This approach exploits the proposed SSGC architecture.
- The performance of the proposed SSGC architecture is analyzed under varying communication network conditions (including randomized configurations) with multiple PMU streams.
- The proposed control system is further enhanced by applying Low Pass Filters (LPFs) in the real-time controller's control error signal to mitigate the overswitching of the primary controllers inside a Battery Energy Storage System (BESS).
- The real-time performance of the SSGC is demonstrated under the presence of faster transients in the system when the control signal is passed through the enhanced controller (with LPFs).

• The SSGC architecture was validated by deploying a second type of secondary controller. The controller utilizes the phase-angle difference between two PMU locations to control the active power output.

1.4. Paper Organization

The remainder of this paper is organized as follows. Section 2 gives an overview of the real-time controller's architecture and the experimental setup developed to validate the proposed approach in this paper. Section 3 presents the results of the performance of the SSGC under both ideal and impaired communication network conditions and the enhancement of the Battery Energy Storage System (BESS) response by enhancing the control function through LPFs, limiting unnecessary BESS switching. Finally, Section 4 outlines future work and Section 5 presents this paper's major conclusions.

2. Architecture and Experimental Setup

2.1. Controller Architecture

The authors of [25] presented the *Khorjin* library, which receives, extracts and parses a C37.118.2 data stream before feeding the information to subscriber applications. The authors of [24,33] demonstrated the data unwrapping and time synchronization functionalities on the real-time embedded system (host), utilizing multiple instances of *Khorjin* extracting data from multiple incoming concurrent PMU streams in parallel.

In this paper, the 'virtual instrument code' running on the host side (in an RT OS) is extended and improved to incorporate crucial secondary control functionalities targeted to control DERs in a microgrid, whose one-line diagram and simplified view is shown in Figure 3. The real-time control system utilizes PI controllers that calculate their set point and process variables by unwrapping the current and voltage phasors received from the concurrent *Khorjin* instances. A simplified view of the system is demonstrated in Figure 4, which identifies both the electrical connections and communication interfaces of the setup. The detailed experimental setup is illustrated in Figure 5.

A *Khorjin* thread requires bidirectional data transmission capabilities for the communication link. After securing the TCP/IP connection, the SSG sends a 'turn off transmission' command and a 'send CFG-2' command. The PMU responds by sending the CFG-2 frame. At this point, the SSG has received all the required information from this frame to initiate the data transmission. Hence, the SSG now requests synchrophasor measurement data, and the PMU begins data transmission. This exact protocol is implemented in all the concurrent *Khorjin* instances. This process is graphically illustrated in Figure 6.



Figure 3. Simplified real-time microgrid model implemented by using Typhoon HIL 604.



Figure 4. Simplified block diagram of the experimental setup.



Figure 5. Detailed architecture of the experimental setup demonstrating the software and hard-ware components.



Figure 6. PMU to SSG/SSGC data transmission protocol by utilizing Khorjin instance.

As can be observed in Figures 5 and 7, the main goal of the real-time controller is to maintain the power at the Point of Common Connection (PCC) constant from the point of view of the utility, meaning that the microgrid self-balances by taking advantage of measurements at the PCC and other locations (e.g., at the BEES terminals). Because the goal of the controller is to redispatch the battery to meet load/generation changes within the microgrid, it is important to mitigate the BESS response in specific time scales. To achieve this goal, the real-time control system was enhanced by incorporating LPFs, as shown in Figure 8, which would prevent the controller from responding to possible high-frequency transients on the load side (e.g., switching transients).



Figure 7. SSGC's utilization within hierarchical control system for microgrid.





Figure 8. Microgrid controller implementation utilized in the experimental setup.

The current work demonstrates a scenario where the proposed SSGC architecture is configured to regulate the power output from a Battery Energy Storage System (BESS)based DER. As shown in Figure 8, the PI controller coded inside the SSGC hardware (situated at the remote location) determines the set point to be utilized at the local (primary) controller inside the BESS. The individual parameters for the PI controller were based on the specifications provided in the model illustrated in [34]. The PI controller was followed by a saturation block (with the upper and lower limits set at 1 and -1, respectively) to ensure stability. The value of K_p and K_i were taken from the Typhoon specifications directly (for this particular application, $K_p = 0.5$ and $K_i = 3.0$). This control algorithm computes P and Q in real time from the voltage and current phasors it receives from the multiple incoming PMU streams. The controller uses P and Q as the control variable. It is also possible to utilize the voltage magnitude and phase-angle differences ($\Delta \delta$) as the control input variables [35–38]. The controller output is fed back to the real-time simulator's analog input channels and used as a control input for the *primary controller* of the Li-Ion BESS, as shown in Figure 7. The proposed control architecture can take advantage of the hierarchical structure of the control system for microgrids, secondary control in particular, as summarized in [21].

It must be noted that, as shown in Figures 3 and 5, the microgrid RT simulation model comprises a diesel generator, a PV system and an external grid alongside the BESS. All these energy resources work in synchronism to supply a configurable load. These models

were based on the existing components available in the Typhoon HIL's model library [34] and [39].

2.2. Experimental Setup

This paper reports a reconfigurable SSGC hardware that can suitably incorporate secondary and tertiary control functionalities. As proof of concept, the authors aim to demonstrate its functionalities through a real-time secondary controller to regulate the power output of the BESS implemented on the SSGC in this work. This is illustrated in the block diagram of Figure 8.

2.2.1. Scope of the Experiments Supported by the Experimental Setup

As shown in Figure 8, the proposed secondary control action utilizes a set point, which is computed in real time from the two parameters P_{Lm} , which represents the measurement from the load side, and P_{bat} , which represents the BESS output power. The experiments in this work will assume that the P_{PV} (active power output from the PV system), P_{Uti} (active power dispatch from the utility) and P_{DSG} (active power output from the diesel generator) are constant. Under this condition, the parameter P_{ref} (reference power) will be a product of the changes in the total load consumption P_{load} only. For this part of the experiment, the two PMUs were placed near the load and near the BESS as the current measurements at these locations were expected to experience changes along with changes in the load and battery dispatch. As an extension, a further experiment was performed by taking the phase-angle difference ($\delta_{PCC} - \delta_{Load}$) as the control variable to regulate the active power output from the BESS instead of using the active powers directly. For this part of the experiment, the phase angles were measured at the point of common coupling (PCC) and the load. Thus, the PMUs were placed accordingly. The reprogrammable and reconfigurable nature of the proposed SSGC hardware can be exploited to adapt the hardware to deploy different control schemes and control of different types of DERs. However, those experiments are considered to be beyond the scope of the current paper. For demonstration, only real-time synchrophasor-based P-Q control of the BESS is presented in this paper. Hence, this paper primarily focuses on the implementation of the SSGC architecture and its validation in the context of simple control-system development targeted for DERs. We also demonstrate how the control performance can be improved by implementing a Low Pass Filter (LPF) $(LPF(s) = \frac{1}{1+\tau S})$, where $\tau = \frac{1}{\omega_c}$ to make the BESS operate safely under a condition where switching transients are present in the load.

2.2.2. Real-Time Communications

It has been discussed that the SSGC requires real-time synchrophasor data (i.e., following the IEEE C37.118.2 std.) to be streamed at its input. Modern RT simulators have the capability to stream synchrophasor data directly from the RT model being simulated, without requiring external PMU hardware. However, the present work was completed by using *Typhoon HIL control center's* 2020.4 release, where the IEEE C37.118 library was primitive and unstable (as discovered through experimentation) when connected to external hardware such as a PDC or SSGC (note that the 2022.4 and 2023.1 releases of the *Typhoon HIL control center* toolkit have stable and dedicated library components for streaming C37.118 data, and the authors of this paper chose not to adjust the hardware configuration and keep the PMUs as external hardware to facilitate impairment). This was chosen to facilitate tampering between the communications network between the PMUs and the SSGC hardware. With the introduction of external PMU hardware based on [40,41], it is simple to pick and choose individual PMUs and corrupt the communication network between any single PMU and the SSGC hardware.

2.3. Hardware Integration

The aforementioned external PMUs (the hardware used is that reported in [42] and extended in [43]) were connected to the low-voltage analog outputs of the real-time simu-

lator. It is crucial to note that these PMU designs feature both current and voltage inputs to function as PMUs whereas Typhoon HIL 604 hardware **only** provides analog voltage outputs. Thus, an external *burden circuit* was introduced in the experimental setup to perform the voltage-to-current conversion, as demonstrated in Figure 9c. The connection between Typhoon HIL 604 (the hosting microgrid model) and the PMUs (streaming synchrophasor data to SSGC) is shown in Figure 9a. Figure 9b demonstrates how the PMUs receive GPS signals to obtain precision timing, and Figure 9d shows the SSGC deployed in a remote location, communicating to the rest of the experimental setup through a standard Ethernet-based communication network.



Figure 9. Hardware arrangement for RT-HIL-testing the SSGC hardware: (**a**) connection between the microgrid and the PMUs, (**b**) PMUs receiving timing information, (**c**) conversion of RT low-voltage signals into current signals and (**d**) SSGC connected remotely to the microgrid RT model.

SSGC Configuration and Integration in the Experimental Setup

Figure 10 shows how the LabVIEW GUI interacts with the physical inputs and outputs of the Typhoon HIL 604 and how the analog signal levels are scaled to obtain the measurements of actual voltages and currents. This technique enables the SSGC operation without any high external amplifiers that are typically required for HIL experiments [30], such as [44], making the experimental environment safer.

IP Addres	Connection Data					MU 2 data processing	9081
ID C 1 Port 2 471	IP Address (PMU / PDC) 192.168.20.218 ID CODE 1 Port Number					MU 1 data processing	c RIO S
ST MUs Da	STOP Shut Dow	'n			rement values	Page 1 Page 2 10 Page 2 11 Page 2 12 Page 2 13 Page 2 14 Page 2 15 Page 2 16 Page 2 17 Page 2 18 Page 2 19 Page 2 10 Page 2 10 Page 2 10 Page 2	Secondar
Good MU Tr No	Philos Data stream Data Error Status Good Measurment Data PMU Triggered Trigger R	(No Errors) eason	PMU Sync Status Dat	Processed PMU Time Quality TIME ERROR < 100 ns Frequency ROCOF	sGC calculating measu	рани и праводани	V Control System
Phasors Types) Voltag	Phasors Phasors	Phasors	Phasors	Phasors (Apple Decreas)	SSGC re	Typhoon HIL break	kout board
Voltac	Voltage	1	2.77509	109.827	trie		
Currer	Voltage	2	2.77529	-10.1703) ji		
Currer	Voltage	3	2.7746	-130.17	E C		
Currer	Current	4	0.0650501	29.2576	ž		And
	Current	5	0.0634604	149.651	da		200
	Const	1	0.063043	-00.0542	- 2		

Figure 10. Details of the control system implemented inside the SSGC.

The communication network between the SSGC hardware and the PMUs was intentionally impaired during experimentation in order to test the robustness of the proposed control architecture. To perform these network impairments, the external *Wide-Area Network emulator and impairment appliance hardware CandelaTech CT910* [45] was connected inside the network, which would tamper the communication link between PMUs and the SSGC. Using CT910, it is possible to introduce custom delays, data drops, jitters and bandwidth limitations within the network. The values of these parameters can be reprogrammed every second, and this procedure can be automated.

3. Results

3.1. SSGC Performance under Ideal Network Conditions

In this experiment, the total load is increased in a step by turning on the *configurable load*, as shown in Figure 3. Initially, a fixed load of 825 kW was supplied by the PV unit (125 kW), diesel generator (500 kW) and the utility (100 kW). This makes the initial dispatch for the BESS inverter to be fixed at 100 kW. With the system running in this "steady state", a step increase of 300 kW in load was triggered externally.

Under this scenario, the control system must respond to this change in load. Hence, the BESS inverter and its dispatch increases from 100 kW to 400 kW. It is important to note that the portion of the controller (in Figure 8) within the dashed red box is implemented within the SSGC hardware. This portion is capable of utilizing synchrophasor measurement data obtained from the PMUs placed at the load and at the BESS. The PMU data are utilized to compute the active and reactive powers, which are then used to calculate a new set point (by using the PI controller block G_{PI}) to operate the BESS. This set point is then utilized by the internal control algorithm (implemented locally inside the BESS) to control the individual current and voltage output of the inverter inside the BESS. This portion of the control system was implemented locally within the BESS model of the real-time simulator because it generates high-frequency switching sequences for the individual semiconductor switches in the inverters that are modeled within the simulator.

Figure 11a shows the 300 kW manual load injection in the system. The SSGC incorporates a PI controller onboard. The output of this PI controller modulates the set point for the local BESS controller to operate, as shown in Figure 11b. This measurement is taken from the SSGC side. Meanwhile, in Figure 11c, the BESS power output response is shown. It can be observed from this figure that the power output of the battery increases from

100 kW to 400 kW to cover for the step increase in the load. Figure 11a–c demonstrate the SSGC's performance under ideal conditions of the communication network while there are no external communication disturbances.



Figure 11. Control system performance for the BESS under ideal network conditions: (**a**) 300 kW load injection by switching the interruptible load, (**b**) response at the output of the PI controller inside SSGC and (**c**) active power output from the Battery Energy Storage System (BESS).

3.2. SSGC Performance under Nonideal Communication Network Conditions

Even though the SSGC hardware can be configured to control different DERs and employ sophisticated control algorithms, such demonstrations are considered to be beyond the scope of the current paper. For experimentation purposes, only the real-time synchrophasor-based control of the BESS is presented in this paper. Hence, the primary focus of this paper is the implementation of the SSGC architecture and its validation in the context of the P-Q control of the BESS-based DER.

Because this controller architecture relies on real-time synchrophasor communications, it is important to assess the performance of the proposed architecture under nonideal communication network conditions. Therefore, to test the robustness of the SSGC architecture, the communication network between the SSGC hardware and the PMUs was tampered with, as shown in Figure 12. As mentioned earlier, to perform experiments impairing the communications, an additional external hardware *CandelaTech CT910* [45] was connected between the SSGC and the rest of the communication network system. This hardware enables the user to introduce custom delays and data drops within the network through a GUI or command line and is used for the experiments in the sequel.



Figure 12. Block diagram of a system comprising SSGC and *N* PMUs; the network between the SSGC and the *k*th PMU is impaired, while all the hardware receive timing information from the same time base.

3.2.1. Network Tampering by Introducing Fixed Delay

In this particular experiment, artificial delays were introduced in between PMU_1 and the SSG prototype. To this end, a network-traffic generator within the CT910 was reconfigured to introduce artificial delays and thereby tamper with the network between the two ports where the PMU_1 and SSGC prototype were connected.

Figure 12 shows a representative connection where the CT910 device is utilized to tamper with the communication link between PMU_1 and the SSGC. The delays are introduced by CT910 (CT910 uses the *LanForge 5.4.6* software library, which provides crucial command-line utilities and a stable GUI to interact with the communication link in real time). The delay between the time when a synchrophasor packet is generated and when that particular packet is received at the SSGC end can be computed by sharing the respective time stamps. This procedure is explained in detail by the authors of [24].

As a simple representative experiment, the network was impaired by injecting an additional 100 ms delay, and the network delay was computed in real time by time-stamp sharing. This network delay is plotted in Figure 13, which shows a window of 10 s, during which the communication link was tampered with an additional 100 ms delay.



Figure 13. Measured delay at the SSGC due to a 100 ms delay injection from the CT910.

3.2.2. Network Tampering by Introducing Varying Delay

In this experiment, the communication link between the PMU and the SSGC is subjected to a network tampering that would randomize the injected delay every second. The hardware restricts the frequency of the network reconfiguration and dictates that, at most, the network can be reconfigured **once every second**. To achieve this, a custom script was executed on the CT910 hardware that would reconfigure its network interface with a random amount of delay every second. A pregenerated data file contained the amount of the injected delay in milliseconds and was used by the script to reconfigure the hardware with varying amounts of delay every second. The overall execution is shown in the flowchart of Figure 14a.

By following the same methodology to compute the network delay as described in Section 3.2.1, the network delay of this experiment is computed in real time. These results are shown in Figure 14b. It can be seen that the network reconfigures itself with a new value of the injected delay every second. The data file containing the raw values of the *network delays* was generated from a *random variable* following a **uniform distribution** between 0 and 200 ms.

Additionally, for the second part of this experiment, *random* delays were also generated to compute the network delay in real time by using a *random variable* following a **normal distribution** with a fixed mean and standard deviation (all the negative values generated were discarded because network delay cannot be negative). The experiment is carried out for 10 min (with the network reconfiguring the delay every 1 s) and repeated 10 times. If the network sustains itself (i.e., the controller keeps operating after 10 min of real-time simulation), the experiment run is termed as *successful*.





Hardware

Data file containing

constrained

Index++

Figure 14. Randomized delay injection: (**a**) algorithm for random delay injection, (**b**) real-time delay measurement after randomized delay injection.

This batch of trials (10 runs, each for a duration of 10 min) was performed with different values of the mean and standard deviation of the injected delay, and whether or not the 10 individual runs were *successful* is summarized in Table 2. The mean delay was varied from 50 ms to 750 ms, and the standard deviation was varied from 5 ms to 200 ms. It can be seen that the performance progressively deteriorates at higher values of the mean delay. It can also be seen that when the mean delay is 500 ms, a small increase in the standard deviation leads to a significant number of *unsuccessful* trials. It is interesting to note that the *unsuccessful* runs failed because the First-In First-Out (FIFO) instances, which transmit data from the PMUs to the SSGC, gradually filled up as the PMUs keep streaming data into a slow network. This shows that in real-time applications under nonideal communication interfaces, the adequate sizing of elastic storage elements in the embedded systems is crucial for the control architecture to function.

Fable 2. SSGC	performance u	under v	varying rar	ndom	network	delays.

σ (ms) μ (ms)	5	10	25	50	100	200
50	10/10	10/10	10/10	10/10	10/10	10/10
100	10/10	10/10	10/10	10/10	10/10	10/10
200	10/10	10/10	10/10	10/10	10/10	9/10
500	10/10	10/10	5/10	5/10	4/10	3/10
750	0/10	0/10	0/10	0/10	0/10	1/10

Note: the color scale is used to denote from green (100% successful) to red (unsuccessful) experiments.

3.2.3. Effect of Data Drop in the Communication Network

In this experiment, the quality of a controller's output signal is analyzed for varying network delays and varying data-drop rates injected simultaneously in the communication network. The controller regulates the power output of the inverter inside the BESS, as demonstrated in Section 3.1. However, its performance is expected to deteriorate under stressed communication network conditions (i.e., higher delay and higher data-drop rates). The results of these tests are summarized in Figure 15. It can be observed that the analog output of the remote controller loses the control signal resolution under higher network delays and higher data-drop rates. However, as discussed earlier in Section 3.1, the control objective of the SSGC does not involve any management of fast system dynamics. Thus, in the short term (up to 30 s), the SSGC-driven control architecture can sustain itself even while operating within a tampered network under drastic delay and data-drop conditions.



Figure 15. Control signal received in the Typhoon HIL microgrid model from the SSGC under varying network delay and data-drop rates.

An additional set of trials were conducted for this experiment. In these trials, the SSGC was set to operate freely under tampered network conditions, and experiments were run to test whether or not it can sustain itself for **longer periods** of time. The network was tampered with by introducing network delays and data drop. Under these conditions, the network was kept running for 10 min. After 10 min, it was determined if the SSGC was still receiving all the PMU streams successfully and if the real-time simulator was still receiving the controller's output. Observations were taken 10 times for each communication network delay and data drop can both adversely effect the robustness of the SSGC. In fact, in a situation where the SSGC is subjected to both a high network delay coupled with a high data-drop rate, the SSGC is almost certain to be unable to sustain itself for a long period of time. However, for lower delays and lower data-drop rates, the SSGC is proven to be reliable. For instance, consider the case for a 0.5% data drop and 50 ms delay: 10 out of 10 runs were sustained, while for a 5% data drop and 200 ms delay, only 2 out 10 runs were sustained.

Delay	በ%	0 5%	1%	フº /_	5º/	10%	
Drop Rate (%)	0 /0	0.5 /0	1 /0	2 /0	570	10 /0	
0 ms	10/10	10/10	10/10	10/10	10/10	3/10	
50 ms	10/10	10/10	10/10	10/10	9/10	0/10	
100 ms	10/10	10/10	10/10	9/10	7/10	0/10	
200 ms	10/10	10/10	10/10	6/10	2/10	0/10	
500 ms	10/10	10/10	5/10	0/10	0/10	0/10	
750 ms	1/10	0/10	0/10	0/10	0/10	0/10	

 Table 3. SSGC performance under varying communication network conditions.

Note: the color scale is used to denote from green (100% successful) to red (unsuccessful) experiments.

3.2.4. Effect of Jitter on the Communication Network

Jitter is defined as the variation in the time delay between when a signal is transmitted and when it is received over a network connection. The CT910 hardware has the provision of incorporating two parameters: *jitter amount* and *jitter frequency* in the network configuration. The parameter *jitter amount* defines the maximum amount of delay mismatch introduced in the network, and the *jitter frequency* determines what percent of data packets would experience the jitter. For this experiment, a jitter frequency of 10% and a maximum jitter delay of 500 ms was introduced in the network. This test was repeated with and without the jitter present. Figure 16 shows the effect of jitter on the control signal being transmitted by SSGC. The jitter delay was maxed at 500 ms, which meant that only a few packets would be experiencing a jitter delay around that range. Experimentally, it was observed that the effect of jitter is visible intermittently for some brief windows (denoted by red boxes in Figure 16), during which the control signal slows down its update rate significantly (thus dropping the high-frequency components). However, these windows are short and are only observed while the applied jitter delay is close to its maximum permissible limit of 500 ms.



Figure 16. Control signal received in the Typhoon HIL microgrid model from the SSGC with (**a**) and without (**b**) jitter present in the network.

3.3. Control Performance Enhancement through LPF Functions

It needs to be noted that only one scenario for controlling the DERs within a microgrid is demonstrated in this paper. In that scenario, the battery is covering for a step increase in the load. While this experiment is an important 'proof of concept', additional experimentation is crucial before implementing the proposed architecture to control real-world DERs.

In real-world applications, the behavior of a BESS-based DER in a power system is more complex than what simulation models can capture, and more importantly, the operation of the controllers are restricted by the physics of the battery. In fact, the batteries utilized in energy storage systems are limited by their response times, which are different during charging and discharging operations in addition to their power availability. The authors of [46] reported that the average response time for a Battery Energy Storage System during charging is about 2.2 s and during discharging is about 0.6 s. Keeping these numbers in mind, the battery cannot be subjected to faster changes than those allowed by the charge and discharge rates. Hence, when aiming to control power flows to balance load/generation changes, any frequency variations, if kept unfiltered, would rapidly increase the switching and would generate excessive heat, thus compromising the health of the batteries.

To address this issue, a practical approach is adopted to restrict the response bandwidth of the proposed controller. To this end, a low-pass filter was introduced as an SSG function, with the goal to eliminate the high-frequency variations in the control signal. In addition, it may also slow down the response of the overall control response. Hence, the LPF needs to be adequately tuned. To illustrate, experiments are conducted by varying the cut-off frequency of this LPF from 4 Hz to 0.25 Hz. The control responses of each of these cases are demonstrated in Figure 17. It can be seen from the results that at a lower cut-off frequency (\leq 0.5 Hz), the control system is free of high-frequency components, and the control signal can be safely employed in the BESS without exposing the BESS to overswitching. These filters can reliably bring the response of the SSGC-based control system within the permissible limit for battery operations, as reported in [46].



Figure 17. Application of LPFs to reduce overswitching of the BESS unit being controlled by the SSGC hardware.

3.4. Control System Redesign to Utilize Phase-Angle Measurements

As a 'proof of concept' that the SSGC can support different control functions, in this section, the control system is redesigned to utilize the phase-angle difference as the controller input, and the power flow is regulated the same way as before. The usage of the phase angle to control the power flow is a tried and tested technique which has been proposed, theorized and archived in [47–49]. Synchrophasor technology is capable of reporting accurate phase-angle measurements in real time [35–38]. This makes this technology suitable for phase-angle-based power-flow control. In this paper, the phase-angle difference between the load and the point of common coupling is used as the control variable to direct the power flow from the BESS. It is to be noted that, for distribution systems, the angle difference between the buses can be very small. Hence, the controller needs to be tuned with precision. Thus, even though the control system architecture is independent of the control variable (the active power or phase angle), the internal PI controller requires significant retuning.

Experiments were performed with the BESS power output being controlled by the phase-angle difference $\delta_{PCC} - \delta_{load}$. The results of this experiment are summarized in Figure 18a–c. It can be observed from Figure 18c that the active power output increases from $\simeq 100$ kW to $\simeq 400$ kW. This response is consistent with the results demonstrated previously in Figure 11c.



Figure 18. Control system performance for the BESS under ideal network conditions with phase angle utilized as the control signal: (**a**) 300 kW load injection by switching load, (**b**) response of the control variable $\delta_{PCC} - \delta_{load}$ to the load change and (**c**) active power output from the Battery Energy Storage System (BESS) equipped with phase-angle-based active power control.

4. Future Works

The current paper introduces a new architecture for control system implementation for DERs in microgrids by utilizing synchrophasor measurements. As a 'proof of concept', one specific case study was tested where the BESS output is increased to match the step increase in the load. Different cases featuring the control of a full range of DERs and a full range of behaviors on the load side, microgrid conditions, etc., must be performed in order to demonstrate the resilience and robustness of the proposed architecture. This work is outside the scope of this paper and is left as future work.

For BESSs, the state of charge (SOC) of the battery is a crucial parameter. In all realistic BESS control systems, based on the SOC, the battery is often put into either charging or discharging mode. The current paper assumes the SOC to be high enough so that the battery can reliably operate in discharging mode; i.e., it can feed active loads. For real systems, this will not be the case. To address this, an additional control loop must be designed to utilize the SOC of the battery and ensure the safe and reliable operation of the BESS. This requires coordination and information exchange with Battery Management Systems (BMSs) and will be the subject of future research.

5. Conclusions

The proposed Synchrophasor Synchronization Gateway and Control system can reduce the complexity and latency of the synchrophasor system and communication network when compared to traditional WAMS/WAMPAC systems by exploiting and expanding upon the existing *Khorjin* library. This architecture was utilized successfully to implement a networked control system for a real-time microgrid model.

A scenario for controlling the DERs within the microgrid was used for experimentation in this paper. In that scenario, the BESS is capable of using synchrophasor data from different locations to respond to a step increase in the load. It was also demonstrated that this architecture can be successful irrespective of the actual control algorithm being employed within it.

Experimentally, the SSGC architecture was tested under different network conditions to establish its validity and robustness. More specifically, the network was subjected to delay, jitter and data drops through external hardware. The performance of the controller was evaluated under those different network conditions. It was observed that for lower values of the data-drop rate ($\leq 2\%$) and lower values of the network delay (≤ 100 ms), the SSGC-based control system is reliable. It was also observed that the introduction of jitter makes the controller lose a significant amount of high-frequency components. However, up to a maximum jitter occurrence of 10% and maximum jitter delay of 500 ms, the SSGC sustains itself successfully even for longer runs.

Finally, an LPF was designed to prevent the BESS from overswitching. This filter would ensure that the battery operations are within the physical limits of the battery and thus increase the lifetime of the battery units within the BESS.

The main limitation of the implementation presented in this work is the cost associated with the National Instruments' cRIO hardware. While such hardware was ideal for prototyping and testing, it is cost prohibitive for product development. For the real-world deployment of the proposed architecture, it would be crucial to utilize a low-cost hardware platform to make it economically viable. Consequently, migrating the *Khorjin* dynamically linked library (DLL) to a different platform is the first step towards the authors' future work.

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Abbreviations					
BESS	Battery Energy Storage System				
DER	Distributed Energy Resources				
HIL	Hardware-In-the-Loop				
CHIL	Controller Hardware-In-the-Loop				
LPF	Low Pass Filter				
PCC	Point of common coupling				
PMU	Phasor Measurement Unit				
PDC	Phasor Data Concentrator				
PV	Photovoltaic				
SSG	Synchrophasor Synchronization Gateway				
SSGC	Synchrophasor Synchronization Gateway and Controller				
WACS	Wide-area control system				
WAMPAC	Wide-Area Monitoring Protection and Control System				

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