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Experimental Testing of a Real-Time Implementation of a PMU-based Wide-Area Damping Control System

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ABSTRACT The modern power grid is being used under operating conditions of increasing stress, giving rise to grid stability issues. One of these stability issues is the phenomenon of inter-area oscillations. Simulations have demonstrated the advantages of Wide-area Measurement Signals (WAMS)-based Oscillation Damping Controls in achieving improved electromechanical mode damping compared to traditional, local signal-based Power System Stabilizers (PSS). This work takes an existing Phasor-based oscillation damping (POD) algorithm and uses it to implement a proof-of-concept, real-time controller on National Instruments hardware. The developed prototype is tested in a real-time Hardware-in-the-loop setup (RT-HIL) using OPAL-RT's eMEGASIM real-time simulation platform and synchrophasor data from actual Phasor Measurement Units (PMUs). The prototype and experiments provide insight into the feasibility and real-world limitations of wide-area controls. Further, it is demonstrated how the proposed control architecture has applications independent of the controlled device. Challenges faced, the solutions implemented together with the present prototype's limitations are also discussed.

INDEX TERMS Power system dynamics, power system stability, power system simulation, power generation control, phasor measurement units

ABBREVIATIONS

AVR	Automatic Voltage Regulator
cRIO	Compact Reconfigurable Input-Output
FACTS	Flexible AC Transmission System
FPGA	Field-programmable Gate Array
HIL	Hardware-in-the-loop
NI	National Instruments
PDC	Phasor Data Concentrator
PMU	Phasor Measurement Unit
POD	Phasor Oscillation Damper
PSS	Power System Stabilizer
RT	Real-time
SVC	Static VAR Compensator
TCP/IP	Transmission Control Protocol and the Internet Protocol
WAPOD	Wide-Area Phasor Oscillation Damper

I. INTRODUCTION

ALTHOUGH the purpose of interconnecting disparate power networks was to increase stability, in the present situation power systems now have to cope with increasing injection of renewable energy sources through constrained power trading corridors, which may impact system stability. One of important stability issue is the phenomenon of electromechanical oscillations [1], both inter- and intra-area. Inter-area oscillations involve groups of generators loclated in two distinct electrical areas oscillating against each other. These groups are typically connected by weak tie-lines [1]. Inter-area oscillations are typically of a lower frequency ($< 1Hz$) relative to intra-area oscillations and are often poorly damped leading to stability problems [1]. Modern solutions to the problems of inter-area and intra-area oscillations use Power System Stabilizers (PSS) [2]. While a PSS provides excellent damping to intra-area modes with good local ob-

servability, its performance with inter-area modes may not be satisfactory [3]. The limited inter-area mode observability in a local signal can be complemented by wide-area, synchrophasor data. Wide-area data allows for calculations and observations such as voltage angle differences, which are not possible with solely local measurement data [4]. This opens the possibility to develop new synchrophasor-based damping control systems that can help with inter-area oscillations. For a more complete treatment of the phenomenon of power system electromechanical oscillations, see [5].

A. LITERATURE REVIEW

1) Feasibility and Design Studies

It has been shown in [4] that wide-area signals are preferable to local signals, such as active power and frequency [3], for the purpose of damping inter-area oscillations. Studies such as [4] have analysed damping performance when using signals such as voltage angle difference, which can easily be computed using data from multiple Phasor Measurement Units (PMUs). Similar studies using off-line simulation-based studies that analyze the use of remote/PMU-based signals in damping loops can be traced to the 90's [6] until recently [7], and have largely focused on control design aspects [7], analysis of communication impact and impairment [8], [9], signal selection [10], etc. Nevertheless, very little research has addressed the actual implementation of such type of control systems in practice other than field testing, with notable exceptions [11] that focus on gain scheduling and model identification approaches. This work seeks to expand on the literature by reporting important implementation aspects not currently discussed in the literature.

The damping performance of a controller that depends on inter-networked data for input is constrained by the network transport delay. Beyond a certain value of time delay, damping will cease to be effective. These effects are explored in more detail in [12], [13], [8] and [14]. This work's treatment of communication network delay is limited to measuring and reporting delay values.

2) Field Tests

Successful field trials of wide-area oscillation damping controllers are reported in [2] and [15] indicating the potential that PMU-based wide area controllers have to offer. These results are not without certain limitations. In [2] it is reported that the limited set of tests conducted with the Wide Area Power Oscillation Damper (WAPOD) are insufficient to compare the performance of a WAPOD to a local-measurement based controller. Coordinating field experiments is often difficult and requires the participation of several entities. This work attempts to approximate real-world conditions as closely as possible by using real-time hardware-in-the-loop simulation incorporating a hardware-based controller prototype, but avoids several of the limitations of working with an operational power system. A more recent demonstration was carried out in 2017 [17] where synchrophasor-sourced voltage angle data was used to damp an inter-area mode in the WECC grid. Unlike our work, [17] uses a derivative filter on bus frequencies and then controls active power flow through an HVDC line to provide damping action. This method is more sophisticated than our work as it selects the best pair from among several PMUs and accounts for network communication delay but has not tested this output with different control mechanisms. Unlike our work, [17] is tested with a live power system and so requires a more sophisticated implementation. Another example of using wide-area synchrophasor data to damp inter-area oscillations is [18]. This work modulates active power in an HVDC link to damp intre-area modes however, even the inter-area modes in the system considered are already damped i.e. the system is not inherently unstable.

B. PAPER CONTRIBUTIONS & GOALS

The specific goals behind this work are:

1) To implement an existing oscillation damping algorithm on real-time hardware and to use synchrophasor data as algorithm input
2) To test the implemented algorithm in real-time so as to mimic a real-world scenario as closely as possible in terms of controller input and response time
3) To demonstrate that the developed controller is able to provide system damping despite real-world constraints such as signal noise & communication delays

The goal of this paper is to implement a hardware prototype and to demonstrate experimentally the potential and flexibility in oscillation damping controller design that is possible by using synchrophasor data (IEEE C37.118). The Phasor Power Oscillation Damping (Phasor-POD) algorithm, originally developed by Ängquist and Gama [19], is implemented and deployed on a National Instruments Compact Reconfigurable Input / Output (cRIO) real-time controller. The Phasor-POD algorithm is demonstrated to provide effective damping in [24] and our work broadly follows the approach presented in [24]. A modified, Simulink model of the four-machine, two-area network developed by Klein-Rogers and Kundur [1] is executed in real-time on the eMEGASIM [20] platform from OPAL-RT. This allows interfacing an externally generated control signal with the simulated model in real-time. A Hardware-in-the-loop (HIL) test is set up to verify the performance of the hardware implementation of the Phasor POD algorithm. Although this work does not use an operational power system, its behavior is closely approximated through the use of analogue data inputs to commercial PMUs which includes real-world constraints such as signal contamination through noise and communication delays. The flexibility of the developed controller is demonstrated by extracting, in real-time, various data from the synchrophasor data-set and using each as a damping input to the controller. This paper also illustrates that the controller can have multiple applications by testing it with two different controllable devices; a generator automatic voltage regulator (AVR) system and a Flexible AC Transmission System (FACTS)-

device excitation system. A brief analysis of the performance of each synchrophasor input to the hardware POD is also presented.

C. A NOTE ABOUT THE USAGE OF 'REAL-TIME'

In the context of this paper, the term 'real-time' is used to refer to a controller where input data is processed and made available as output within a deterministic time frame. The usage of the term is similar to that in the field of embedded systems in that strict deadlines are imposed and system reaction time is guaranteed and fixed. To this end, the real-time simulator's clock runs synchronously with the real-world clock and therefore generates and processes data in real-time. This requires that any external, hardware controllers connected to it operate at an identical pace. These constraints imply that the algorithm implementation in this work is tested under conditions that closely approximate a real-world situation. Constraints such as signal magnitude limits, variable network communication delays and noise apply. If the proposed hardware implementation of the POD algorithm fails to respond in a deterministic manner, it is deemed to have failed.

D. LIMITATIONS OF EXISTING CONTROLLER DESIGNS

Problems exist with traditional damping controller design that is based around model linearisation and off-line non-linear simulations [15]. This paper circumvents these issues by adopting a phasor-based damping algorithm [19] that can operate independent of the network configuration. In addition, because this is a similar algorithm used in proprietary implementations [2], the prototype developed is directly comparable to other real-world implementations. The developed controller is designed with modularity and portability in mind, as it is possible to deploy in other similar hardware platforms from National Instruments, and is demonstrated to be able to provide effective damping in multiple application scenarios. Although [4] presents a scenario where the generator AVR's error signal is modulated using PMU data, this work presents an experimental validation of those results. While multi-mode damping can be attractive [16], the focus of this work is single-mode damping to verify and be comparable to real-world cases that have been deployed to date [2], [15] .

E. PAPER ORGANISATION

This paper is organized as follows. Section II presents a brief, theoretical background of the work presented in this study while Section III introduces the software and hardware used. Section IV covers the preparation of the Simulink models for real-time simulation and two real-time test cases, one with the WAPOD input fed to the excitation system of a Static VAR Compensator (SVC) and the other with the WAPOD modulating the input of a generator's Automatic Voltage Regulator (AVR). The results obtained from the two tests are presented and analysed in Section V. Section VI examines some of the major challenges faced in the development, implementation and testing of this WAPOD controller. No experimental implementation is ever ready for the field and there is always room for improvement. This is outlined in Section VII and finally conclusions are drawn in Section VIII.

II. BACKGROUND

A. WHY IS THE PHASOR-BASED ALGORITHM USED?

Traditional controller design for synchronous generators and FACTS devices depend on accurate system models at a specific operating condition. Large systems often experience changes in their topology and data about the present condition may not always be available to apply conventional control design methods. Further, identifying system oscillation modes and designing appropriate dampers is based on small signal and linear analysis techniques applied to power system models has inherited limitations. These models are often difficult to derive and maintain for large and inter-connected power systems [21], therefore limiting their accuracy to represent the real grid. In addition, linearised models are also only valid for small deviations from the linearisation point. One important reason for choosing the Phasor-POD algorithm for real-time implementation in this work was the fact that the algorithm itself uses limited inputs and is independent of network configuration and topology (i.e. it does not require a power system model). The only network-dependent algorithm parameter is the oscillation frequency and this is usually known from system studies or can be determined directly from synchrophasor measurements [22]. Compared to conventional controllers designed using linearisation-based methods, the adoption of phasor-based controllers has not been common mainly due to the fact that such controllers tend to be highly non-linear and thus difficult to, both, model in simulation studies [23] and implement in real-time applications [2].

B. PHASOR POD ALGORITHM

Some of the problems that emerge from the model linearisation approach are addressed by phasor-based oscillation damping algorithms. The algorithm chosen for implementation here is the Phasor-POD algorithm developed by Ängquist and Gama [19]. The measured signal $s(t)$ can be represented as a space-phasor [23]:

$$s(t) = s_{avg} + \mathrm{Re}\left\{\vec{s}_{ph} \cdot e^{jwt}\right\} \tag{1}$$

where, $\vec{s}_{ph}$ is a complex phasor, rotating at the frequency ω [19]. This presents an average value and the associated oscillatory part, in a stationary reference frame. The oscillating part can then be used to generate a control signal for the FACTS (or other controllable device) using a control algorithm. This method is independent of the system state or configuration and is not computationally intensive. Controllers based on this approach may also incorporate error checking and phasor estimation algorithms. The real-time hardware implementation of the Phasor-POD algorithm was

based on the Simulink implementation in [24] and its goal was to replicate the behaviour of the Simulink implementation as closely as possible. The algorithm accepts three inputs; the search frequency, ω_{cs1}, the sampling time T_s, the phase correction $alpha$ in addition to a signal scaling factor. It takes advantage of the fact that the oscillation frequency for a given network configuration is usually known, which in this case is the 0.64Hz inter-area mode. Using this known frequency value, a co-ordinate system, rotating at this known frequency, is set up where the oscillating component is continuously extracted as a phasor [19]. In simpler terms, the Phasor-POD algorithm separates an input signal into an average valued and an oscillating component. The oscillating component, when suitably phase-shifted, can be used as a supplementary damping input to a generator's AVR or the excitation system of a FACTS device. In this work, the search frequency and sampling time are known and constant while the phase correction depends on the communication delay, a situation that is similar to the real-world. We determine the required phase compensation $alpha$ through measurement of the end-to-end delay (see Fig. 8) and then convert this value to a corresponding angle. This is described in more detail in Section VI-A. We assume that the communication delay and therefore the phase compensation $alpha$, remain relatively constant over a given time.

III. SOFTWARE ARCHITECTURE AND HARDWARE CONFIGURATION

The WAPOD[1] prototype developed here uses commercially available micro-controller hardware and uses PMU measurements received over a TCP/IP network. The Phasor-POD algorithm [19] was executed on the control hardware in real-time. The inputs to the controller come from one or multiple PMU's, each monitoring data at different points of the power system. The power system model used in this paper is the two-area four-machine model, originally proposed by Klein, Rogers and Kundur [1]. To prove the real-world applicability of the developed controller, all tests are carried out in real-time, with conditions such as measurement noise and communication network delay present.

A. HARDWARE CONFIGURATION

The power system model was simulated in real-time on OPAL-RT's eMegasim [20] real-time simulation platform (Figure 1). This model was interfaced with externally generated, analogue signals in a HIL configuration. Current and voltage signals from different points (Buses 5 and 11 in Figure 4) on the simulated network are extracted as analogue signals, amplified and then supplied as inputs to two PMUs. Two cRIO-9076 [25] devices are used as PMUs, although any other commercial device could be used. Each PMU is equipped with three-phase analogue voltage and current input modules in addition to GPS time synchronisation. The PMUs report data every 20 ms. The synchrophasor data stream generated by these PMUs is sent over a TCP/IP network to a Phasor Data Concentrator (PDC) which produces a time-aligned output stream. This stream is then accessed on a PC running LabVIEW over a TCP/IP network. Data is extracted and sent to the FPGA (Field Programmable Gate Array) running the Phasor-POD algorithm. The FPGA on the cRIO-9081 [25] generates a damping signal which is then wired back to the real-time simulator for use in the Simulink model.

Reference [24] describes the details of the equipment used here. It is important to note that the data flow in Figure 1 involves both D/A and A/D conversions. Also, because no synchronisation is used for these conversions, it is important that the sample rates or loop rates of each section be integer multiples of each other. This prevents data sampling errors. The issue of different loop rates is discussed in Section VI-C.

B. SOFTWARE ARCHITECTURE

As shown in Figure 2, LabVIEW's Real Time and FPGA software was used to write the code for the respective sections of the cRIO. Because no synchrophasor data-extraction software was available that could run independently on the RT controller, the process of extracting raw measurement data from the synchrophasor data stream was performed on a desktop computer. The software used for this was the Smart grid Synchrophasor Software Development Kit (S^3DK) which runs on a workstation computer, extracts data from the PMU stream and sends this extracted data to a LabVIEW program running on the same computer[2]. Using the S^3DK, a LabVIEW application was implemented to select the PMU's from which the data was to be utilized. Once available in LabVIEW, this data was then sent to the RT controller using LabVIEW's Shared Variables [32] over a TCP network.

C. REAL-TIME IMPLEMENTATION OF PHASOR-POD ALGORITHM

The hardware implementation of the POD was based on the cRIO 9081 [25] from National Instruments. This controller is equipped with an on-board FPGA (maximum clock speed of 80Mhz[3]) in addition to an independent real-time controller (1.06GHz Intel Celeron U3405).

A three-layer, modular code architecture [26], following guidelines from the manufacturer [29], was selected for implementation. An outline of the architecture is shown in Figure 2 and each of the three layers are briefly described below (Corresponding to the numbers in Figure 2).

1) Remote Interface: Runs on a standard, workstation computer. Used to input algorithm parameters and monitor data & performance. Receives the aligned

[1]Historically, damping stabilizers have been termed WAPOD where the P represents a measurement of active power through the line. Active power here would be used as a controller input signal. Although this term is not accurate when other quantities are used as control inputs or feedback signals, the term is used here to maintain consistency with existing literature.

[2]Available open-source at https://github.com/ALSETLab/S3DK

[3]http://www.xilinx.com/support/documentation/data_sheets/ds162.pdf

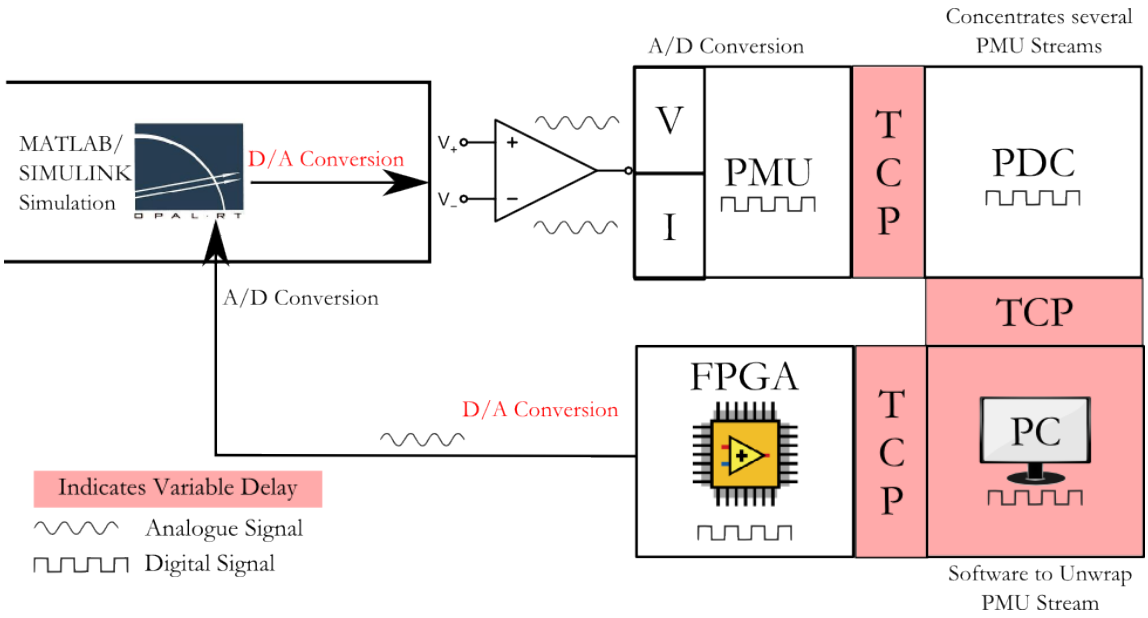

FIGURE 1. Hardware loop showing complete data path, signal nature at each point and sources of delay.

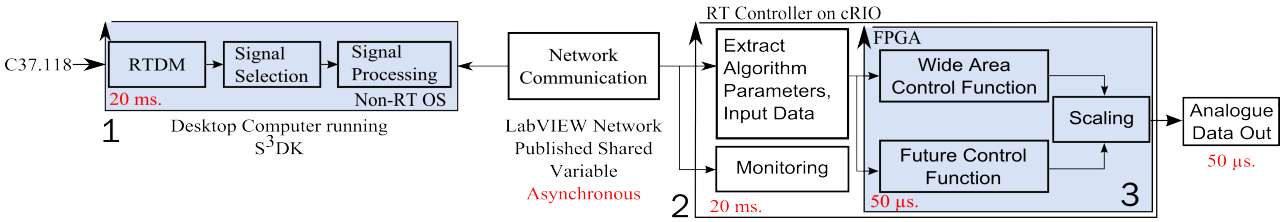

FIGURE 2. Three-layer Software and Hardware Architecture of the WAPOD Controller. Loop rates are indicated in red.

synchrophasor data stream and extracts measured value data. This layer is non deterministic in time.

2) Real Time (RT) Software : Manages network communication to the remote interface and also generates performance monitoring data. The remote interface interacts with this layer over the communication network. Transfers extracted synchrophasor data to the FPGA.
3) Core FPGA Software : Interacts with hardware terminals for I/O and runs the Phasor-POD algorithm. Input data comes through the RT interface running on the cRIO.

The Phasor-POD algorithm could be implemented on either the real-time section of the cRIO or the FPGA but was implemented on the FPGA. This decision was made keeping in mind the computational resources and response speed needed to match the step size of the real-time simulator. The complexity of the code meant that the cRIO's real-time controller would not be able to complete each iteration of the algorithm in the required 50μs response time. The real-time section of the cRIO only handles network communication. Its primary purpose is to receive measurement data that the workstation computer extracts and to stream this data to the Phasor-POD algorithm running on the FPGA. The real-time controller also handles commands coming from the user interface running on the workstation computer. It also monitors the output of the FPGA, sends data to the user interface for monitoring, periodically logs input and output data and handles error conditions.

The remote interface runs in LabVIEW on a conventional computer. The Phasor-POD algorithm can be controlled and monitored from this interface. The operating system here is not real-time but multi-tasking. The execution speed therefore depends on the processor load and is not deterministic. The S^3DK was used to unwrap the PMU streams coming from the PDC and extract phasor measurements. This allowed for data to be extracted and used directly in the LabVIEW environment. The PMU reporting rate was 50 messages a second and new data was available every 20ms. The loop rate used by the S^3DK was therefore 20ms. The selection of an input signal for the controller and any signal processing required are performed here. For example, if active power is to be used as a POD input, voltage and current values must be multiplied to obtain the active power.

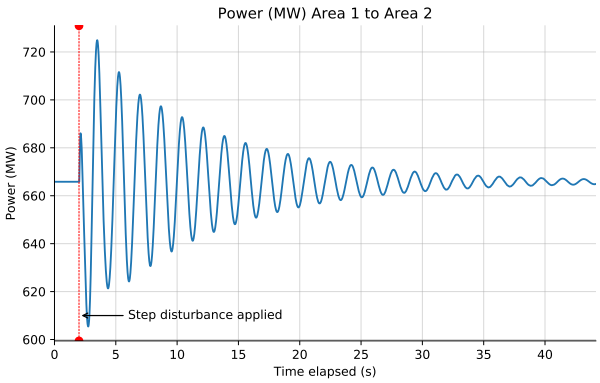

FIGURE 3. Damping performance of the base case PSS only at Machine M1. Local active power is used as the PSS input.

If the voltage angle difference is to be used as an input, the required calculations are performed in this LabVIEW Virtual Instrument (VI[4]).

IV. EXPERIMENTAL SETUP

The nature of the Phasor-POD algorithm is generic enough to allow it to be used as a modulating input to a variety of controlled devices. Two examples are illustrated in this work, one, as a damping controller modulating a generator's AVR system and the other as a modulating input to the excitation system of a FACTS device (here, an SVC). Figure 4 illustrates both these uses along with the two-area network outline. Note that both functions are not implemented simultaneously.

A. TWO-AREA MODEL PREPARATION - GENERATOR AVR

The original Klein-Rogers-Kundur model in [1] was modified for the studies in this work. In order to assess the performance of the WAPOD, the base case employs a damping control system (PSS) only at Machine M1 in Area-1 (see Figure 4). All other machines do not have a PSS installed. The WAPOD output is used as an additional input to machine M1's AVR system. This configuration was verified to be stable and is able to restore the system to stability after the application (and subsequent clearing) of an 8 cycle, three-phase to ground fault at bus 8 in Figure 4. Note that without the action of the PSS, the system is unstable. To demonstrate a potential application scenario for the developed POD prototype, the performance of the PSS was set up so that it is able to provide damping but with a long response and settling time (Figure 3). This figure shows the system response to a 200 ms., 5% perturbation in the voltage reference of machine M1. Note that under the action of the sole PSS at machine M1, the inter-area mode is damped and the system is restored to stability. This mimics a real-world situation with an already installed PSS whose performance has degraded over time due to changing network conditions or poor tuning. Using only one PSS ensures that the inter-area mode is clearly visible.

The intent of this modification is to demonstrate that a hardware implementation of the POD algorithm can improve system damping despite the controller's real-world limitations. It is not the goal of this work to demonstrate that a hardware-based controller is able to improve system damping with a PSS installed at each machine. Though this may be possible, this work only seeks to demonstrate that a hardware implementation of a Phasor-POD based on synchrophasor data is able to function as expected.

B. TWO-AREA MODEL PREPARATION - FACTS DEVICE

The second application in Figure 4 is to use the WAPOD output as a modulating input to an SVC's excitation system. The two-area model was prepared for simulation in the same way as in the previous case, however, in this case a PSS was included at all four machines. The SVC model implemented was an average-value model, identical to that used in [24]. The SVC was connected at the mid-point of the two area network (Bus 8 in Figure 4). As shown in [28], this is the point where voltage swings will be the greatest and also where the SVC can be most effective at damping power flow swings. For comparison purposes, two parallel and identical implementations of the Phasor-POD algorithm were used, one implemented in Simulink and the other on the cRIO. Either could be switched in at a given time. It is important to note here that when the hardware-POD was switched in, the PSS's at each of the four machines were disconnected, leaving the SVC as the sole control and damping device in the network. The ability of the SVC to keep the network stable and also to restore it to stability was verified with off-line simulations using the Phasor-POD implemented in Simulink.

C. REAL-TIME SIMULATION

The modified network in each case was grouped into subsystems and prepared for simulation using RT-LAB [20]. The simulation time step chosen was 50μs meaning that outputs and inputs of the real-time simulator were updated every 50μs. Current and voltage measurements were taken from the buses marked (in green) in Figure 4 and were extracted via the analogue outputs of the real-time simulator. The damping signal dVpod in Figure 4 was generated at two points; one in the real-time simulation itself using a Simulink implementation of the Phasor POD algorithm and one externally on the cRIO. Both signals were generated simultaneously and either one could be switched in for use in the simulation.

V. TESTING & RESULTS

The POD algorithm implemented in Simulink uses locally available active power measurements as input. In the case of the Generator PSS, this is the active power measured at the terminals of the generator. In the case of the SVC, the active power at the mid-point of the interconnecting line (also the point of connection of the SVC) is used as an input. The WAPOD hardware prototype can use these

[4] A LabVIEW program. See http://www.ni.com/white-paper/7001/en/

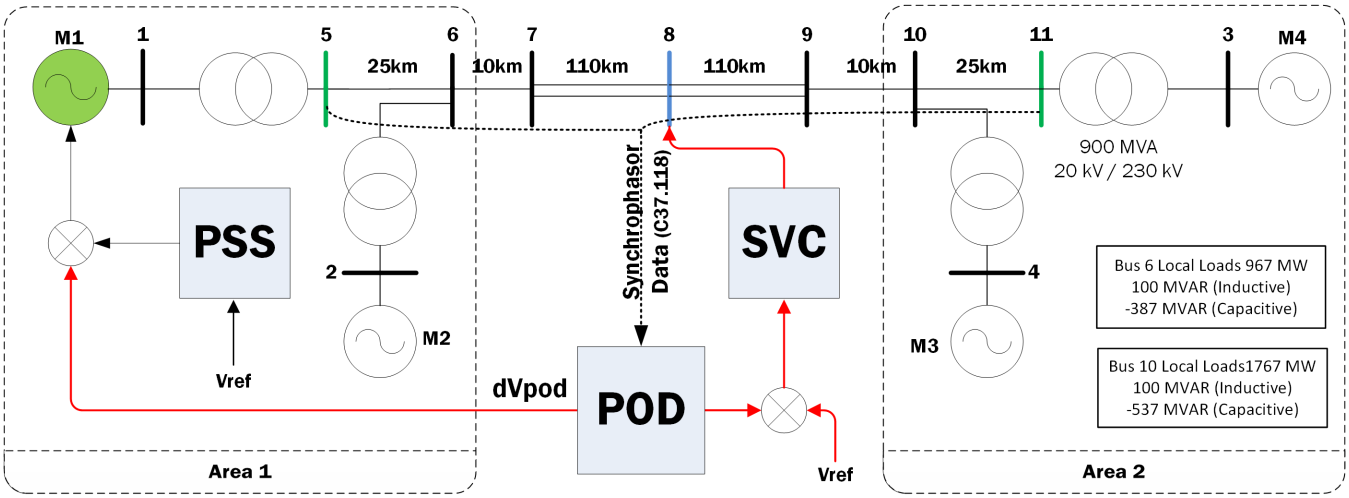

FIGURE 4. Modified Two-Area Four-Machine network outline showing PMU data sources and both uses of the POD damping output. Note that only one scenario is implemente

same signals as inputs in each case but can also exploit other data from the synchrophasor data stream. Testing the operation of the hardware prototype involved using the HIL setup outlined in Figure 1 and verifying whether steady-state stability could be maintained in the simulated two-area network. This test proved that the hardware prototype was able to prevent the existing inter-area oscillation mode from increasing in magnitude. Once this was demonstrated, the inter-area mode was excited by perturbing the voltage reference V_{ref} of Machine M1. The oscillations caused by this disturbance would then be damped out by the proposed controller. Testing was carried out in two phases, one with the Simulink POD operational and the other with the cRIO-based WAPOD feeding in to the real-time simulation. In the latter case, three different damping inputs were tested: active power, positive sequence current magnitude and the voltage angle difference between buses 5 and 11 in Figure 4.

A. SVC EXCITATION SUPPLEMENTARY INPUT

Figure 5 illustrates the response of the hardware controller to a small disturbance at machine M1. This disturbance is a 5% change for 200 ms. in the reference voltage of the AVR. This is sufficient to excite the inter-area mode. The best damping performance is achieved using voltage angle difference as a damping input to the Phasor-POD algorithm. This supports the theoretical results discussed in [4]. Response parameters such as settling times and overshoot were calculated based on the response in Figure 5 and are presented in Table 1. The response of the simulated POD (in Simulink) was used as a baseline to calculate the overshoot. The settling time is calculated as the time required for the response of the controller (in volts) to be constrained to +/- 1V.

All data presented in Figure 5 was captured in the real-time simulator. Data was also recorded at other locations in the simulation such as at the PDC but these have a lower time resolution and are thus not presented here. As further proof of the results presented in this work, the output of the hardware controller is captured directly using an oscilloscope (Figure 6).

TABLE 1. Response Parameters : SVC Excitation Supplementary Input

Input Parameter	Percentage Overshoot	Settling Time (s)
Simulated POD (Active Power)	N/A	3.875
Active Power	290.05	13.94
Pos. Seq. Current	142.67	16.95
Voltage Angle Diff.	-11.26	9.66

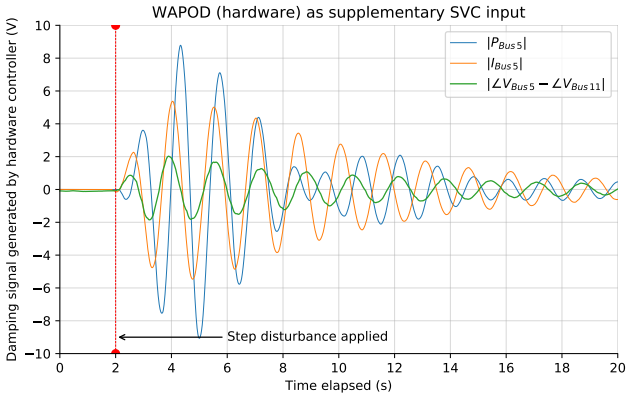

FIGURE 5. Controller Response Comparison : Supplementary SVC Excitation Input.

B. GENERATOR EXCITATION SUPPLEMENTARY INPUT

The controller response to a small disturbance when operating in tandem with a degraded PSS is shown in Figure 7. It can also be noted that the response of the damping signal

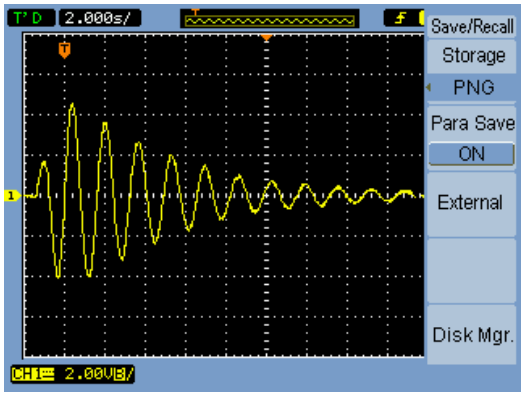

FIGURE 6. Controller Response with Voltage Angle Difference input Captured using an Oscilloscope.

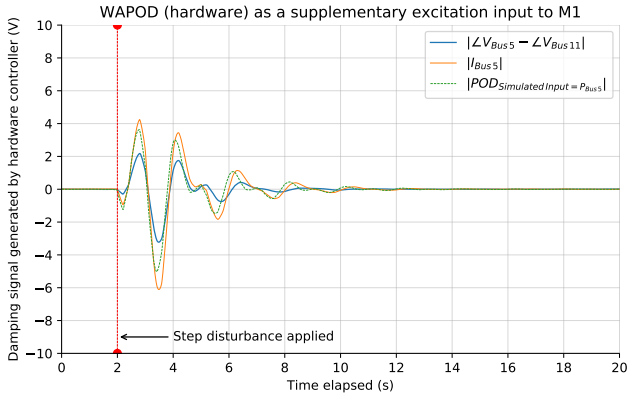

FIGURE 7. Controller Response Comparison : Supplementary Generator Excitation Input.

is significantly different from that in Figure 5, where the dominant 0.64Hz mode is clearly visible. Also evident from Figure 7 is the fact that the damping performance of the WAPOD changes significantly as its input is changed. Using the voltage angle difference as input provides the best performance. The performance of the WAPOD with the voltage angle difference input is very close to the performance of the simulated POD algorithm that uses local active power as input. This performance is achieved despite the presence of a stochastic time delay and noise in the input measurements of the WAPOD. As in the case with the SVC, the theoretical results in [4] agree with the experimental results presented here.

As in the previous case, response parameters such as settling times and overshoot were calculated based on the response in Figure 7 and are presented in Table 2. Definitions are identical to the previous case.

VI. CHALLENGES OF A REAL-WORLD IMPLEMENTATION

Listed below are some of the challenges faced with implementing and testing our real-time implementation of the Phasor-POD algorithm. Solutions are proposed where possible and works subsequent to this are cited where applicable. It is not our aim to provide solutions for nor to examine every challenge in detail. We intend for these factors to serve as considerations for future implementations of such a system.

TABLE 2. Response Parameters : Supplementary Generator Excitation Input

Input Parameter	Percentage Overshoot	Settling Time (s)
Simulated POD (Active Power)	N/A	6.26
Active Power	0.10	6.41
Pos. Sequence Current	23.46	6.53
Voltage Angle Diff	-34.72	5.20

A. TIME DELAYS

The Phasor POD algorithm implemented in Simulink has close to zero time delay between the power system changing and the controller responding. The same algorithm, when run on the cRIO, receives input data with a stochastic delay. It is evident from Figure 1 that several sources of deterministic and stochastic time delay exist. Deterministic delay is due to the analogue amplifiers, the FPGA (50μs) and the real-time processors of the cRIO; these all represent fixed, non-zero time delays. Elements such as the D/A and A/D conversion in the real-time simulator also add a deterministic time delay. However, elements in the data path such as TCP/IP network communication and the PC used to extract raw measurement data from the PDC synchrophasor stream all represent variable delays.

The total delay allows for a network disturbance to grow slightly before the controller begins to respond. This delay also changes the phase compensation required in the Phasor-POD algorithm. The phase compensation needed can be changed from the remote interface, depending on the measured delay. The phase compensation required was calculated experimentally by trial-and-error. The experimentally measured end-to-end delay over the complete data path in Figure 1 averaged 344 ms. This was calculated by logging data in the real-time simulator and measuring the delay between the power system response and the controller response (Fig. 8). Presently, the phase compensation required is determined iteratively and off-line, however, this can be automated using time-stamped data together with an adaptive phase compensation scheme, which is subject to to future work.

Note that the average delay of 344 ms is significant when considering a 0.64 Hz. The delay represents a 40 degree (electrical) delay between the oscillation becoming detectable and the controller responding. Although this is significant, we argue that despite this, the controller was able to damp the oscillations, return the system to stability and to keep it there. Note also from Figure 8 that the end-to-end time delay varied significantly within the same groups of experiments. This was attributed to network traffic. Our method of determining phase compensation via trial-and-error is not idea.

Proposed solution Eliminate non-deterministic components from the communication path. A major contributor to time delay here is executing the (S^3DK) on a non-real time computer. The (S^3DK) is responsible for decoding the PMU data stream. As demonstrated in [33], unwrapping the PMU stream can be performed in a deterministic manner on the cRIO hardware. Reducing components in the signal path such as the PDC is also an option by allowing the real-time controller direct access to PMU data. This solution was not explored in this work.

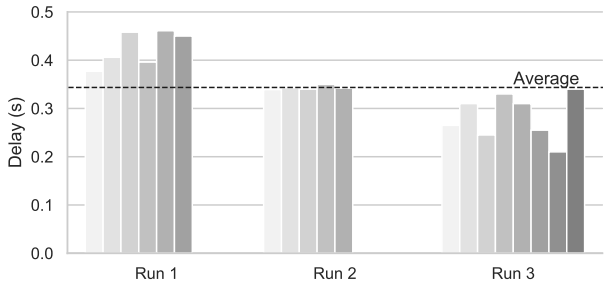

FIGURE 8. Time delay measurements for 19 HIL experiments.

B. ANALOGUE LIMITS AND NOISE

The original POD algorithm [19] was developed and simulated in an ideal, noise-free environment with zero delay (Simulink). More importantly, no limits are imposed on the magnitude of either the controller's inputs or outputs. In contrast, a hardware-based implementation as in this paper, uses analogue signals and thus is constrained by analogue signal limits (see Figure 9). Consider the analogue outputs of OPAL-RT's eMEGASIM simulator which are rated for $\pm 16V$ or $\pm 10mA$ [20]. In contrast, the standard input modules of typical PMU's are rated for 0-300V. A 0-16V analogue signal will not occupy a significant dynamic range of the PMU's inputs. Additionally, a signal of such a small magnitude will be contaminated by noise and will consequently have a poor Signal-to-Noise ratio. A similar argument can be made for the analogue current outputs. Our solution involved amplifying the analogue signals from the real-time simulator to levels that used more of the dynamic range of the PMU input modules. This simultaneously improves both accuracy and the signal-to-noise ratio.

The output of the simulated POD can vary over several orders of magnitude, ranging from 10^5 p.u., at times of peak damping, to as small as 10^{-3} p.u. once the oscillation magnitude becomes small. It is difficult to accurately recreate this output as an analogue signal with such a vast dynamic range. The voltage output module used here had a 24-bit resolution and was limited to $\pm 10V$ in magnitude. Any values generated by the POD algorithm that were greater in magnitude that 10V would have caused output saturation. All these issues meant that signal magnitudes had to be amplified in certain cases to use the full measurement ranges or had to be limited in other cases, so as to capture variations without saturation. This was because a hard-wired POD output was used in our experiment. A solution, that is subject of future work, would be to transmit the POD output digitally, using substation communication protocols.

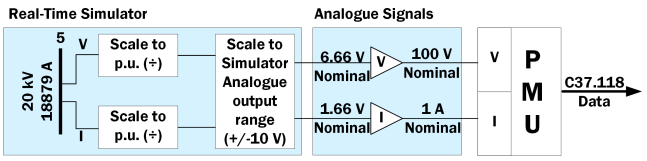

FIGURE 9. Signal Scaling at each step of simulation.

Proposed solution The analogue signal limits are introduced by using analogue components in the signal path such as signal amplifiers and cRIO I/O modules. Eliminating these also eliminates signal limits. A PMU driven by actual power system data will use CTs and PTs for inputs so signal magnitude limits are unlikely to be a problem.

C. LOOP RATES AND FPGA RESOURCES

The most significant challenge in the real-time implementation of the Phasor-POD algorithm was the fact that different sections of the hardware loop ran at different loop rates or step sizes (see Figure 2). Added to this was the fact that the real-time simulator generated data every 50 μs (and thus expected data from the HIL set-up at the same rate) while the rest of the HIL set-up did not support such a high data rate. The PMUs used supported a maximum reporting rate of 50 samples/second. Table 3 lists the different components of the HIL set-up together with their respective loop rates.

TABLE 3. Comparison of Loop Rates of Different Components

Element	Loop Rate	Mode
OPAL-RT Simulator	50μs	Real Time
PMU (cRIO)	20ms	Real Time
Workstation Computer	20ms	Not Real Time
PDC	20ms	Not Real-Time
POD - RT Section	20ms	Real Time
POD - FPGA	50μs	Real Time

50 μs. was chosen for the FPGA loop rate to match the loop rate of the real-time simulator. This ensures that data was always available at the analogue input of the real-time simulator and that no erroneous data points were read. The 50 μs. loop rate of the FPGA meant that new input data was expected every 50 μs., corresponding to a 20000 samples/s PMU sampling rate. The first limitation was the execution speed of the real-time processors of the cRIO, which was limited to 1ms, significantly slower than the FPGA's speed. Further, new synchrophasor data was available from the PMUs only every 20 ms. One solution to this problem was up-sampling synchrophasor data. The major drawback of this method was that the up-sampling process on the RT controller was beyond the computing capacity of the processor and would not run at the required 20 ms. loop rate.

An alternative solution was a sample-and-hold algorithm implemented on the FPGA. The FPGA simply holds any data received by it till new data arrives. This was implemented and found to work satisfactorily.

D. FPGA NUMERIC DATA FORMATS AND ACCURACY

While the FPGA is a fast, deterministic and reliable computational device, it brings with it some limitations. Most of these arise from the fact that an FPGA has no operating system and all circuit logic is directly implemented in hardware. All computations are performed at the bit level, limiting the amount and complexity of computations that can be performed. Functions such as division or multiplication consume significant space on the FPGA [32]. The FPGA on the cRIO9081 implements a numeric representation called Fixed Point [32]. Here, the number of bits assigned to represent the integer and fractional part of a number is fixed before code execution [32]. This assignment must be done in advance of code execution and the FPGA as a whole uses one fixed-point accuracy.

Setting the number of bits used for fractions in the fixed-point representation is constrained by several factors such as the FPGA's analogue outputs, which have finite limits. This limits the maximum integer part of the numbers used in the fixed point representation. Problems arise, however, when handling input to the POD algorithm as its magnitude it not constrained by analogue limits. Observe from Figures1 and 2 that input data to the POD algorithm is digital and is transmitted over a TCP/IP network. This is the challenge with determining the fixed point representation used on the FPGA. Using too many bits for the integer part of the number results in poor fractional accuracy which is important as the analogue outputs have finite limits. Using too few bits for the integer part of the number results in possible rounding and overflow conditions when working with large input data values.

Proposed solution This is an issue unique to the National Instruments hardware used in this implementation and it is not practical to propose a generic solution. Consider a situation where the POD algorithm output is used an an input to an SVC. The SVC has finite reactive power limits and knowledge of these limits combined with a suitable scaling factor can be used to set limits on the POD's output magnitude and therefore its data format and precision.

VII. FUTURE WORK

This prototype is dependent on manual signal selection and algorithm parameter value calculation. These two processes can be automated by having the WAPOD itself monitor the various input signals and intelligently select the one having the highest observability of a particular mode [4]. The algorithm parameters, including the required phase compensation can also be determined adaptively on the WAPOD itself. On the same lines, this can further be extended to include selection among available measurement locations on the network. The fact that a stochastic time delay is introduced by unwrapping the synchrophasor data stream on a desktop computer can be addressed by performing this function on the WAPOD controller (here, the cRIO) itself thus making the whole control loop more deterministic which is part of on-going work [33]. Finally, we suggest testing the developed controller prototype with larger-scale electrical network models and multiple hardware implementations (i.e. on various hardware platforms), all using the real-time, hardware-in-the-loop approach.

VIII. CONCLUSION

This work has provided experimental results showing the feasibility and benefits of using wide-area power system measurements as an input to an oscillation damping controller. The generic nature of the developed controller was demonstrated by using an identical implementation with mere changes in parameters to suit the controlled device's input requirements and capabilities. The hardware prototype developed on the NI cRIO was tested in a real-time HIL setup and was demonstrated to work satisfactorily. Real-world constraints such as time delays and signal conditioning were replicated as closely as possible. The flexibility of synchrophasor data was demonstrated and the wide range of inputs possible from this were also tested. The results from this work serve as experimental proof-of-concept to the theory presented in [4] and pave the way for the development of other PMU-based real-time control systems.

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