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A WACS exploiting generator Excitation Boosters for power system transient stability enhancement

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ABSTRACT

Excitation Boosters (EB) are designed to improve transient stability of synchronous generators equipped with bus fed static excitation systems. They can be controlled using either local or remote signals following a disturbance. This paper explores how critical clearing times (CCT) can be improved by EBs controlled using remote signals. Particularly, Pseudo Center of Inertia (PCOI) and Dominant Interarea Path (DIP) signals derived from Phasor Measurement Units (PMU) within a Wide Area Control System (WACS) are used. Prototype controllers are tested by means of a Real Time (RT) Hardware-in-the-Loop (HIL) experimental setup.

1. Introduction

1.1. Previous work

The Excitation Booster [1] is an ultracapacitor-based device that helps improving the transient stability performance of synchronous generators equipped with bus fed static excitation system. This technology was patented by Alstom Power (currently GE Power) to remedy the limitations of this kind of excitation systems to comply with grid codes Fault Ride Through (FRT) capability requirements. Both, "on–off" control using local measurements and a modulated control exploiting remote signals from a Wide Area Control System (WACS), were explored through simulations in [2].

1.2. Motivation

WACS performance depends on the characteristics of different components comprising it: Phasor Measurement Units (PMU), Phasor Data Concentrator (PDC), communication network and the control systems driving a power component. This kind of systems can be analyzed in better using Real-Time Hardware-in-the-Loop (RT-HIL) simulation can be used to simulate the power system and the Excitation Booster (EB), while closing the loop with actual WACS hardware. In practice, very few WACS have been developed, implemented and tested; with notable exceptions for damping enhancement and voltage control [3–9]. While, no actual prototypes of RT WACS to improve transient stability has been reported in the literature (to the knowledge of the authors), the well-known implementation of Ref. [9] can be considered a precursor of WACS for transient stability enhancement. However, it did not use Phasor Measurement Units (PMU) at the time, and it's coordination with a tripping scheme makes it more similar to a Special Protection Integrity Scheme (SIPS), whereas the authors' approach conforms to the concept of closed-loop control systems.

Previous references suggest using Flexible Alternative Current Transmission Systems (FACTS) devices such as Static Var Compensators (SVC) [3,4,6,8], Static Synchronous Compensators (STATCOM) [6], Synchronous Condensers (SC) [6,8] or HVDC [5,7] as the actuators of their damping or voltage controllers. However, the WACS EB controller presented herein takes advantage of the capability of the synchronous generators' excitation systems as actuators of the controller. The only tested precursor on using the excitation system is Ref. [9] with the difference that it merely raises the voltage reference after a fault detection. By contrast, the WACS EB controller under discussion uses modulation of an ultracapacitor that can be installed in pre-existent facilities as an upgrade. The WACS EB controller uses remote signals based on voltage phase dif-

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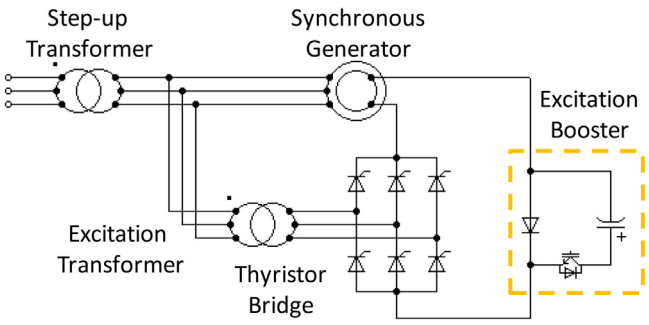

Fig. 1. Bus fed static excitation system with EB.

ferences as Refs. [3,4], and also uses voltage phase signals related to the Center of Inertia (COI).

1.3. Paper contributions, scope and limitations

Although some simulation studies have explored the use of WACS for transient stability enhancements, e.g. Ref. [10], to the authors' knowledge, none of such applications have been implemented nor tested. The contributions of this paper are:

- Use of Pseudo Center of Inertia (PCOI) and Dominant Interarea Path (DIP) based signals to modulate EB voltage to improve transient stability.
- The implementation of the proposed WACS control system in a hardware platform.
- Concept validation trough a Real Time (RT) Hardware-in-the-Loop (HIL) experimental setup including industrial PMUs and PDCs, communicated through standard protocols.

The scope of the paper covers first swing transient stability in a weak power system and how to improve it through EBs distributed across the network and controlled by a WACS.

1.4. Paper organization

The remainder of this paper is organized as follows. Section 2 provides background on the EB device. Section 3 explains the WACS design for EB control. Section 4 deals with the experimental implementation of such a device and describes the architecture of the setup, the constraints that have been found, and means to overcome them. Section 5 presents an analysis from experiments using the HIL prototype, and finally, Section 6 draws the conclusions.

2. Background: Excitation Booster (EB)

2.1. The EB and its operation

Bus fed static excitation systems are among the fastest, cheapest and most reliable ones. However, during faults in the grid; (a) their ability to provide the generator with maximum field voltage is compromised, as their output depends on the generator terminal voltage; and (b) their field voltage must be increased.

The Excitation Booster (EB) [1] is an upgrade to bus-fed static excitation systems to improve their FRT capability as required by grid codes. Fig. 1 depicts a power plant excited by a bus fed static excitation system and equipped with an EB.

The EB is comprised of a fast switch (usually an IGBT), a diode and an ultracapacitor. If a fault is detected in the grid, the IGBT switches on and connects the ultracapacitor to the diode. As they are connected in such a way that the diode's anode to cathode voltage becomes negative, the diode switches off and the field current flows through the ultracap. This reduces the acceleration of the generator and increases its critical clearing time (CCT).

Therefore, the field voltage is reinforced by the addition of the ultracap voltage to the output of the static exciter. The EB can be controlled through either an on–off or a modulated control scheme [2]. On one hand, under the on–off control scheme, the IGBT connects the ultracap during a finite timespan, so the whole ultracap voltage is applied. On the other hand, under a modulated control scheme, a variable voltage is applied due to commutation of the IGBT at a certain frequency and duty ratio. This feature opens the opportunity to develop more sophisticated controls.

2.2. WACS EB control

Fig. 2 shows the block diagram of the field-voltage controllers in a generator, including the proposed WACS EB control and the EB itself. The EB output is modeled as a supplementary voltage, V_{EB}, that is added to the static exciter output to produce the field voltage E_{FD}. V_{EB} is obtained from the modulation of the ultracap voltage, V_{CAP}. The WACS control that produces the modulation signal is described in Section 3. V_{CAP} is computed using an ideal capacitor model, which is the integration of the ultracap current, I_{CAP}, divided by the capacitance C. The ultracap current is obtained from the product between the field current, I_{FD}, and the modulation signal. A limiter with U_{emax} and U_{emin} has been set in E_{FD} to model the rotor insulation protection. This value is equal to 15 pu in the non-reciprocal per unit system. The ultracap ratings in the non reciprocal per unit system are a capacitance of 1 s and a voltage of 9 pu. The description of the sizing method can be consulted in Ref. [11].

3. WACS design for EB control

3.1. Control proposal & design

The impact of the EB is measured in this paper through two cases: in the first one the network has no EB, whereas in the second one, every generator is equipped with an EB that can be operated under different control schemes.

A basic scheme of the EB control that elaborates the modulation signal is shown in Fig. 2. The controller receives as input voltage phasors from PMUs situated at different bus locations of the grid and the voltage phase angles are extracted. The voltage phases are confined between ±p, so they need to be unwrapped. After that, they are smoothed using a digital Bessel filter. Then the filtered phases are processed by a discrete derivative function, subjected to a dead band to limit the action of the controller for small disturbances, and multiplied by a constant gain. Finally, a saturation block is used to limit the values of the modulation signal between 0 and 1. This modulation signal multiplies the ultracap voltage output. However, when interfacing with an actual (hardware) EB, this signal would be used in the power electronic stage to obtain a modulated voltage output.

The discrete derivative is defined by two parameters, a filtering time constant and a gain. The filtering time constant is equal to the reporting rate, 20 ms, whereas the gain is obtained using a heuristic computation approach. Firstly, the gain range is limited to those values that produce an output between 0.1 and 3 times (some saturation is allowed) the EB voltage after a critical fault. After that, the gain value that maximizes the critical clearing time for that fault is chosen. Finally, the gain value is tested for other relevant faults in the system. If the critical clearing time for those faults exceeds the clearing time of first zone (120 ms) the design of the gain is finished, otherwise the process is repeated.

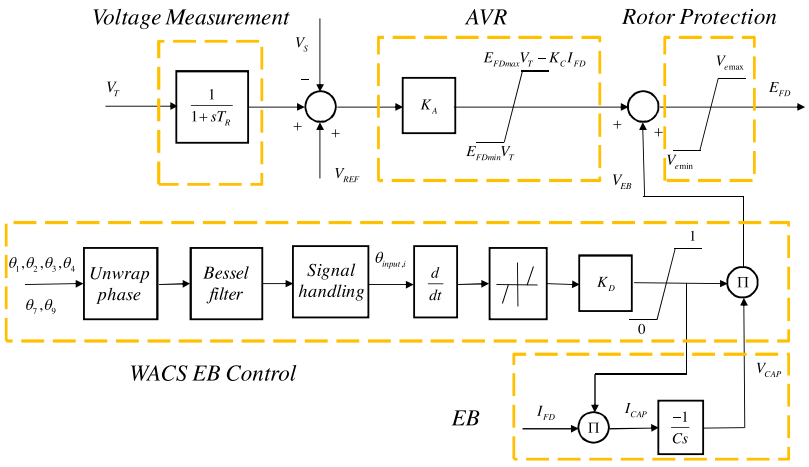

Fig. 2. AVR, EB and WACS control.

3.2. Controller input signals

The three different variants of the signal handling block from Fig. 2 are described:

3.2.1. Input signal using the Pseudo Center of Inertia (PCOI) concept

Lyapunov theory can be used to deduce control laws to improve transient stability. Precisely, Ref. [12] has demonstrated that signals proportional to the speed deviation with respect the COI can actually improve the transient stability of a system. The additional term in Eq. (1) contributes to increase the negativity of the Lyapunov function derivative:

$$\Delta E_i = K_D\,(\omega_i - \omega_{COI}) \tag{1}$$

As generator speed measurements are not commonly available in most commercial PMUs, in this work, the speed is approached by the nodal frequencies at the generator terminals:

$$\Delta E_i = K_D\,(f_i - f_{COI}) = K_D\left(\dot{\theta}_i - \dot{\theta}_{COI}\right) \tag{2}$$

Eq. (2) can be regarded as a proportional derivative controller with the voltage phase of the system generators as inputs.

In practice, the COI approach is not suitable for an actual hardware device. The "true" COI center is calculated by multiplying the phase of each generator by its inertia and dividing the sum of those products by the sum of the inertias. Not only generator inertia parameters are uncertain, but having to monitor changes in active generators make a COI-based controller unnecessarily complex and unreliable. Given the available measurements from PMUs, the most sensible and practical approach is to synthesize a control input signal that utilizes the real-time data from multiple PMUs and a controller that is blind to the inertias of the system, as proposed next. This approach estimates the phase deviation of each generator with respect a Pseudo COI (PCOI) according to Eq. (3)

$$\theta_{input,i} = \theta_i - \frac{\sum_{j=1}^{N}\theta_j}{N} \tag{3}$$

where θ represents the voltage phase, i denotes the generator where the signal is applied and j indicates each generator in the system. The underlying idea is to apply a voltage proportional to the angular deviation of each generator with respect the PCOI. Therefore, only generators whose speed is larger than the PCOI are affected. Note that a different input signal is introduced into each EB controller.

3.2.2. Input signals based in the Dominant Interarea Path (DIP) theory

According to the 10th chapter from Ref. [13], different signals can be elaborated after analyzing the Dominant Interarea Paths of a given system. These signals will have the highest observability of the interarea oscillation mode, which is responsible for the loss of synchronism. Moreover, local oscillation modes can be averaged out when the designing the signals following this approach. Consider the test system in Fig. 3, which will be used for testing in the next section. Eq. (4) shows the input signals to the EB controls from generators of areas 1 and 2, when phases θ_7 and θ_9 are used (2 PMUs). The EB control using this signal will be referred to as DIP2.[1]

$$\theta_{input,AR1} = \frac{\theta_7 - \theta_9}{2} \quad \theta_{input,AR2} = -\frac{\theta_7 - \theta_9}{2} \tag{4}$$

The equivalent signal for areas 1 and 2 if phases $\theta_1, \theta_2, \theta_3$ and θ_4 (4 PMUs) are used as shown in Eq. (5). The EB controller using this signal will be called DIP4, and the signals are given by:

$$\theta_{input,AR1} = \frac{\theta_1 + \theta_2}{2} - \frac{\theta_3 + \theta_4}{2} \quad \theta_{input,AR2} = -\frac{\theta_1 + \theta_2}{2} + \frac{\theta_3 + \theta_4}{2} \tag{5}$$

4. Experimental testing and implementation

4.1. Test system

The EB WACS control is tested in the well known Klein–Rogers–Kundur system [14] of Fig. 3. The Klein–Rogers–Kundur system modeled in Simulink SimPowerSystems [15], has been modified to execute in the OPAL-RT simulator. The model has been discretized with a step size of 25 μs. A total of 240 MW have been removed from the loads and connected to the generator terminals, while keeping the 400 MW power flow from area 1 to area 2. Thus, a 60 MW load has been connected to each generator. A further modification has been done to reduce the high CCTs that result from applying a solid three phase short circuit in any of the buses. This modification consists of reducing the inertias of generators of area 1 from 6 to 3 s. The generators are driven through a single mass turbine and governor [15], whereas the PSS (V_s input) and the static exciter AVR have been taken from Ref. [14]. The latter is displayed in Fig. 2.

The Klein–Rogers–Kundur system has been chosen as it is helpful to show the advantages of global measurements over

[1] This signal can be obtained as well applying Eq. (3) from PCOI to phases θ_7 and θ_9.

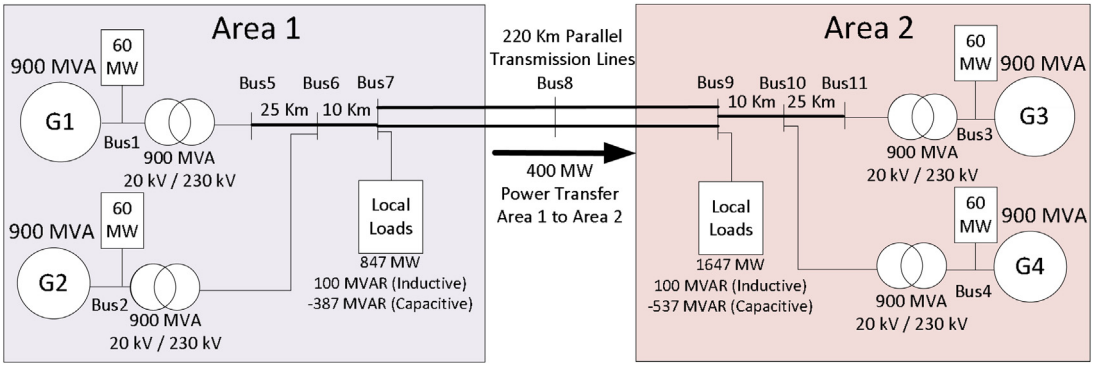

Fig. 3. Two-area test system.

Table 1
CCTs after a fault at bus 8 cleared by opening of one of the double lines 7-8 for different locations of the EB.

EBs	No	Area 1	Area 2	Areas 1 & 2
CCT (ms)	210	340	170	270

local measurements. Theoretically, boosting the excitation of synchronous generator during a fault should improve the stability of the system. However, Ref. [10] showed for this system that not every excitation should be boosted for every fault, provided that in some cases the stability was hindered. Ref. [10] proposed to use global measurements to decide which excitations should be boosted.

This fact was confirmed in this study by means of placing the EB at different locations (area 1, area 2, areas 1 and 2) and comparing their CCT to the case without EB. The on–off control based on generator terminal voltage level (local measurements) was tuned to force the activation of the EB for every fault in the grid. Simulations showed that depending on the location of the active EBs the stability was improved or deteriorated. i.e: Table 1 shows the CCT of a fault in bus 8 cleared by opening of one of the double lines 7–8, when the EBs under on–off control are placed at various locations in the system. The CCT was increased when EBs from area 1 were activated, it was decreased when EBs from area 2 were activated and laid in between when every EB in the grid was activated.

4.2. Test facility and experimental setup for this work

Experimental implementation and testing of the EB controls have been carried out at SmarTS Lab [16], which is a laboratory for Wide Area Monitoring Protection And Control (WAMPAC) application development. Fig. 4 shows an overview of the facility with the main components used for this work indicated with red dashed rectangles. The OPAL-RT simulator [17] is no. 1, PDC [18] is no. 2, NI cRIO 9074 [19] is no. 3, oscilloscope is no. 4, amplifiers are no. 5 and PMUs within SEL-421 protection relays [20] are no. 6.

4.3. Controller prototype architecture

Fig. 5 displays the architecture of the Hardware-in-the-Loop (HIL) prototype. The power system and the EB control are simulated in the RT Simulator (RTS). However, functions of PMUs, PDC, communication network and digital to analogue synchrophasor data processing are carried out through actual hardware. The striped blocks indicate variable time delay, whereas the white blocks indicate deterministic time delay.

The OPAL-RT simulates the power system and its controls in RT with a time step size of 25 μs. Depending on the chosen EB control, either the three phase voltages of buses 1–4 or the three phase

Fig. 4. SmarTS lab experimental laboratory setup. (For interpretation of the references to color in the text, the reader is referred to the web version of this article.)

voltages of buses 7 and 9 are placed in its analogue outputs (max. ±16 V) through Digital to Analogue Converters (DAC).

These voltage signals are wired to the pair of PMUs that are integrated in SEL-421 relays. PMUs' low voltage test inputs (±5 V) can be used to avoid the usage of amplifiers. This choice avoids the inherited bias and delay of the single phase amplifiers. PMUs produce phasors (amplitude and phase) at a rate of 50 messages per second from those bus voltages according to IEEE Std C37.118.2-2011 [21], and transmit them through the TCP Ethernet network to the PDC according to IEEE Std C37.244.2013 [22].

The PDC aligns the phasors according to their time stamps and streams the data packages through the TCP Ethernet network to the workstation and then to the NI cRIO 9074 analogue outputs through the NI cRIO 9074 FPGA. The PDC has a waiting period of 150 ms to obtain messages from every PMU.

A workstation is equipped with the S^3DK [23] that unwraps the PDC data stream and provides it to the user in the LabView environment. This usable data is redirected to a NI cRIO 9074 through the Ethernet, it is processed through a real-time processor and an

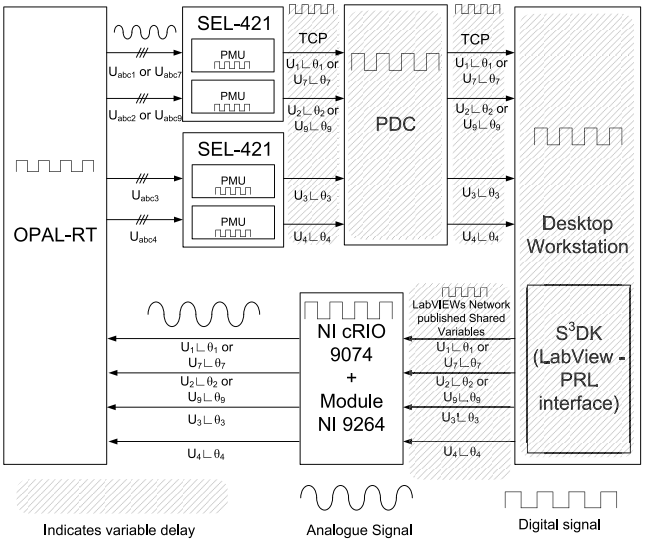

Fig. 5. HIL prototype architecture.

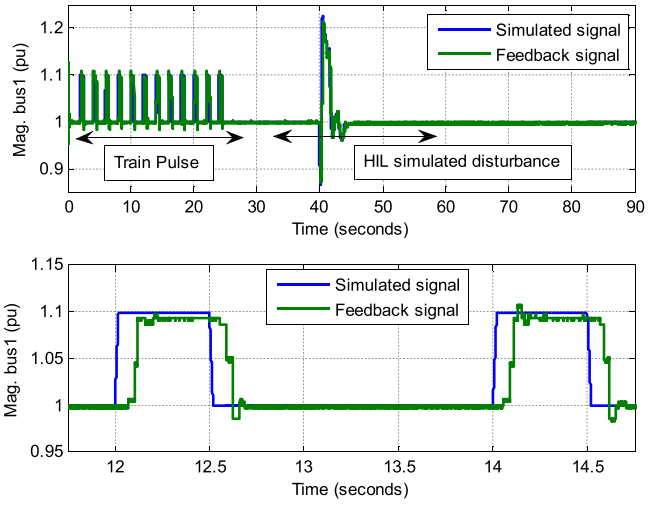

Fig. 6. Comparison between the simulated generator bus voltage and the feedback PMU signals measured and sampled by the RTS to calculate the average delay.

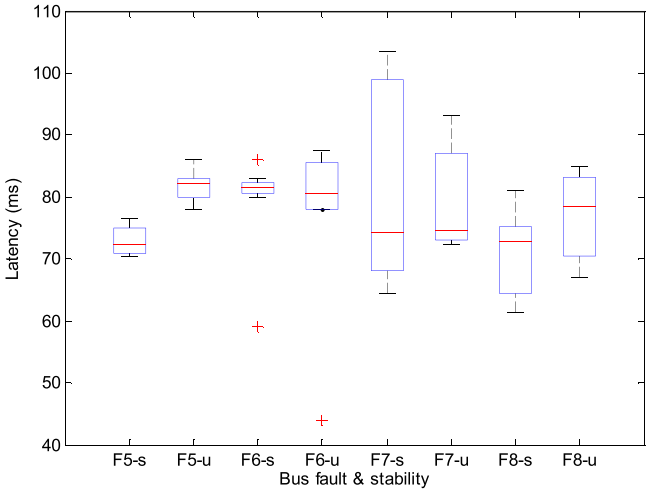

Fig. 7. Time delay box plot for critically stable and unstable RT-HIL experiments simulating faults at different buses (with EB PCOI4). This figure summarizes the results of 8 HIL experiments. The outliers from F6-s and F6-u are due to digital noise and have not been considered for the estimation of the delay median.

FPGA to be provided to a Digital to Analogue Converter (DAC). The DAC provides the analogue phasor signals (amplitude and phase) back to the OPAL-RT Analogue to Digital Converter (ADC) inputs (max ±16 V). These phasor signals are used by the RTS to calculate the latency, using the modules and to provide inputs to the EB controllers.

4.4. Constraints & design choices

The constraints shown in Table 2 are relevant considering similar design choices that can be found in a similar WACS industrial implementation [4] and the WACS prototype in [3].

4.4.1. EB control implementation

Previous work studied the use of speed signals for EB control [2]. However, given that PMUs generally do not measure the generator's speed unless additional equipment is placed in the plant [24]; and such types of PMUs are generally unavailable in most power systems with the notable exception of China [5]; a more realistic design requires the use of phasor quantities. Hence, adopting a sensible, realistic and practical approach, voltage phase inputs were used for the prototype implementation. The implementation of the EB control on the cRIO FPGA was initially foreseen as in the work in Ref. [3]. However, due to hardware limitations and due to the fact that FPGA coding is a time consuming and cumbersome task, a trade-off between implementation time and complexity had to be made. The EB control is implemented in the RTS, whereas the S^{3}DK library which handles the PDC data is executed in a workstation and the D/A in the cRIO FPGA.

The advantage of this option is that a rapid validation of the concept is achieved. Good engineering practice [25] states that a proof prototype should be developed from lesser complexity to higher complexity. If the basic prototypes do not meet the expectations, it is not worthy to invest more resources in building a more complex one. Therefore, the proof of concept prototype was built as explained next.

The implementation consists of processing the PDC data in a workstation and performing D/A in a cRIO 9074 FPGA, whereas simulating the EB and its control in the OPAL-RT. The workstation streams the phasor data from the S^{3}DK to the cRIO using shared variables [23]. Then, the cRIO delivers these raw measurements to the voltage module NI 9264 using the FPGA to interface with the D/A stage. Finally, the NI 9264 voltage module generates the analogue signals, which are wired to the OPAL-RT analogue inputs. The EB control is modeled and run in a core of the RTS at 20 ms instead of 25 μs, to emulate the sampling rate of the input PMU data and to minimize potential numerical issues when interfacing with the RTS.

4.4.2. Measurement and communications latency delay

Communication latency [26] is a key factor affecting WACS applications. The longer the latency, the worse the performance of a WACS [27,28]. Therefore, it was necessary to determine it in every test. The procedure is described using Fig. 6, at the beginning of the test a pulse train with period of 2 s and half a second duty ratio is injected in the voltage analogue signals that are sent to the PMUs. Note that this disturbance is not introduced in the network, so the system is not disrupted. The pulse train travels through the closed loop system and is injected back in the RTS analogue outputs. Then, both signals are compared and the average of the delay of the 12 pulses is computed.

Fig. 7 shows the statistical distribution of the delays for 8 HIL experiments that constitute the marginally stable and unstable responses for faults at different bus locations. For each HIL exper-

Table 2
List of constraints and design choices.

Constraint	Source	Design choice
Time consuming and cumbersome control implementation in FPGA	Hardware & Software	1) EB control implementation in RTS at 20 ms
Unknown closed loop latency	Hardware & Software	2) Estimate the closed loop time latency in every test using experimental measurement data
Need to transmit the PDC data to be used by a controller	Hardware & Software	3) Transfer PDC data using a mediator that can be interfaced with hardware into analogue signals through sample and hold
Voltage phase data wrapped between ±180°	Software	4) Unwrapping algorithm
Derivative computations are sensitive to noise	Software	5) Use of a digital Bessel Filter

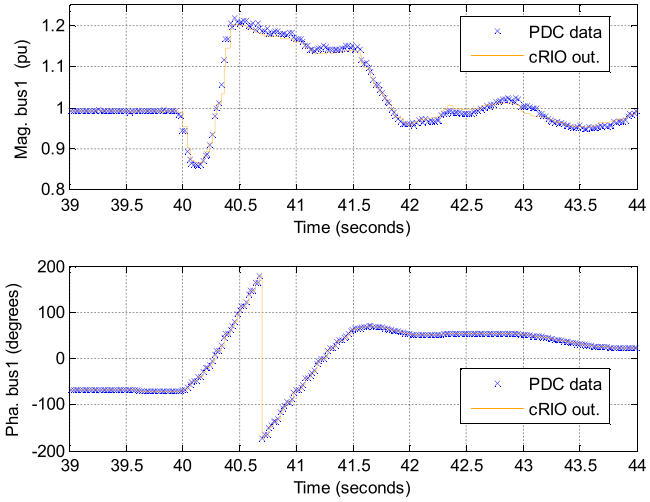

Fig. 8. PDC data and analogue output of the cRIO.

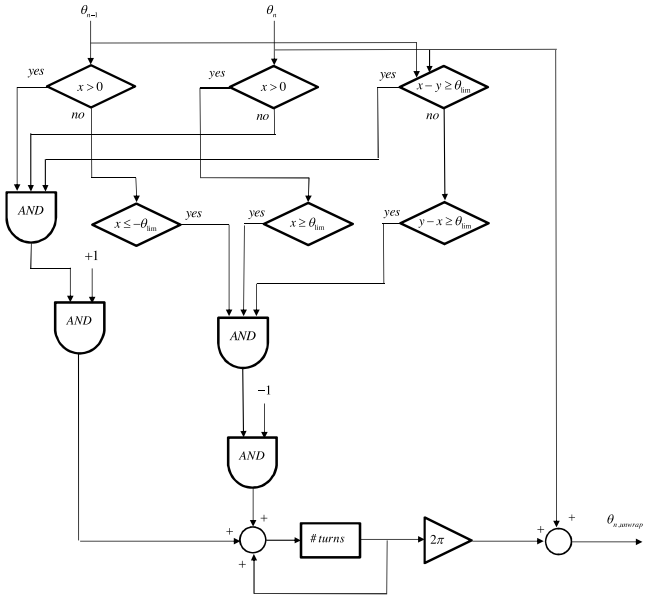

Fig. 9. On line phase unwrapping algorithm.

iment 12 individual delay estimates are calculated. The median of the delays in each case varies from 72 ms to 82 ms. The variance changes randomly from one test to another due to the uncertainty of delay at different parts of the WACS. These communication delays are of the same order as a state of the art WACS industrial application relying on dedicated fiber communications [27,28].

4.4.3. DAC processing of synchrophasor signals

Both, the PDC and the EB control are digital and operate at a rate of 20 ms. In a final field deployment, the EB control would be integrated together with a similar real-time data mediator to the S^{3}DK library and deployed in a single piece of hardware to receive directly the PDC data. However, in this prototype implementation each software was deployed in different hardware. Once the PDC data was received in a workstation, the S^{3}DK provides all phasor data available to the the cRIO via shared network variables [23]. From those signals, the ones to be used are chosen, processed and forwarded to the cRIO analogue module through the FPGA.

An analogue output signal is generated by the cRIO analogue module by applying a sample and hold to the received PDC data. This method is useful to cope with lost data too. The signal is hard-wired to the OPAL-RT analogue input, which samples it at a rate of 25 μs. However, as the simulated EB control samples the input at 20 ms, a rate transition has been placed in the middle to resample it again and avoid numerical issues.

In Fig. 8 variable delays can be appreciated between the PDC data and the analogue output signal of the cRIO. Both figures present the voltage phasor measured at the bus 1 when a solid three phase fault is applied at bus 8; every generator is equipped with an EB under the DIP control scheme.

4.4.4. Phase unwrapping algorithm

The phasor phase is delivered wrapped between ±π by the PDC. This fact is particularly useful when transmitting the data as resolution is maximized even if the phases are continuously increasing (or decreasing). However, they need to be unwrapped before being used as an input to any kind of control because abrupt changes in a controller's input can lead to erroneous outputs.

The algorithm from Fig. 9 has been developed and implemented to unwrap the phasor phase angle. This algorithm compares the value of the current phase θ_n to the previous θ_{n-1} and detects abrupt changes in both directions, from positive to negative (angle increasing) and from negative to positive (angle decreasing). The former is usually related to a transient stability disturbance, while the latter is related to a drift of the angle with respect the GPS Ref. [29] . In addition, this algorithm takes into account the sign of the departure angle, as it is referenced to a GPS signal and it can appear anywhere between ±π. A limiter, δ_{lim}, has been set to $5\pi/6$ to guard the algorithm from data gaps. The unwrapping algorithm has been implemented in the RTS.

Fig. 10 shows the output of the algorithm during a test when a solid three phase short circuit is applied at bus 8 at t = 40 s. For the sake of illustration the algorithm is disabled at the beginning of the

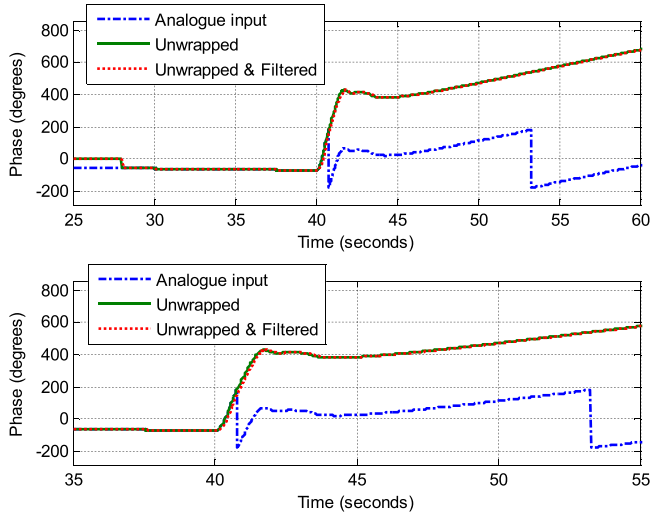

Fig. 10. Unwrapping and filtering.

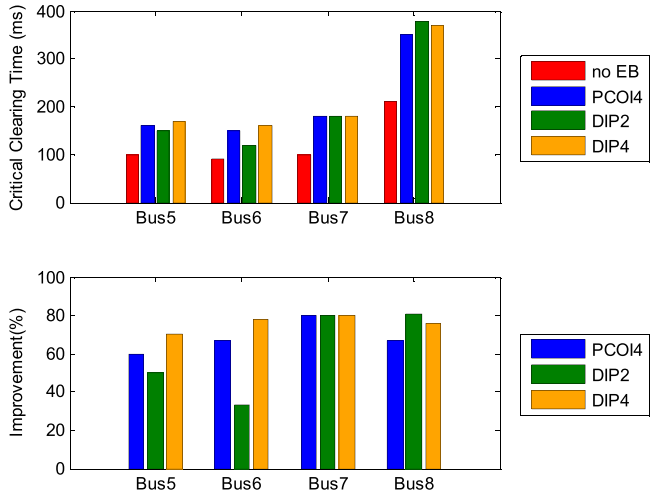

Fig. 11. CCTs achieved when adding EBs under different control schemes. A total of 28 HIL experiments are shown.

experiment until the t = 28 s, when the algorithm is enabled (not shown in the figure).

4.4.5. Phase filtering

A 3rd order Bessel digital low pass filter, as shown in Fig. 2, is used to minimize noise amplifying effects from derivative computations. The Bessel filter has a cut-off frequency of 5 Hz to remove noise and transients that are not related to rotor angle stability. The sampling period of the filter is 20 ms. The filter is given by Eq. (6), where $K = 31006$, $a = 29.58$, $\alpha = 46.85$ and $\beta = 1048$.

$$F_{Bessel} = \frac{K}{(s+a)\cdot\left(s^2+\alpha s+\beta\right)} \tag{6}$$

5. Experimental results and analysis

In this section HIL experiments are used to evaluate the proposed WACS by analyzing two performance metrics: CCT performance and control global performance.

5.1. Critical clearing time (CCT) performance

In Fig. 11 a total of 28 HIL experiments are summarized. It shows the CCTs obtained after applying faults at different bus locations, without EB and when every generator is equipped with an EB under different control inputs. Furthermore, it displays the controller CCT improvement (i.e. the increased time margin in % due to EB controller) in percentage for the different EB controls. Faults at buses 5–8 are displayed. The fault at bus 8 is cleared by opening of one of the double lines between buses 8 and 9. Faults at buses 9–11 are not shown because their CCTs exceed 400 ms without EB. Such long CCTs do not need any additional improvement.

Globally the highest improvements and CCTs correspond to the DIP4, followed by the PCOI4 and the DIP2 EB controls. Improvements for both, DIP4 and PCOI4 are between 60 and 80%, whereas for DIP2 they are between 30 and 80%. The performance of the DIP2 control is compromised for faults occurring close to its PMUs (bus 7) compared to the other controls.

5.2. Global performance

The WACS EB global performance is evaluated through the inspection of speed-angle charts. According to transient energy functions theory [30] the area covered by such trajectory is proportional to the transient energy increase in a generator after a fault. The ability of the system to dissipate that energy is connected to the system's stability. Fig. 13 compares generator trajectories without EB and with a DIP4 EB control after a fault at bus 8 is cleared by opening of one of the double lines between buses 8 and 9. Three trajectories are displayed:

- Trajectory without EB WACS for its CCT (210 ms).
- Trajectory with EB under DIP4 control (210 ms).
- Trajectory with EB under DIP4 for its CCT (370 ms).

Comparing the areas covered by the trajectories of the generators with and without EB WACS for a fault clearing of 210 ms (blue and red traces), it can be observed that the area is smaller with a controller. This means that the energy increase of the system is smaller for a given clearing time if every generator is equipped with an EB WACS. Moreover, if the areas with and without EB for their respective CCTs (370 and 210 ms respectively, magenta and red traces) are noticed, it can be observed that the area with EB is much larger. This indicates that, the system is able to cope with much more transient energy if the generators are equipped with EB WACS. Furthermore, the system is able to dissipate more transient energy with EB WACS than without it and therefore allows the system to withstand longer faults.

Fig. 13 displays the area enclosed by the trajectories of each generator under different control schemes for the same fault as in Fig. 12. The responses of the controls to a fault clearing of 210 ms and with respect to their own CCT are compared.

The following important facts are observed:

(A) The area covered by the trajectories of the EB WACS for the clearing time of the system with no EB WACS (no EB-210) is smaller for controls PCOI4-210 ms and DIP2-210 ms. Hence, with the exception of EB WACS DIP4-210 ms, the transient energy at a clearing time of 210 ms is substantially less than with no EB. This helps to understand why the CCT for the system is increased using EB WACS.

(B) Fig. 13 shows that the area covered by each EB WACS for their respective CCTs (350, 370 and 380 ms) is significantly greater than without EB WACS. Although the improvements of the three controls are quite similar, Fig. 13 can help to understand better the difference between the three controls. DIP2 exhibits

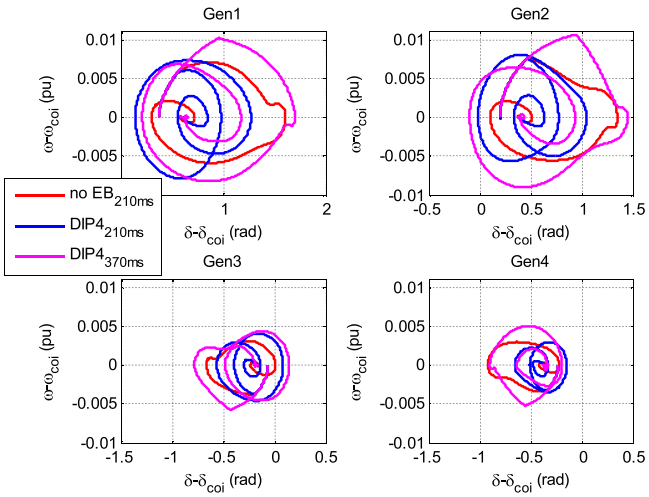

Fig. 12. Speed-angle chart without (210 ms) and with EB DIP4 (210 ms & 370 ms) after a solid three phase fault at bus 8.

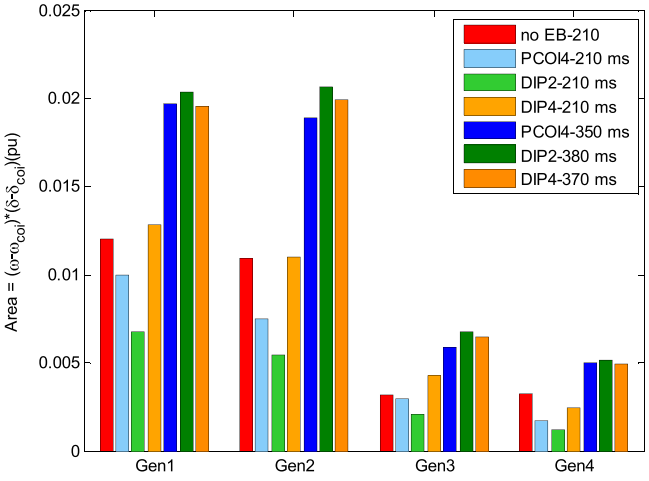

Fig. 13. Comparison of the area enclosed by generator trajectories after a solid three phase fault at bus 8 for different EB control strategies for their respective CCTs. (For interpretation of the references to color in the text, the reader is referred to the web version of this article.)

the highest CCT for a fault in bus 8. It can be verified that DIP2 minimizes the area for a fault clearing of 210 ms and maximizes it for its own CCT. Therefore, the system is able to dissipate more energy with a DIP2 EB control. DIP4 displays both, the second highest CCT and second largest area. PCOI4 control has the smallest area for its own CCT and the smallest improvement. However, for a fault of 210 ms, PCOI4 is the second control that better distributes the transient energy after the fault, provided that its area is the second smallest one.

Fig. 14 displays the input signal to the DIP4 controller, together with its derivative and the supplementary field voltage generated by the EB under this control scheme for the same disturbance as in Figs. 12 and 13. It can be seen that the EB WACS that are active are the ones whose derivative is greater than zero. The alternating behavior is explained by the oscillations of the angle.

6. Conclusions

The presented EB WACS prototype controller modulates the voltage of its ultracap according to the derivative of an input signal

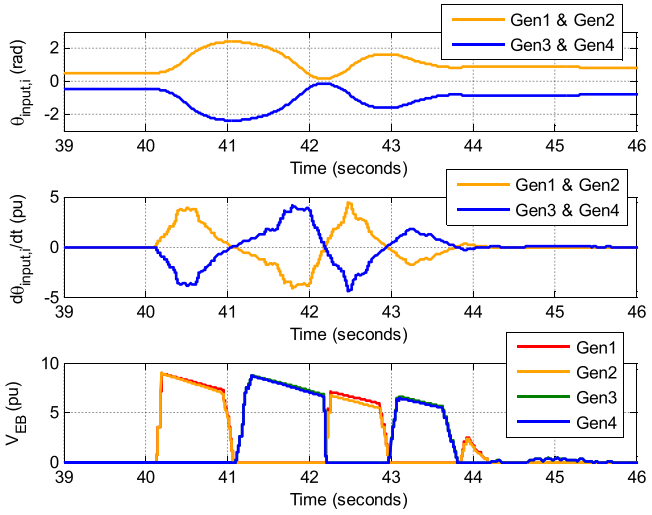

Fig. 14. Input signal, control signal and supplementary field voltage (with EB DIP4 370 ms) after a solid three phase fault at bus 8.

built from a combination of voltage phase angles obtained by PMUs at different buses in the system.

Data handling and transfer is a major challenge in WACS applications. Developing a real hardware prototype requires careful consideration of signal treatment, data exchange and variable communication delays that have been considered in this paper.

Three different PMU-based input signals were tested: PCOI4 (a signal based in the Pseudo Center of Inertia that uses the 4 generator bus voltage phases), DIP2 (a signal based in the Dominant Interarea Path that uses the bus voltage phases from the two endings of a long interconnection line) and DIP4 (that is based in the same principle but using the voltage phases from the 4 generator bus voltage phase angles).

By carrying out a total of 196 HIL experiments this paper shows that CCTs improvements between 30% and 60% are feasible and therefore the system is stable above clearing times of the 1st and 2nd zones (depending on the fault). Although the contributions of the three control strategies are of the same order, the DIP based signals offer slightly higher increases. Solutions with more PMUs (PCOI4 and DIP4) are more robust against faults occurring close to the measurement points than those with less (DIP2). This was observed for faults in bus 7.

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