RT-HIL Implementation of the Hybrid Synchrophasor and GOOSE-Based Passive Islanding Schemes

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***Abstract*—Real-time hardware-in-the-loop performance assessment of three different passive islanding detection methods for local and wide-area synchrophasor measurements is carried out in this paper. Islanding detection algorithms are deployed within the phasor measurement unit (PMU) using logic equations. Tripping decisions are based on local and wide-area synchrophasors as computed by the PMU, and trips are generated using IEC 61850-8-1 generic object-oriented substation event messages. The performance assessment compares these islanding detection schemes for the nondetection zone and operation speed under different operating conditions. The testbench that is demonstrated is useful for a myriad of applications where simulation exercises in power system computer-aided design software provide no realistic insight into the practical design and implementation challenges. Finally, different communication latencies introduced due to the utilization of synchrophasors and IEC 61850-8-1 GOOSE messages are determined.**

***Index Terms*—Phasor measurement unit (PMU), power system islanding, protection relays, real-time hardware-in-the-loop simulation (RT-HIL), synchrophasors.**

I. Introduction

ISLANDING is a condition where a part of the power system consisting of both loads and generation becomes isolated from the rest of the power grid, and generators continue to energize the isolated network [1]. Two types of islanding occur in a power system: 1) intentional islanding and 2) unintentional islanding. Intentional islanding is performed for either maintenance or load-shedding purposes to protect the rest of the power grid and avoid a blackout. The isolated generators operate in voltage and frequency control mode to provide constant voltage to local loads in the isolated network while maintaining the isolated grid frequency. Unintentional islanding occurs due to equipment failure or severe faults resulting in the opening of circuit breakers (CBs) that interconnect the island with the rest of the power system. Unintentional islanding may result in hazards in power system operation and may lead to safety risks for maintenance staff. In addition, during unintentional islanding, the isolated network suffers from significant voltage and frequency variations that can damage both loads and generators within the island. Furthermore, autoreclosing of the tie line, which is a standard automated procedure followed in case of temporary faults, results in out-of-phase and unsynchronized reclosing when the system is subject to unintentional islanding.

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A. Paper Motivation

For the particular case of distributed generation (DG), the IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems (IEEE Standard 1547-2008) [2] states that the DG must be disconnected from the isolated grid within 2 s after an unintentional islanding event. This maximum delay of 2 s includes islanding detection, trip signal generation, trip signal transfer, and a breaker opening for the connected DG. It is therefore important to not only have fast islanding detection algorithms, but also to have low-latency trip signal transfer schemes to open the breaker.

Synchrophasors from multiple local and remote measurement locations in the grid may be exploited for islanding detection [3]. A hybrid synchrophasor and IEC 61850-8-1 (GOOSE) [4]-based scheme can provide faster operation times compared to traditional hardwired schemes, as it omits the output circuitry delay, for example, "make or break" the delay of auxiliary signaling relays which is typically 8–10 ms [5]. Even with digital protection relays having optoisolated digital in input/outputs (I/Os), the utilization of the GOOSE message results in a tripping time that is 3–6 ms faster than the hardwired digital I/O-based trippings [6].

B. Literature Review

It has been reported in [7] that synchrophasors-based islanding detection schemes can provide fast, reliable, and accurate detection of islanding conditions under different power system operating conditions. However, these studies were based on offline simulations, and actual data from real hardware PMUs were not used for performance analysis of the proposed islanding detection algorithms. Thus, the communication latencies introduced due to the utilization of synchrophasor measurements were not taken into account. In [8], wide-area synchrophasor measurements are utilized to continuously monitor the phase of generators to determine synchronism within the generators, and loss of synchronism is interpreted as a loss-of-mains scenario. This algorithm was tested using archived synchrophasor measurements from the power grid, and the prototype was deployed in Labview on a non-real-time operating system (RTOS). The different communication latencies associated with this algorithm were not taken into account. In [9], a synchrophasor-based islanding detection

scheme is implemented as an add-on feature in a software version of a phasor data concentrator (PDC). PDC software is typically installed on servers with Windows OS which is not a real-time operating system (RTOS). The software PDCs cannot be time synchronized with sufficient accuracy in such an environment and, therefore, PDC processing delay cannot be thoroughly evaluated. The processing time of the PDC is dependent on its configured waiting time, which refers to the maximum amount of time to wait for all inputs to be received, time-aligned, and concentrated in a specific output stream. This waiting period is generally 100–200 ms (depending upon the geographical location of the PMUs). This adds extra delay to the overall operating time of a synchrophasor-based islanding detection scheme and, thus, may violate the anti-islanding criteria specified in IEEE Standard 1547-2008 [2]. In order to accurately identify the communication delays incurred by the PDCs, a hard RTOS for PDCs is essential. In addition, current PDCs have been designed for wide-area monitoring purposes and, therefore, they face challenges to meet real-time requirements for time-critical applications (e.g., protection).

C. Paper Contribution

This paper presents the implementation and RT-HIL performance assessment of a hybrid synchrophasor and IEC 61850-8-1 (GOOSE) [4] -based passive islanding detection algorithms utilizing local and wide-area synchrophasors. Real-time-hardware-in-the-loop (RT-HIL) simulation [11], [12], including PMUs from Schweitzer Engineering Laboratories [13], is executed for performance analysis of these schemes. Methods to accurately calculate different latencies associated with synchrophasor-based islanding schemes, such as PMU filtering delay, PMU synchrophasor computation delay, PMU algorithm execution delay, PMU time-alignment delay (for remote measurements), synchrophasor frame formation delay, and GOOSE latencies are also presented.

Different islanding detection algorithms are deployed as simple logic equations within the PMU. This approach is generic, as logic equations are supported by all of the microprocessor-based protection relays. Performance assessment of the proposed algorithms is performed by evaluating the criteria documented in IEEE Standard 1547-2008 [2]. The nondetection zone (NDZ) [14] is evaluated for active and reactive power mismatches, between generation and local load, for all algorithms.

The proposed approach is subjected to minimum possible communication latency and can be used for fast prototyping of any passive islanding detection algorithm that utilizes local or wide-area synchrophasor measurements.

II. Islanding Detection Methodologies

This section gives a brief overview on different islanding detection methods commonly used by utilities.

A. Passive Islanding Detection Methods

These methods are based only on the electrical quantities being monitored. These methods detect an islanding condition when these electrical quantities violate a prespecified threshold.

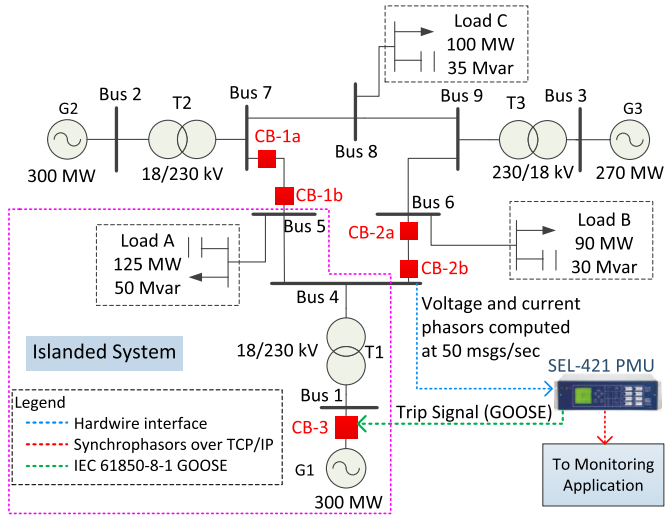

Fig. 1. IEEE 3-machine, 9-bus power system modelled in MATLAB/Simulink. The islanded region is outlined.

Passive islanding detection methods can be implemented in two ways as follows.

- Local-based passive islanding detection: These are based on local measurements at the DG side. However, they have a large NDZ [14], which is defined as the range of power mismatches between the DG supply and local load for which the particular islanding detection method may fail.
- Wide-area passive islanding detection: If the power mismatch between the DG and the local load is negligible, the local-based passive islanding detection methods may fail. Wide area-based passive islanding detection schemes utilize synchrophasors from both DG and utility side to detect an islanding condition [7].

These methods require intense offline simulations to set the threshold limit to accurately identify islanding conditions, as the performance of these schemes depends on the protection relay settings. Too rigorous limits can result in false islanding detection and tripping of the DG in normal operating conditions while too loose settings will result in longer operation time and, therefore, violate the DG disconnection requirement of 2 s as specified by IEEE Standard 1547-2008 [2].

B. Active Islanding Detection Methods

In active islanding detection methods, a small perturbation is introduced in the system deliberately. These methods have a very small NDZ and can detect islanding conditions even if there is a perfect match between DG and local load [15], [16].

Active islanding detection schemes are relatively slow in detecting islands compared to passive islanding methods. This is because they rely on the response of the injected perturbation in the system which takes additional time to detect.

III. Power System Test Case Modeling

A modified IEEE 3-machine 9-bus system [10] is modeled in MATLAB/Simulink for real-time execution and is shown in Fig. 1. The system contains 3 generators, 9 buses, and 3 loads. The system was modified for 50-Hz nominal operating

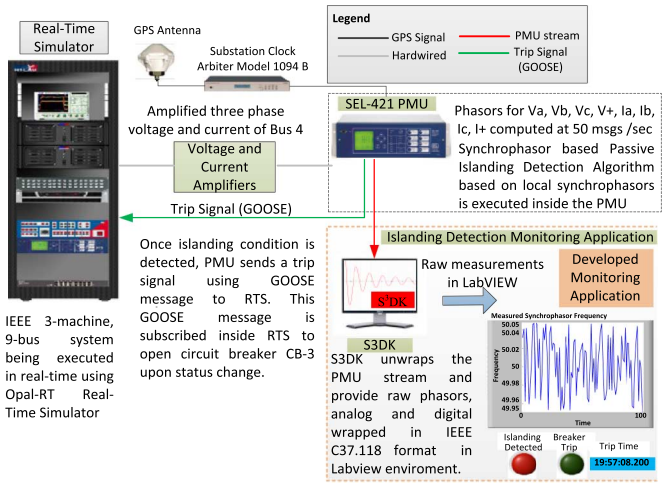

Fig. 2. Experimental setup for performance analysis of synchcrophasor-based islanding detection schemes using local synchrophasors.

frequency and real-time simulation purposes (including detailed three-phase branch/breaker modeling). If CB-1a, CB-1b and CB-2a, CB-2b are opened simultaneously, this results in an islanding condition with G1 supplying power to the Load A at Bus 5. Once the breakers are opened and the island is formed, this condition needs to be detected and the DG (in this case G1) needs to be disconnected from the isolated network within 2 s as specified by IEEE Standard 1547-2008 [2]. A PMU from Schweitzer Engineering Laboratories SEL-421 [13] is interfaced at Bus-4 (the DG side).

IV. Experimental Setup

The RT-HIL experimental setup is shown in Fig. 2 and was configured at SmarTS-Lab [17]. The power system model is executed in real-time using Opal-RT's eMEGAsim real-time simulator (RTS) [11]. The three-phase voltage and currents of Bus-4 are accessed through the analog outputs of the RTS. These low-level analog signals are amplified to a nominal range of 300 V and 1 A using linear amplifiers. Amplified analog voltage and current signals are fed to the PMU which computes phasors for all of the phases and positive sequence for voltage and current that are reported at 50 frames/s.

The synchrophasors are internally utilized by the PMU to execute the islanding detection algorithms deployed using logic equations. These logic equations are discussed in the next section. Once the islanding condition is detected, a trip command is generated by the PMU, and a GOOSE message with changed status is sent to the RTS. This GOOSE message, published by the PMU, has a subscription from the RTS that is configured to open circuit breaker CB-3 in the model. This disconnects the DG (G1) from the isolated network. The performance evaluation of the islanding detection algorithm is carried out by calculating the time difference between the opening of CB-1 and CB-2 to form an island and the tripping of CB-3 caused by the PMU to disconnect G1. The nondetection zone (NDZ) [14] is determined by changing the active and reactive power consumption of Load A to simulate different operating conditions.

The RTS' GOOSE subscription is configured through a GOOSE subscriber. This is achieved through a block that requires a IED Capability Description (ICD) file. A ICD file describes the complete capability of an IED. In order to subscribe to a GOOSE message the Multi-cast address of publication as well as its identifier (AppId) are used to produce control signals corresponding to the GOOSE message received through the IEC 61850 network [4].

In order to monitor the synchrophasors and to analyze the behavior of the islanding detection algorithms, a simple monitoring application was developed in LabView. The PMU was configured to stream out all computed phasors. Important states of the islanding detection algorithm's and the tripping signal were configured as digital output signals within the PMU stream as specified by the IEEE Standard for Synchrophasor data transfer for Power Systems (IEEE Standard C37.118.2-2011) [18]. This PMU stream is received in a workstation using Statnett's Synchrophasor Software Development Kit (S3DK) [19] which provide real-time synchrophasor data in the LabView environment. Within LabView, these raw measurements are presented in real-time displays for monitoring purposes and are stored for further analysis.

V. Implementation of Local Passive Islanding Schemes

This section gives a detail of different passive islanding detection methods implemented in the PMU. Using logic equations, it is possible to deploy a variety of passive islanding detection schemes, such as those presented in Section II-A. However, in this section, only passive islanding detection schemes that are computationally efficient and that use local synchrophasor measurements were implemented. The description of each islanding detection method and its implementation using logic equations is presented.

A. Overvoltage/Undervoltage

When an island is formed, the voltage magnitude at the DG side changes significantly if there is a large variation in the DG power supply and the connected local load. If this voltage magnitude variation persists for a specific period of time (10 cycles), an island condition is detected and a trip signal is generated [20]. The 10-cycle delay that is incorporated in these schemes is to accommodate the instantaneous tripping of the protection function by the corresponding protection relay and the opening time of the breaker. Instantaneous protection operating time varies between 10–40 ms depending upon the type of protection, the fastest being instantaneous overcurrent (10–15 ms), followed by distance protection (15–25 ms) and differential protection (20–40 ms). In addition to this instantaneous protection operation time, the opening time of the 230-kV CB is considered, which is between 3–5 cycles (60–100 ms). As a fair estimate, the timer of 10 cycles (200 ms) is used to accommodate for all these transients in the power system. Fig. 3 shows the logic diagram of this deployed islanding method and its respective logic equation programmed in the PMU.

Once the local voltage phasor magnitude exceeds 1.1 p.u. or goes below 0.9 p.u., a conditioning timer PCT01 is activated. If the voltage violates this threshold for 10 cycles, the output of the timer (PCT01Q) changes its status from 0 to 1. This output is configured to generate the general trip signal. This general trip is also published as a IEC 61850-8-1 GOOSE message.

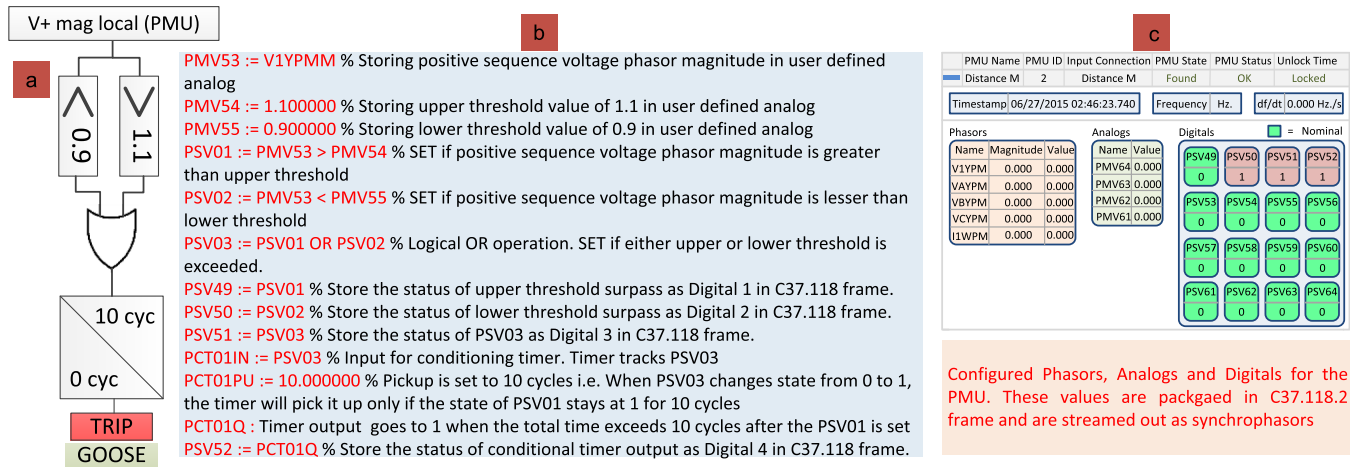

Fig. 3. (a) Logic diagram. (b) Protection logic equations used to deploy the algorithm within the PMU. (c) Synchrophasor frame showing the configured phasors, analogs, and digitals. PSV 49-PSV 52 stores the digital status as configured by the protection logic equations (b).

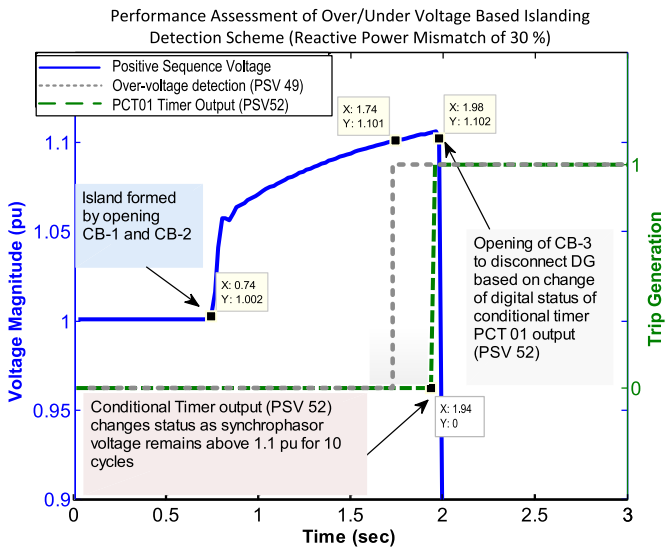

Fig. 4. Overvoltage/undervoltage-based passive islanding detection scheme for 30% reactive power mismatch. The total operating time is 1.24 s.

Fig. 4 shows synchrophasor positive-sequence voltage magnitude computed by the PMU and the response of the overvoltage/under voltage-based islanding detection method when there is a 30% reactive power mismatch between G1 and Load A. At t = 0.74 s, circuit breakers CB-1 and CB-2 open, resulting in an island. The synchrophasor voltage (Fig. 4) starts increasing and at t = 1.74 s, the synchrophasor voltage goes above 1.1 p.u., resulting in the change in status of digital variable PSV 50 and starts the timer PCT 01. Once the timer reaches 10 cycles and the overvoltage condition is sustained, the timer PCT 01 changes the status of its output PSV 52 at t = 1.94 s. This output of the overvoltage timer is published as a GOOSE message that opens the CB CB-3 at t = 1.98 s to disconnect the DG from the isolated island. The total operating time for the anti-islanding scheme is the difference between the time at which the island is formed (i.e., opening time of $CB-1_{a,b}$ and $CB-2_{a,b}$) which, in this case, is t = 0.74 s, and the opening of CB-3 due to the overvoltage condition at t = 1.98 s. Thus, the total operation time for this scheme with 30% reactive power mismatch is 1.24 s.

The NDZ is calculated by fixing the active and reactive power output of generator "G1" and changing the active and reactive power consumption of "Load A." The NDZ for the overvoltage/undervoltage-based islanding detection method is shown in Fig. 5(a). The scheme results in successful islanding detection only if there is significant active power or reactive power mismatch between the DG and the local load in the island. This scheme requires a reactive power mismatch of at least 20% or an active power mismatch of more than 30%.

B. Overfrequency/Underfrequency

The frequency of a power system reflects active power mismatches between generation and consumption. During normal operation, the power system is interconnected and the grid frequency varies within ±0.5–1% (±0.25–0.50 Hz for a 50-Hz system) of the nominal frequency. However, in the case of islanding, the power mismatch between the isolated DG and local load causes the frequency to rise (overfrequency) or drop below (underfrequency) the allowed thresholds. This physical behavior is used to set the trip command that isolates the DG [21]. PMUs estimate frequency deviation and rate-of-change of frequency from the positive-sequence synchrophasor voltage angle. The frequency deviation is calculated as

$$f_k = \frac{(\theta_k - \theta_{k-1})}{\Delta t \times 360} = \frac{(\theta_k - \theta_{k-1})}{\left(\frac{1}{F_s}\right) \times 360} \quad (1)$$

where θ_k and θ_{k-1} are consecutive positive-sequence synchrophasor voltage angles computed at k and $k-1$. Δt is the time difference between the angle calculations. F_s is the synchrophasor reporting rate of the PMU which, in this study, is 50 frames/s.

Fig. 6(a) shows the logic diagram of the over/under synchrophasor frequency-based passive islanding detection algorithm and its respective logic equation programmed in the PMU. The overfrequency threshold was set to 51 Hz and the underfrequency was set to 49 Hz [21]. The NDZ for the overfrequency/underfrequency-based islanding detection method is

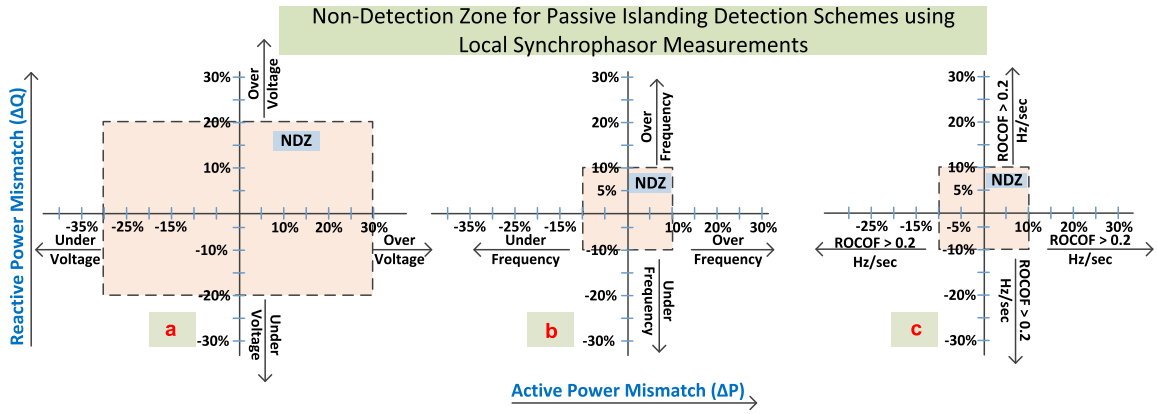

Fig. 5. NDZ for (a) an under/overvoltage-based islanding detection scheme with $V_{min} = 0.9$ p.u., $V_{max} = 1.1$ p.u. (b) Underfrequency/overfrequency-based detection method with $f_{min} = 49$ Hz and $f_{max} = 51$ Hz. (c) ROCOF-based islanding detection scheme with an ROCOF threshold limit set to 0.2 Hz/s.

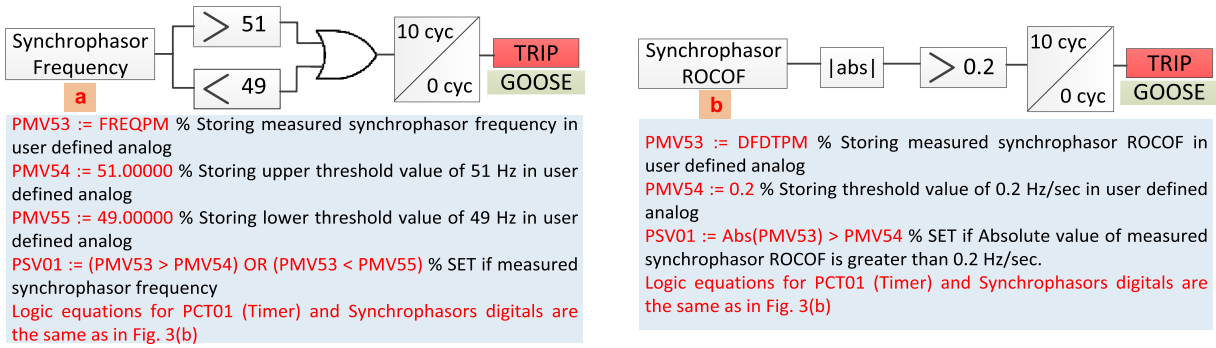

Fig. 6. (a) Logic diagram and protection logic equations used to deploy the overvoltage/undervoltage synchrophasor frequency-based islanding detection algorithm within the PMU. (b) Logic diagram and protection logic equations used to deploy the synchrophasor ROCOF-based islanding detection.

shown in Fig. 5(b). The NDZ is much smaller compared to the overvoltage/undervoltage-based islanding scheme [Fig. 5(a)]. However, it still requires an active or reactive power mismatch of at least 10% to accurately detect the islanding condition.

C. Rate of Change of Frequency (ROCOF)

The rate-of-change-of-frequency (ROCOF) method is frequently used to deploy loss-of-main (LOM) detection because of its simplicity and cost effectiveness compared to other methods [22]. When the island is formed, the active power imbalance between the DG and the local load results in a dynamic change in frequency.

PMUs are capable of calculating ROCOF and it is streamed out in the synchrophasor frame according to IEEE Standard C37.118.2-2011 [18]. PMUs calculate the ROCOF by computing the time derivative of the difference in consecutive frequency estimations according to the following equation:

$$\text{ROCOF} = \frac{df}{dt} = \frac{f_k - f_{k-1}}{\left(\frac{1}{F_s}\right)} \tag{2}$$

where f_k and f_{k-1} are consecutive frequencies estimated by the PMU at time k and $k-1$. F_s is the synchrophasor reporting rate of the PMU which, in this study, is 50 frames/s.

ROCOF can be readily used to implement islanding detection. In this study, the implementation of the ROCOF threshold limit is set to 0.2 Hz/s to account for islanding. The logic diagram and the respective logic equations for the synchrophasor ROCOF-based islanding detection algorithm are shown in Fig. 6(b).

The NDZ for the ROCOF-based islanding detection method is shown in Fig. 5(c). The NDZ is similar to that of the overfrequency/under frequency-based islanding scheme [Fig. 5(b)]. However, it still requires active or reactive power mismatch of at least 10% to accurately detect the islanding condition.

VI. RT-HIL Simulation Results for Local Passive Islanding Schemes

Passive islanding detection schemes exploiting local synchrophasors are computationally efficient and cost effective. Trip decisions depend on these local measurements and, therefore, communication delays associated with remote measurements have a minimum impact on their performance.

The comparison of the operation time of the implemented schemes for different active power and reactive power mismatch is shown in Figs. 7 and 8, respectively. These operation times include the islanding detection algorithm processing time, PMU phasor computation time, GOOSE message communication delay, and CB opening time. The overvoltage/undervoltage-based islanding detection scheme shows faster operation time with an increase in active and reactive power mismatch. Reactive power mismatch shows faster operation time compared to active power mismatch for voltage-based islanding detection schemes.

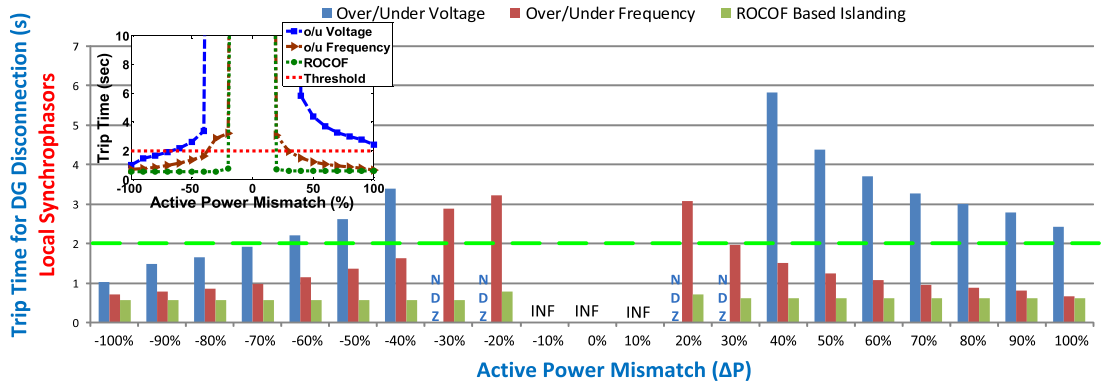

Fig. 7. Comparison of operation time of passive islanding detection schemes (local synchrophasors) when there is active power mismatch.

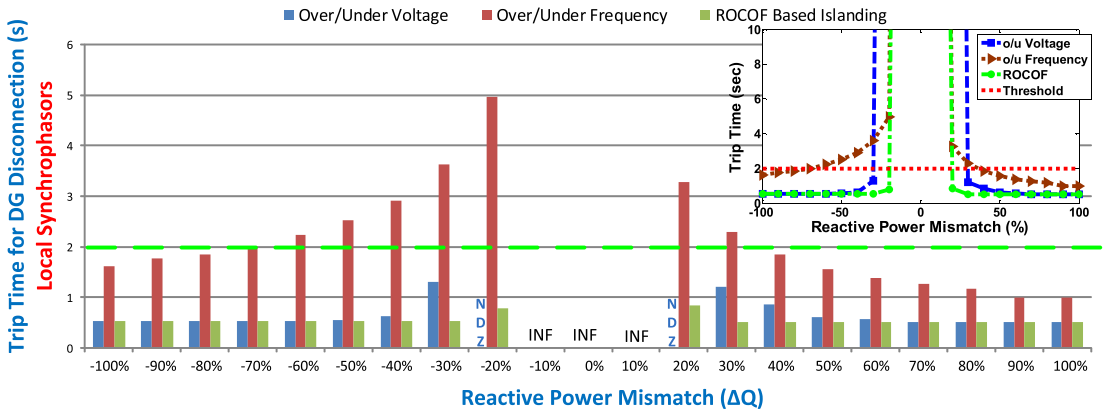

Fig. 8. Comparison of operation time of passive islanding detection schemes (local synchrophasors) when there is reactive power mismatch.

By taking into consideration all of the PMU processing delays and communication delays in the transmission of the GOOSE message, it can be noted that overvoltage/undervoltage-based islanding detection schemes fulfil the requirement of 2 s for DG disconnection if the reactive power mismatch between DG and local load is larger than 20% (Fig. 8).

Overfrequency/underfrequency-based islanding detection methods have a wider islanding detection zone [Fig. 5(b)]. However, acceptable operation requires an active power mismatch between the DG and the local load larger than 30% (Fig. 7). Overfrequency/underfrequency-based islanding detection schemes perform very slowly if there is only a reactive power mismatch (Fig. 8). ROCOF-based islanding detection schemes are highly reliable if the power mismatch between the DG and local load is more than 10%. ROCOF results in faster operation than the remaining methods discussed in this study for active and reactive power mismatch. However, ROCOF does not detect the islanding condition if the power mismatch between DG and the local loads is less than 10% (Figs. 7 and 8).

The accuracy of the passive islanding detection schemes depends on the accuracy of the synchrophasor being computed by the PMU. Transients have a major effect on estimated frequency and ROCOF. In [23] and [24], the authors have carried out extensive experiments on steady-state and dynamic compliance testing for PMUs from three different vendors. Most of the commercial PMUs used in this study failed the dynamic compliance testing; however, once the dynamic (transient) condition is over, all three PMUs remain within the maximum-allowable tolerance limits for frequency error and ROCOF thresholds. The authors believe that the 10-cycle timer used in the simulation accommodates for transients (fault + breaker opening) and, therefore, the PMUs frequency estimation can be considered reliable enough during the posttransient disturbance condition.

All of the local synchrophasor-based islanding detection techniques discussed in Section V are, in reality, performed by stand-alone protection relays, for example, overvoltage/undervoltage protection relay (ANSI Code 59/27), overfrequency/underfrequency (ANSI Code 81), and ROCOF (ANSI Code 81R). All of these protection relays are configured either to provide instantaneous tripping or definite time-based tripping (once the fault is picked up, a relay waits for a certain preconfigured time before issuing a trip). These protection relays will not require synchrophasor estimation and subsequent utilization to perform islanding.

Local synchrophasor-based islanding detection schemes are the first logical step toward the implementation of more complex and wide-area synchrophasor-based islanding schemes. This helps increase the confidence of transmission system operators (TSOs) and distribution system operators (DSOs) on PMU technology utilization in time-critical protection schemes such as anti-islanding. As a result, this will build trust on utilizing wide-area synchrophasor technology for different protection schemes that may benefit from it.

The islanding detection schemes presented and tested in Section V can be utilized for both transmission and distribution systems. Since the schemes are based on synchrophasors,

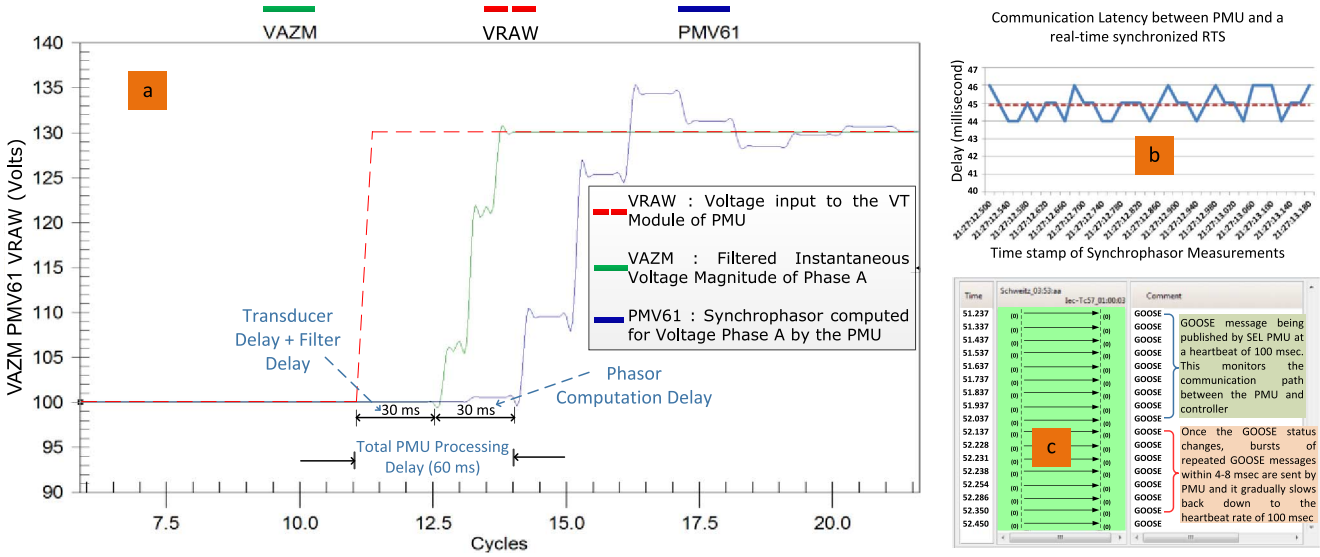

Fig. 9. Calculation of different latencies: (a) PMU processing delay (60 ms), (b) delay associated with assembling synchrophasors in IEEE C27.118.2 format (45 ms), and (c) communication latency of GOOSE messages (4 ms).

limitation of the current PMU technology (their accuracy and compliance with the standard), make them suitable to be utilized only in transmission networks. However, with the ongoing development of more accurate and robust PMUs for distribution systems, the same schemes can be used in the distribution grid [8], [25] in the future.

The proposed hybrid synchrophasor and IEC 61850-8-1-based islanding scheme involves some unavoidable time delays. These delays are due to the use of PMUs and the communication link involved for streaming out synchrophasors and GOOSE messages. Fig. 9 depicts the calculation of different latencies. They are explained as follows.

PMU Processing Delay: Synchrophasors are computed by filtering the incoming analog voltage and current signals fed to the PMU's voltage-transformer (VT) and current-transformer (CT) transducers, respectively. These filtered voltage and current measurements are used to compute synchrophasors. In order to accurately identify delays, event recordings of the PMU were retrieved and the raw input analog signal, filtered measurements in the PMU and the computed synchrophasor of PMU were plotted. The difference between a raw input analog signal from a testset and the filtered measurements retrieved by PMU gives the filter delay, which is 30 ms [Fig. 9(a)]. The difference between filtered measurements and the associated synchrophasor provides a synchrophasor algorithm delay which is also 30 ms [Fig. 9(a)]. So the PMU processing delay is 60 ms.

IEEE C37.118.2 Frame Formation Delay: In order to investigate the delay associated with the packaging of synchrophasors in the IEEE C37.118.2 format, the real-time simulator (Opal-RT) [11] was synchronized to a coordinated universal time (UTC) traceable time-source similar to the one provided by the global positioning system (GPS). For this purpose, the hardware GPS synchronization module from Spectracom (Tsync-PCIe express board) was used [26]. This module provides a UTC time-stamp within the real-time environment (using dedicated libraries provided by the vendor Opal-RT) and provides a PPS signal to a clock adapter to generate a synchronized clock. The way the driver of this module works is that it reads the integration time-stamp configured in the mathematical model and generates a pulse at the corresponding frequency, which is aligned to the PPS of the GPS source. The synchrophasor stream from the PMU is received inside the simulation model using C37.118 data parsing (C37.118 Master block provided by the vendor Opal-RT). This block captures real PMU streams (based on the configuration file setup) and reads these synchrophasors directly inside the simulation model. Fig. 10(a) shows the Opal-RT eMEGAsim Real-Time Simulator architecture with a time synchronization module inserted while Fig. 10(b) shows the Simulink model to read the GPS synchronized in real time and to parse the synchrophasor stream inside the simulation model. The latency was computed to be 45 ms with a jitter of 2–3 ms [Fig. 9(b)].

GOOSE Latency: PMU streams out the GOOSE message with a preconfigured "heartbeat" rate. The heartbeat rate chosen for this study was 100 ms. Every 100 ms, the PMU sends to the communication link the GOOSE messages it is configured to publish. However, if there is a state change in the value of the GOOSE message, the PMU sends a burst of repeated GOOSE messages within 4 to 8 ms, only gradually slowing back down to a heartbeat rate of 10 messages/s again [Fig. 9(c)]. The maximum delay encountered by the GOOSE message is thus 4–8 ms.

Islanding Detection Algorithm Delay: The PMU's protection and control processing capability specifies that the PMU updates its calculations/status at a rate of 8 times per power system cycle [13]. At 50 Hz, the relay processes the logic every 2.5 ms. At a reporting rate of 50 frames/s or every 20 ms, the protection logic equations are updated every 2.5 ms. The algorithm is executed every 2.5 ms irrespective of the complexity of the algorithm. Once the al-

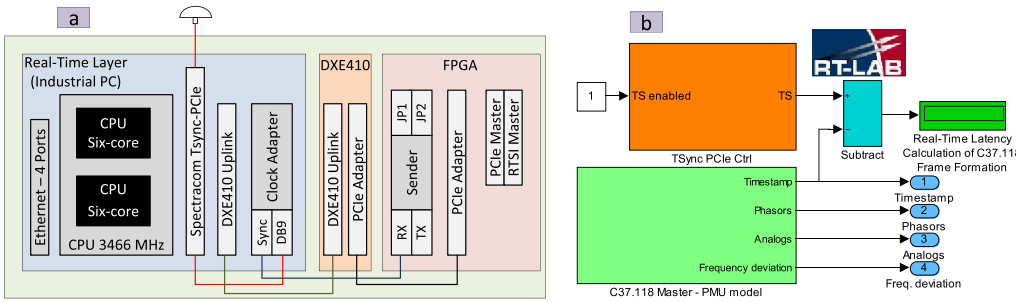

Fig. 10. (a) Opal-RT architecture showing the coupling of the Spectracom time-synchronization module to synchronize the simulator with the GPS, and (b) shows the Simulink model with one block to provide real-time signals while the other block parses an incoming synchrophasor stream from the PMU in C37.118.2 format.

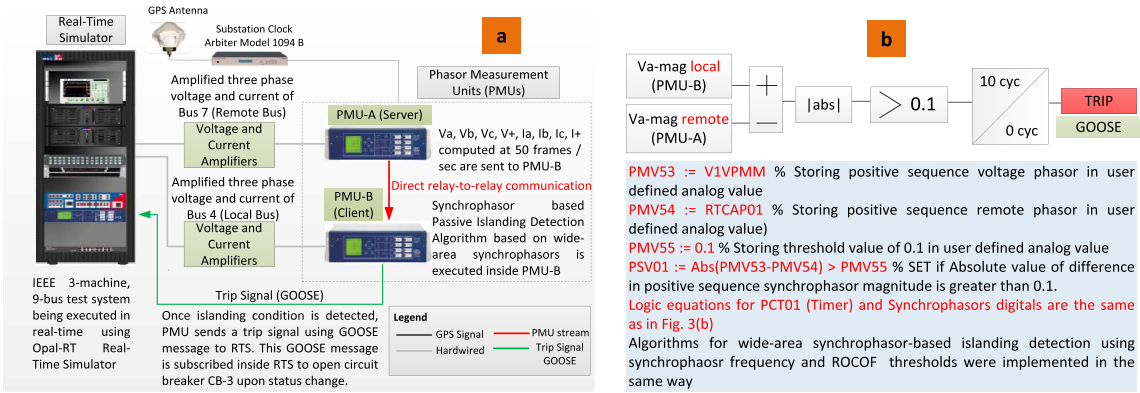

Fig. 11. (a) Experimental setup for performance analysis of the synchcrophasor-based islanding detection schemes using wide-area synchrophasors, and (b) logic equations used to deploy the wide-area synchrophasors-based passive islanding scheme using overvoltage/undervoltage thresholds. The algorithm is deployed within PMU-B.

gorithm gets too complex (e.g., if it uses too many protection logic equations and variables), the PMU issues a status representing that the PMU execution capability is exceeded.

The only intentional delay, which was introduced, was the timer of 10 cycles (PCT01PU) to ensure that the islanding detection scheme only operates if the synchrophasor quantities exceed the threshold for more than 10 cycles [20].

VII. Wide-Area Passive Islanding Schemes

In order to investigate the benefit of utilizing wide-area synchrophasor measurements for the passive islanding algorithms presented in Section V, the RT-HIL setup shown in Fig. 11(a) is deployed. PMU-B is considered to be a local PMU (in the vicinity of a DG) being fed with currents and voltages from Bus-4, while PMU-A is a remote PMU installed at Bus-7 and streams out synchrophasors at the same rate of 50 frames/s. The experimental sequence presented in Section V was repeated to simulate the islanding scenario.

The same strategy of deploying islanding detection algorithms within the PMU is carried out by making PMU-B a client for PMU-A and using a direct relay-to-relay communication technique between them. The direct relay-to-relay communication technique allows the two PMUs to exchange synchrophasors directly, without the requirement of an intermediate PDC [13]. This reduces the overall latency of the wide-area synchrophasor-based islanding detection schemes, and it further advocates one of the contributions of this paper which is to test and validate these islanding schemes with minimum latencies. Thus, PMU-B processes the remote synchrophasor data, time aligns them with local data internally, and makes them available for the passive islanding schemes.

The logic equations used to deploy the overvoltage/undervoltage-based passive islanding detection algorithm using wide-area synchrophasor measurements within PMU-B are shown in Fig. 11(b). In PMU-B (client), an analog variable is dedicated to store the value of the positive-sequence synchrophasor voltage magnitude being received by PMU-A (server). The rest of the algorithm is similar to the one presented in Fig. 3(b). The only difference is the utilization of the difference in magnitude of the positive-sequence voltage synchrophasor between local and remote buses to detect islanding conditions. The threshold for this scheme was set to 0.1 p.u. to compare the results with the local synchrophasor-based scheme.

Similarly, wide-area synchrophasor-based islanding detection algorithms using overfrequency/underfrequency were also implemented. In this case, the absolute value of the difference in synchrophasor frequency between local and remote buses was used to detect islanding. The threshold for this scheme was set to 1 Hz for comparison purposes.

Finally, a wide-area synchrophasor-based ROCOF islanding detection scheme was implemented by deploying an algorithm in PMU-B that adds an absolute value of ROCOF from local and remote PMUs and detects islanding if this value exceeds a threshold of 0.2 Hz/s.

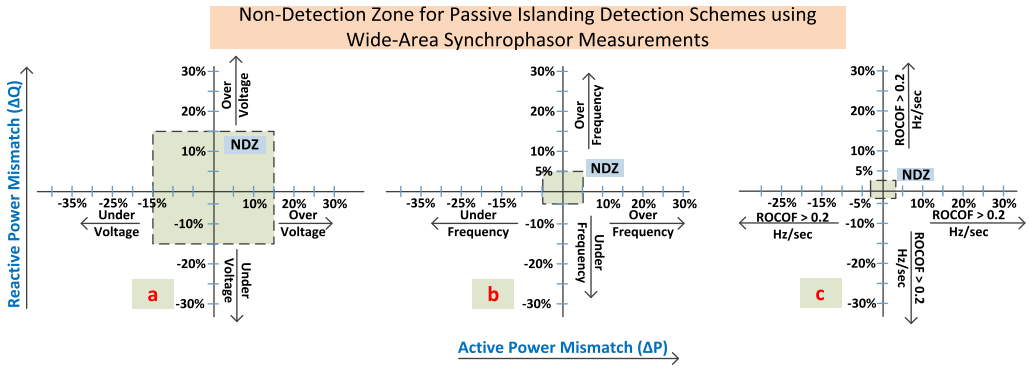

Fig. 12. Nondetection zone (NDZ) for wide-area synchrophasors-based passive islanding detection. (a) Undervoltage/overvoltage-based islanding detection scheme with abs $|V_{B-PMU} - V_{A-PMU}| \geq 0.1$ p.u. (b) Underfrequency/overfrequency-based detection method with abs $|f_{B-PMU} - f_{A-PMU}| \geq 1$ Hz, and (c) ROCOF-based islanding detection scheme with the $ROCOF_{B-PMU} + ROCOF_{A-PMU}$ threshold limit set to 0.2 Hz/s.

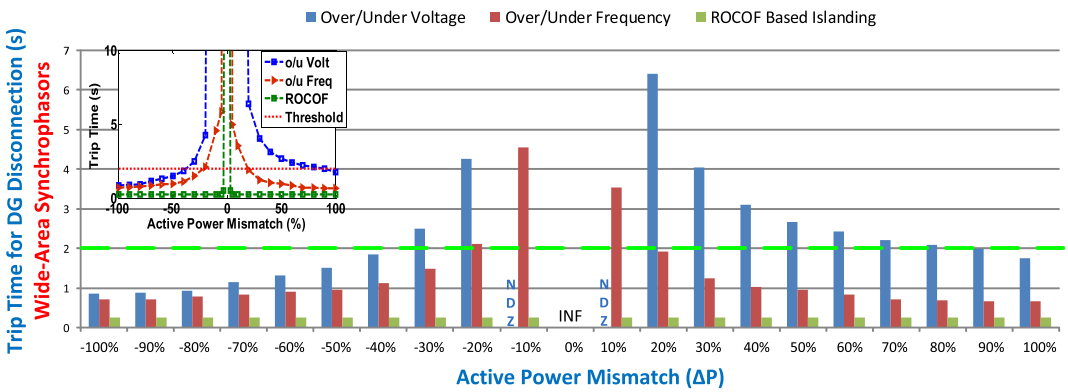

Fig. 13. Operation time of passive islanding detection schemes (wide-area synchrophasors) when there is an active power mismatch.

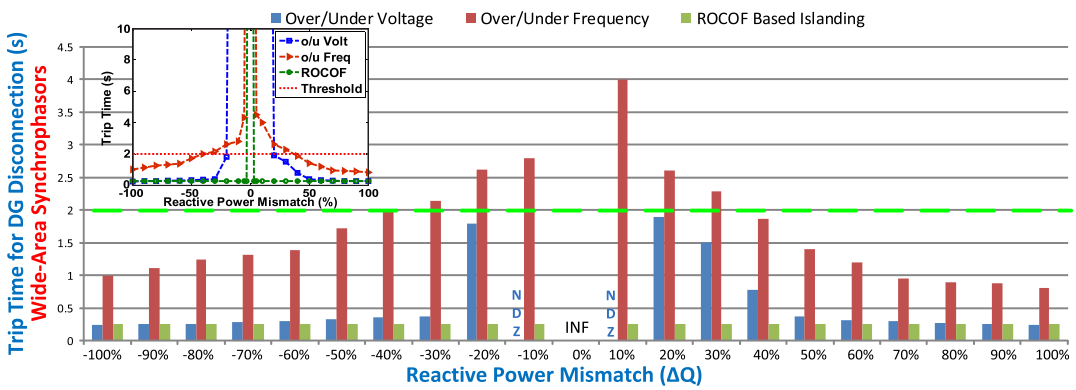

Fig. 14. Comparison of operation time of passive islanding detection schemes (wide-area synchrophasors) when there is reactive power mismatch.

VIII. RT-HIL Simulation Results for Wide-Area Passive Islanding Schemes

The NDZ for wide-area passive islanding schemes is shown in Fig. 12, while Figs. 13 and 14 show the operating time of these schemes for active and reactive power mismatch. The operating times of all the schemes decreases with an increase in active or reactive power mismatch between the DG and local load (Figs. 13 and 14).

Compared to NDZ with local synchrophasors (Fig. 5), the NDZ with a wide-area synchrophasor for the overvoltage/undervoltage scheme [Fig. 12(a)] is reduced from 30% to 15%; for the overfrequency/underfrequency, the NDZ is reduced from 10% to 5% [Fig. 12(b)]; and for the ROCOF-based scheme, the NDZ is reduced from 10% to 3% [Fig. 12(c)].

The ROCOF-based scheme results in faster operation for active and reactive power mismatches [Figs. 13 and 14] than the remaining methods. However, the operating time of the ROCOF-based scheme reduces from 0.6 s (Figs. 7 and 8) with local synchrophasors to 0.25 s (Figs. 13 and 14) with wide-area synchrophasors.

The acceptable operation time of the islanding detection scheme with overfrequency/underfrequency thresholds is achieved when there is an active power mismatch of at least 20% (Fig. 13) while utilizing wide-area measurements whereas an active power mismatch of at least 30% is required when

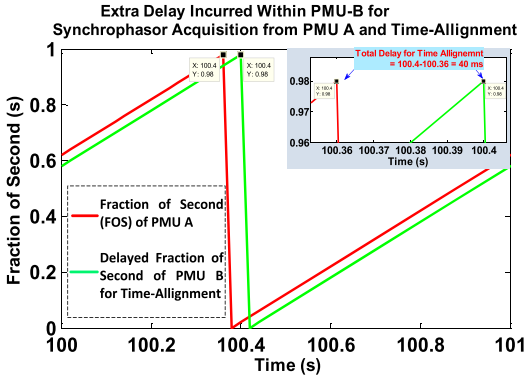

Fig. 15. Additional delay of 40 ms incurred inside PMU-B for synchrophasor acquisition from PMU-A and its time alignment while executing wide-area synchropahsors-based passive islanding detection schemes.

utilizing local synchrophasors (Fig. 7). Similarly, all passive islanding detection schemes utilizing wide-area measurements (Figs. 13 and 14) require less active and reactive power mismatch compared to local synchrophasor-based schemes (Figs. 7 and 8) to operate within 2 s.

The wide-area synchrophasor-based islanding detection schemes deployed and analyzed in this section are subjected to one additional delay (in addition to those discussed in Section VI). This additional delay is 40 ms. It occurs inside PMU-B for the synchrophasor acquisition from PMU-A (remote) and its time alignment with local synchropahsors, which is required to execute wide-area islanding algorithms. This latency is calculated by taking the difference of the fraction of second [18] associated with the synchrophasor frame from PMU-A (remote) and the fraction of second of the delayed, time-aligned PMU-B (local) measurements as shown in Fig. 15.

IX. Conclusion

This paper presented the implementation and RT-HIL performance assessment of three passive islanding detection methods that exploit local and wide-area synchrophasor measurements and initiate tripping using IEC 61850-8-1 GOOSE messages. ROCOF-based islanding detection schemes are effective for active and reactive power mismatch, and result in faster operation time compared to overfrequency/underfrequency and overvoltage/undervoltage-based islanding detection schemes. For the same islanding detection techniques, wide-area measurements not only perform faster, but also have smaller NDZs compared to local synchrophasor-based schemes.

By performing more than 400 RT-HIL experiments, this paper shows that if latencies are kept to a minimum, wide-area passive islanding detection schemes reduce the NDZ to half or two-thirds of the one using local synchrophasors.

The proposed hybrid schemes ensure minimum communication delays. This is due to the use of synchrophasor measurements internally in a PMU to perform these protection actions using logic equations to avoid the delays incurred due to the intermediate PDC or IEEE C37.118.2 protocol parser. The RT-HIL testbench proved effective in accurately calculating the latencies, such as PMU filtering delay, PMU synchrophasor computation delay, latencies associated with remote measurements time alignment, PMU algorithm execution delay, synchrophasor frame formation delay, and GOOSE message delays.

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