# Active Fault Current Limiting Control for Half-bridge MMC in HVDC Systems

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***Abstract*—DC faults of MMC can result in a significantly large fault current due to the discharge of submodule capacitors. The fault current not only risks damaging the MMC but also demands a considerable breaking capacity from the dc circuit breaker (DCCBs). This paper introduces two novel active fault current limiting methods (AFCLs), namely virtual impedance-based and energy control-based AFCL. The first method utilizes circulating current feedforward, which introduces a virtual arm impedance to suppress the rate of rise of the fault current. Meanwhile, the second method relies on the control of the internally stored energy of the MMC to automatically minimize the number of submodules that discharge during a dc-side fault. Therefore, both the dc-side current and the MMC arm current can be effectively suppressed after the occurrence of the fault. The proposed methods do not require fault detection and their response is proportional to the rate of rise in the fault current. Simulation case studies are presented to demonstrate the proposed methods.**

***Index Terms*—modular multilevel converter (MMC), dc fault, active current limiting control, virtual impedance, energy control**

## I. Introduction

DC faults in MMC-based HVDC systems can primarily be divided into two categories: pole-to-pole and pole-to-ground faults. The pole-to-ground fault is usually of less concern w.r.t. the fault current, which is limited by a high-impedance grounding scheme in either the ac- or dc-side that prevents the discharge of SMs. On the contrary, the fault current during a pole-to-pole fault condition has a significantly high peak value and a rapid rate of rise due to the low number of inductive elements within the dc-grid. A large pole-to-pole fault current can cause damage to the switching and protection apparatus of the MMC, and usually impose substantial challenges for the dc circuit breakers (DCCBs), such as increasing the required current interruption capacity and fault clearance time. In addition, in radial and meshed HVDC systems, it is usually preferable to avoid the MMC's SM blocking action and utilize DCCBs to interrupt the fault current, thus facilitating selective protection [1], [2]. As a result, fault current limiting is crucial for MMC-HVDC protection.

The methods to limit the dc fault current fall into two broad categories: passive and active. Passive methods require the installation of dc smoothing reactors or superconducting current fault limiters (SFCLs) at the dc outlet of MMC stations [3], [4], while active methods work by using the MMC controls. Despite the fact that passive methods are straightforward and can effectively limit the fault current, additional passive elements increase the cost and space requirements, and could jeopardize the dynamics and stability of the overall dc system [5]. Among the active methods in existence, one category of methods involves the use of full-bridge submodules (FBSMs), hybrid FBSMs and Half-Bridge SMs (HBSMs) or other topologies [6], which can generate dc voltage opposite to the direction of the fault current, thereby limiting the fault current. Nevertheless, compared to HB-MMC, the number of IGBTs used and the power losses are doubled (or even greater). Since HB-MMCs are widely used in practical applications, approaches that integrate additional control functions to limit the fault current have attracted significant interest. Such approaches include emulation of a virtual dc-side reactor through controls [7], and bypassing SM by decreasing the insertion indices of the MMC [8], [9]. Because the virtual dc-side reactor is emulated by modifying the phase current control command generated by the dc voltage control or the real power control, it is not suitable for the MMC rectifier controlling ac-side voltage and frequency. On the other hand, bypassing essentially involves changing the duty ratio (denoted as $d$) of the MMC after the fault occurrence [10], which includes bypassing all SMs (i.e., $d = 0$) or part of them (i.e., $d$ is a fixed constant between $0 \sim 0.5$). By doing so, the fault current is effectively limited due to the reduced number of SMs that have been discharged. However, exsiting bypassing schemes present several limitations: 1) Bypass strategies in [9], [10] are initiated when protection detects a dc fault, usually $2 \sim 3$ *ms* after fault occurrence, a period during which the fault current may still induce the overcurrent of the MMC and blocking operation; 2) Immediate bypassing all the SMs in [9] is not necessary when a MMC is located far away from the fault; 3) For partial bypassing of SMs [10], the calculation of $d$

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requires knowledge of the inductance and capacitance in the fault circuit, which is not practical.

In order to address the shortcomings of the existing active current limiting control (AFCL), this paper first proposes a method based on circulating current feedforward control that emulates the reactor in each arm to prevent the fault current from rising greatly. This approach is applicable to both MMC inverters and rectifiers, serving as a complement to the virtual dc-side reactor-based AFCL method proposed in [7]. Furthermore, given the correlation between the discharge of the SM capacitors and the decrease in the internally stored energy of the MMC, the paper proposes an energy control-based AFCL method. This method adjusts the duty cycle $d$ in response to the variations of the internally stored energy of the MMC, with the aim of minimizing the discharge of the SM capacitors. Importantly, neither of the proposed methods requires fault detection signals and associated triggering delay, and both are self-adaptive to the rising rate of fault current.

The remainder of this paper is structured as follows. Section II reviews and provides an analysis of the fault current. Sections III and IV introduce the virtual impedance-based and energy-control-based AFCL methods together with their respective design considerations. Section V validates the effectiveness of the proposed AFCL methods by conducting electromagnetic transient (EMT) simulations in a symmetrical monopole HB-MMC-based HVDC system. Section VI concludes the paper.

## II. Pole-to-pole Fault of MMC

As previously noted, a pole-to-pole fault typically exhibits a more severe fault current than a pole-to-ground fault. To limit the scope of the paper, this paper will focus on pole-to-pole faults within an HB-MMC-based symmetrical monopole system. More specifically, the presentation and examples concentrate on a pole-to-pole fault located at the dc-bus of the MMC station, as depicted in Fig. 1. In addition, the analysis of different stages of the dc fault presented in [11], [12] indicates that the discharge of SMs stops immediately upon their blocking. Therefore, this paper investigates the active current limiting controls during the stage immediately following the occurrence of the dc fault and prior to blocking SMs.

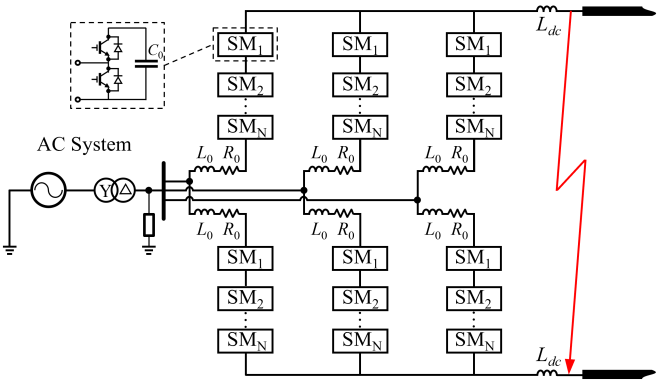


Fig. 1. Diagram of the HB-MMC power stage under study

### A. Averaged Equivalent Circuit under a Pole-to-pole Fault

The fault current is comprised of the dc discharge current of the SMs and the ac infeed current from the ac system, with the dc component serving as the predominant component before the blocking of the SMs [11]. During this stage, typically the first few milliseconds after the fault, the control and modulation of MMC still continuously change the number of SMs being inserted. As a result, the discharged SMs vary after the fault occurs, which makes the fault circuit of a non-linear time-varying nature. Therefore, to model the equivalent fault circuit while considering the change in inserted SMs, the state-space averaged model of the equivalent fault circuit can be posed as (see [10]):

$$\begin{bmatrix} L_{eq} & 0 \\ 0 & C_{eq} \end{bmatrix} \frac{\mathrm{d}y}{\mathrm{d}x} \begin{bmatrix} \bar{i}_{dc}(t) \\ \bar{v}_c(t) \end{bmatrix} = \begin{bmatrix} -R_{eq} & 2dN \\ -\frac{d}{2N} & 0 \end{bmatrix} \begin{bmatrix} \bar{i}_{dc}(t) \\ \bar{v}_c(t) \end{bmatrix} \tag{1}$$

where $\bar{i}_{dc}(t)$ and $\bar{v}_c(t)$ represent the averaged dc fault current and SM capacitor voltages, respectively. The term $d$ denotes the duty ratio, which is the ratio between the inserted SMs and the total number of SMs per phase. The equivalent resistance, inductance, and capacitance, denoted as $R_{eq}$, $L_{eq}$, and $C_{eq}$, respectively, are defined as follows:

$$R_{eq} = \frac{2}{3}R_0; \quad L_{eq} = \frac{2}{3}L_0 + 2L_{dc}; \quad C_{eq} = \frac{3C_0}{2N} \tag{2}$$

in which $R_0$, $L_0$ and $C_0$ represents arm resistance, arm inductance and SM capacitance, respectively, while $L_{dc}$ signifies the dc smoothing reactor.

Assuming the fault occurs at $t = t_0$, the averaged equivalent fault ciucuit in *Laplace* domain can be dipcted as Fig. 2

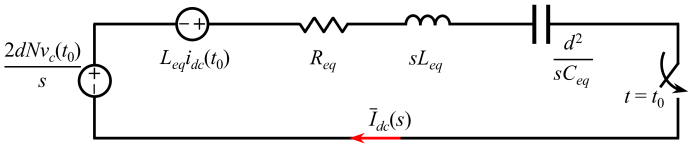


Fig. 2. Averaged equivalent fault circuit before blocking SMs

### B. DC Fault Current Response

Based on the averaged equivalent circuit presented in Fig. 2, the averaged dc fault current can be obtained as

$$\bar{I}_{dc}(s) = \frac{2dNv_c(t_0) + sL_{eq}i_{dc}(t_0)}{s^2L_{eq} + sR_{eq} + d^2/(sC_{eq})} \tag{3}$$

where $i_{dc}(t_0)$ and $v_c(t_0)$ denote the initial dc current and SM capacitor voltage at $t = t_0$, respectively. Taking the inverse *Laplace* transform of (3) yields

$$\bar{i}_{dc}(t) = e^{-\frac{t}{\tau_{dc}}} \left[ -\frac{i_{dc}(t_0)}{\sin\theta_{dc}} \sin(\omega_{dc}t - \theta_{dc}) + \frac{2dNv_c(t_0)}{R_{dis}} \sin(\omega_{dc}t) \right] \tag{4}$$

where

$$\begin{cases} \tau_{dc} = \frac{2L_{eq}}{R_{eq}} & \omega_{dc} = \sqrt{\frac{1}{C_{eq}L_{eq}} - \frac{R_{eq}^2}{4L_{eq}}} \\ \theta_{dc} = \tan^{-1}(\tau_{dc}\omega_{dc}) & R_{dis} = \sqrt{\frac{L_{eq}}{C_{eq}} - \frac{R_{eq}^2}{4}} \end{cases} \tag{5}$$

The term influencing the amplitude of $\bar{i}_{dc}(t)$ in (4) is not readily interpretable, necessitating further simplification of (4) for ease of analysis. Given that $R_0$ is typically designed to be small to minimize the power loss of MMC, $R_{eq}$ can be reduced to zero. This leads to the following approximations: 1) $e^{-\frac{t}{\tau_{dc}}} \approx 1$; 2) $\theta_{dc} \approx \pi/2$; 3) $\omega_{dc} \approx \sqrt{1/(C_{eq}L_{eq})}$; 4) $R_{dis} \approx \sqrt{L_{eq}/C_{eq}}$. Consequently, (4) can be simplified as:

$$\bar{i}_{dc}(t) \approx \frac{2dNv_c(t_0)}{\sqrt{L_{eq}/C_{eq}}}\sin(\omega_{dc}t) + i_{dc}(t_0)\cos(\omega_{dc}t). \tag{6}$$

Considering the use of a dc smoothing reactor, the value of $\omega_{dc}$ is typically small. Thus, within a few milliseconds right after the fault occurs, two small-angle approximations can be used: 1) $\sin(\omega_{dc}t) \approx \omega_{dc}t$; 2) $\cos(\omega_{dc}t) \approx 1$. Substituting these two approximations into (6), yields

$$\bar{i}_{dc}(t) \approx \frac{2dNv_c(t_0)}{L_{eq}}t + i_{dc}(t_0). \tag{7}$$

As indicated by (7), there exist two potential approaches to constrain the increase of fault current:

- Increasing $L_{eq}$, for instance, by using a larger dc smoothing reactor or using virtual dc reactor-based control.
- Decresing $d$, which implies a reduction in the number of discharged submodules.

## III. Virtual Impedance-based AFCL

### A. Basic Principle of VI-AFCL

The active fault currrent limting strategy proposed herein builds upon the circulating current feedforward scheme illustrated in Fig. 3, delineated in blue. Specifically, a derivative term, $sK_v$, is placed in parallel with a standard $2^{nd}$-order circulating current suppression controller (CCSC) [13]. Within Fig. 3, $K_v$ represents the gain of the circulating current feedforward loop, while $H_z^x(s)$ denotes the Proportional-Integral (PI) compensator of the CCSC. $i_z^x$ represents the circulating current, note that, $x$ designates the phase (a, b, c). To prevent potential interactions between the CCSC and the feedforward loop, and to avoid undesired effects from other high-frequency components in the circulating current, the feedforward loop should include a first-order lowpass filter with comparatively lower bandwidth. The resulting tranfer function of the feedforward controller can thus be given by

$$H_{vi}(s) = \frac{sK_v\omega_c}{s+\omega_c} \tag{8}$$

where $\omega_c$ represents the cuttoff frequency of the first-order lowpass filter.

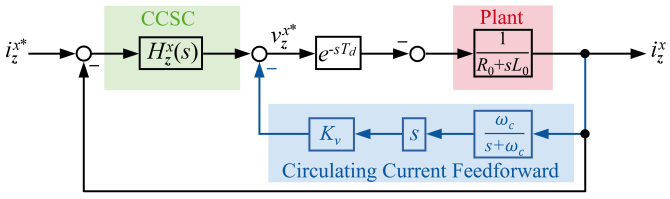


Fig. 3. Block diagram of CCSC and circulating current feedforward control.

Note that during steady-state operation, the dc component of the circulating current remains virtually constant, making the output of $H_{vi}(s)$ negligible. Therefore, the effect of VI-based AFCL on the dc current of MMC can be ignored during normal opeartion of MMC. However, when a fault occurs, the dc component of the circulating current experiences a significant increase due to the discharging of the SMs, and the $2K_v$ virtual $R-L$ sections are immediately inserted across the three legs of the MMC.

Drawing upon Fig. 3, the equivalent circuit of MMC's fault response is depicted in Fig. 4. The feedforward loop can be visualized as multiple virtual parallel $R-L$ sections connected in series with the arm reactors and the dc smoothing reactor of the MMC. As presented by Fig. 4: 1) the quantity of $R-L$ sections equals $2/3\cdot K_v$; 2) the reactance in each $R-L$ section equals 1 henry; 3) the resistance of each $R-L$ section corresponds to the cutoff frequency of the selected lowpass filter, that is, $R_v = \omega_c$ ohms. This approach is herein named as the virtual impedance-based active current limiting (VI-based AFCL) method.

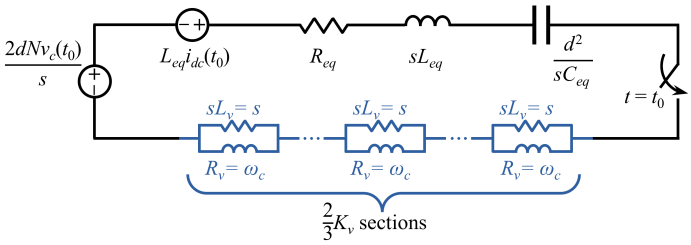


Fig. 4. Equivalent fault circuit of an MMC with the proposed VI-based AFCL.

### B. Design Considerations of $K_v$ and $\omega_c$

The expressions for the virtual impedance depicted in Fig. 4 does not reflect any time delay effect. This is due to the fact that the fault circuit response primarily concerns components in dc, where the delay effect on the circulating current feedforward control can be neglected at this frequency. However, when considering the impact of delay on the controller and MMC, improper selection of $R_v$ (i.e., $\omega_c$) and $K_v$ could potentially result in: 1) instability of the circulating current feedforward loop; 2) degradation of the small-signal stability of the MMC, leading to oscillations between the MMC and the dc grid during normal operation. Consequently, the appropriate tuning of $K_v$ and $\omega_c$ is discussed next.

#### 1) Parameter Tuning of $K_v$

Based on Fig. 3, the loop gain of proposed circulating current feedforward loop can be expressed as

$$G_{vi}(s) = K_v\omega_c\frac{1}{R_0+sL_0}\frac{s}{s+\omega_c}e^{-sT_d}. \tag{9}$$

To better understand the influence of $K_v$ on the loop gain, Fig. 5 illustrates the frequency response of $G_{vi}(s)$, with $\omega_c$ fixed at $2\pi\cdot 5$ rad/s, $K_v$ selected as 3, 7, and 10, and a control delay time $T_d = 200\mu s$ is assumed. The plot clearly demonstrates an increase in the crossover frequency of $G_{vi}(s)$ as $K_v$

is enlarged, which could potentially lead to loop instability when the phase response of $G_{vi}(s)$ falls below -150° (that is, the phase margin of 30°). As a result, while a larger $K_v$ can enhance the current limiting effect due to an increase in inductance, it should not exceed a certain upper limit, which is determined by the loop stability of $G_{vi}(s)$.

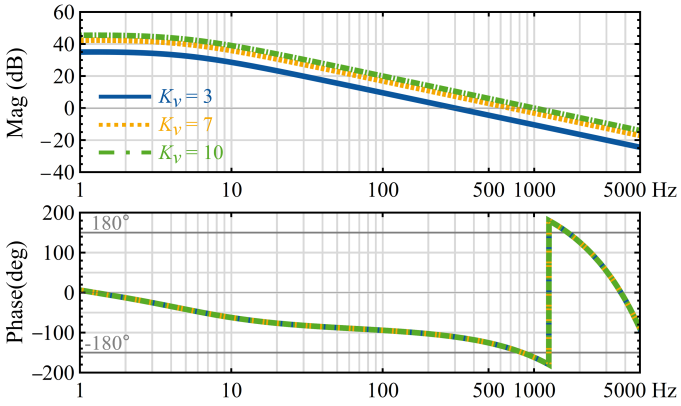


Fig. 5. Frequency response of loop gain of circulating current feedforward with $\omega_c = 2\pi 5$ rad/s

Based on the above analysis, given specific values for $\omega_c$ and $T_d$, the maximum value of $K_v$ must be set to that corresponding to a phase response of $G_{vi}(s) = -150°$ at the crossover frequency. Consequently, the upper limit of $K_{v,max}$ can be determined by solving

$$\begin{cases} \omega_{cross} = \mathsf{FindRoot}[G_{vi}(j\omega) = 0] \\ K_{v,max} = \mathsf{FindRoot}[|G_{vi}(j\omega_{cross})| = 1] \end{cases} \tag{10}$$

where, FindRoot denotes the solution of the roots of the polynomial, which can be programmed in any available numerical computing environment.

*2) Parameter Tuning of $\omega_c$*

As illustrated in Fig. 4, $R_v$ determines the real part of the virtual impedance emulated by the proposed circulating current feedforward loop. Due to the influence of the time delay $e^{-sT_d}$ on the controller, such real part of the virtual impedance becomes negative in the high-frequency range [14], [15], introducing negative damping to the MMC. This might lead to instability if the system resonance between the MMC and the dc grid falls off the MMC's negative damping region. Therefore, the selection of $\omega_c$ must take into account the small-signal stability of the MMC dc impedance. The averaged model of the MMC from the dc-side in [16] defines the high-frequency impedance behavior of the MMC, which can be expressed as

$$Z_{dc}(s) = \frac{2}{3}(sL_{arm} + R_{arm}) + \frac{2}{3}H_{vi}(s)e^{-sT_d} + \frac{V_{dc}^2/P_0}{1 + sC_{eq}v_{dc0}^2/P_0} \tag{11}$$

where $C_{eq} = 6C_{sm}/N$, $V_{dc}$ and $P_0$ is the rated dc voltage and power of MMC, respectively. It should be noted that $\omega_c$ in (8) is chosen to be in the tens of rad / s, allowing $s/(s+\omega_c)$ to be approximated as unity in the high-frequency range. In addition, the arm resistance is typically designed to be small to minimize power loss, thus contributing a negligible amount of damping to MMC impedance in the high-frequency range [14]. As a result, (11) can be further simplified as:

$$Z_{dc}(s) = \frac{2}{3}sL_{arm} + \frac{2}{3}K_v\omega_c e^{-sT_d} + \frac{V_{dc}^2/P_0}{1 + sC_{eq}V_{dc}^2/P_0} \tag{12}$$

To better show the effects of $\omega_c$ on the MMC dc impedance in the high-frequency range, Fig. 6 compares the dc impedance responses with selections of $\omega_c$ varing between $2\pi 3$ rad/s to $2\pi 7$ rad/s. In this case, the MMC control delay is fixed to 200 $\mu s$ and $K_v = 5$. The comparison shows that a higher value of $\omega_c$ increases the level of negative damping between roughly 1-3 kHz, making the MMC prone to resonances on the dc side in this frequency range. However, it is not suggested to select a relatively small $\omega_c$ as it could compromise the fast response of the VI-based AFCL to dc faults. Therefore, the selection of $\omega_c$ should start from 1 Hz and gradually increase it to as high as possible, while simultaneously ensuring that $Z_g(s)/Z_{dc}(s)$ satisfies the Nyquist stability criterion, where $Z_g(s)$ denotes the impedance of the dc grid.

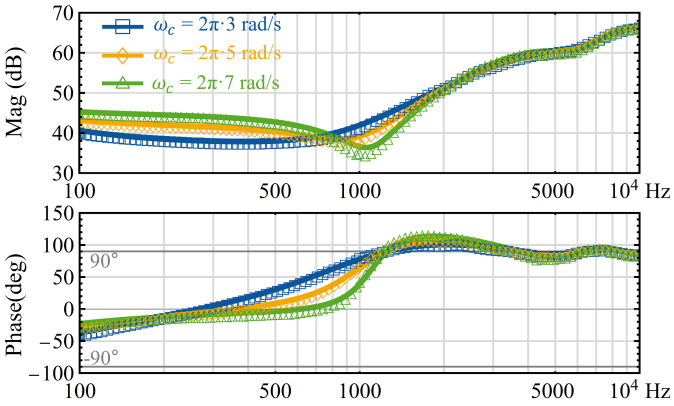


Fig. 6. Effects of $\omega_c$ on MMC dc impedance: numerical scans (plot markers) versus anlytical results predicted by (12) (solid lines)

## IV. Energy Control-based AFCL

As indicated by (7), the fault current is proportional to the number of SMs inserted in the arm. This number can be intentionally adjusted by manipulating the duty ratio, $d$. A reduction in $d$ leads to a decrease in the number of SMs involved in the fault circuit, which in turn limits the dc fault current.

### A. Internally Stored Energy Control

The dynamics of internally stored energy of MMC is approximated as [17]

$$\frac{\mathrm{d}w_\Sigma}{\mathrm{d}t} \approx v_{dc}3i_z^0 - p_{ac} \tag{13}$$

where $w_\Sigma$ is the internally stored energy of the MMC, $i_z^0$ denotes the zero-sequence common-mode current, $v_{dc}$ represents the dc-side voltage and $p_{ac}$ the average ac power exchanged between the MMC and the ac system. During

steady-state operation, the dc grid voltage is assumed constant due to the voltage regulation provided by the MMC in the dc-voltage control mode (e.g., a master MMC in a multi-terminal system). Therefore, to keep the mean value of $w_\Sigma$ constant, the MMC should adjust $i_z^0$ in each phase, to compensate for any fluctuation in its internally stored energy.

### B. Basic Principle of EC-AFCL

The key characteristic of the MMC dc fault is the discharge of SM capacitors, which is directly related to changes in the zero-sequence circulating current ($i_z^0$) and the internally stored energy of the MMC ($w_\Sigma$). To adaptively determine $d$, in accordance with the discharging rate of SM capacitors, an internally stored energy control-based AFCL (EC-based AFCL) is proposed, as shown in Fig. 7. In Fig. 7, $H_W(s)$ is the energy controller and $H_z^0(s)$ denotes the zero-sequence circulating current (ZSCC) controller. Meanwhile, $v_z^{x*}$ represents the reference voltages produced by the CCSC. The fault current limiting mechanism of this method is listed below.

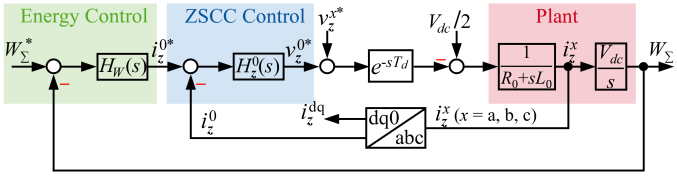


Fig. 7. Block diagram of energy-based active fault current limiting control.

1) Due to the discharging of SMs across all six arms, both the average values of $W_\Sigma$ and $i_z^0$ change immediately. In the dual-loop cascaded structure consisting of the energy control and the ZSCC control, the outer energy control loop is typically designed to exhibit at least ten times less bandwidth than the inner ZSCC loop. Therefore, when analyzing the behavior of the ZSCC control right after a dc fault occurs, $i_z^{0*}$ can be considered unchanged compared to $i_z^0$.
2) To regulate $i_z^0$ to $i_z^{0*}$, the ZSCC control will enlarge the zero-sequence voltage reference $v_z^{0*}$. Consequently, the total dc voltage reference for MMC's modulation decreases from $V_{dc}/2$ to $(V_{dc}/2 - v_z^{0*})$.
3) The insertion indices of the upper and lower arm of each phase are determined by the following equations (14), where $u$, $l$ indicates the upper and lower arm, $x$ the phase (a, b, c), and $v_s^{x*}$ the ac-side output voltage reference. As a result, with an increasing $v_z^{0*}$ provided by ZCSS control, both $n_u^x$ and $n_l^x$ will decrease and the SMs are bypassed.

$$\begin{cases} n_u^x = [V_{dc}/2 - v_s^{x*} - v_z^{x*} - v_z^{0*}]/V_{dc} \\ n_l^x = [V_{dc}/2 + v_s^{x*} - v_z^{x*} - v_z^{0*}]/V_{dc} \end{cases} \tag{14}$$

Note that, MMCs are usually operated under a direct modulation scheme [18], whereby the internally stored energy control asymptotically converges to its nominal value of $3C_{sm}V_{dc}^2/N$, even in the absence of energy control. This indicates that $v_z^{0*}$ are virutally zero during steady-state operation and do not affect the MMC insertion indices. However, energy control serves as a fallback, providing a way to automatically reduce the number of SMs inserted into the arms upon the occurrence of a fault (i.e., bypassing additional SMs).

A term, $\Delta d$, reffering to the 'displacement' in which $d$ varies, is introduced here for the purpose of indicating the level of SM bypassing. During steady-state operation, both $v_z^{0*}$ and $\Delta d$ are zero, thereby maintaining $d = 0.5$, and the amount of inserted SMs remains fixed at $N$. After the occurrence of a dc fault, due to the regulation of $H_z^0(s)$, $\Delta d$ is determined by

$$\Delta d = K_{pz}^0(i_z^{0*} - i_z^0) + K_{iz}^0 \int (i_z^{0*} - i_z^0)dt \tag{15}$$

where $K_{pz}^0$ and $K_{iz}^0$ are the proportional gain and integral gain of $H_z^0(s)$, respectively. As evident in (15), assuming that $i_z^{0*}$ remains unchanged before and right after a dc fault occurs, $\Delta d$ has a strong correlation with both $i_z^0$ and the design of $H_z^0(s)$. This relationship provides EC-AFCL with more advantages over existing bypassing-based AFCL methods [9], [10]. These benefits include:

- The automatic triggering of SM bypassing when a large variation in $i_z^0$ occurs, thereby eliminating the need for fault detection;
- Self-adaptability to the severity of SM's discharging as exhibited by Fig. 7 and (15). Specifically, a faster rate of rise in fault current results in a correspondingly faster increase in $v_z^{0*}$, leading to a quicker bypassing of the SMs. For instance, an MMC located close to the fault location (e.g., the dc-side of the MMC) could bypass all SMs within a few milliseconds, thereby preventing a substantial discharge current. Conversely, an MMC situated farther away from the fault location is more likely to bypass fewer SMs than an MMC located closer, facilitating its recovery once the dc fault is cleared.
- The bypassing rate can be adaptively adjusted according to the design of $H_z^0(s)$.

### C. Design Considerations of $H_W(s)$ and $H_z^0(s)$

#### 1) Control Tuning of $H_z^0(s)$

As the zero-sequence circulating current $i_z^0$ is part of the circulating current, $H_z^0(s)$ can be designed as a proportional-integral compensator, maintaining the same cutoff frequency and phase margin as standard CCSC. Given the response characteristic of an integrator and the slower time-domain response of $H_W(s)$ compared to $H_z^0(s)$, the variation in $d$ immediately after the occurrence of the fault will be mainly associated with the proportional gain of $H_z^0(s)$. Combining (7), (15), and the relationship between $d$ and $\Delta d$ (i.e., $d = 0.5 - \Delta d$), the approximation for the duty ratio can be expressed as follows:

$$d(t) \approx \frac{L_e}{4K_{pz}^0 t + 2L_e} \tag{16}$$

To expand on (16), consider two extreme scenarios:

- When the EC-AFCL is disabled, equivalently setting $K_{pz}^0 = 0$, $d(t)$ remains fixed at 0.5 both before and after the dc fault occurence. Consequently, no SMs will be bypassed for fault current limitation.

- Theoretically, when $K_{pz}^0$ is set to be infinitely large, $d(t)$ drops to zero immediately after the fault. In other words, all SMs will be bypassed immediately upon fault occurrence.

As indicated by (16), when EC-AFCL is used, the duty ratio $d$ changes w.r.t. time and is inversely proportional to $K_{pz}^0$.

*2) Control Tuning of $H_W(s)$*

In the dual-loop cascaded control structure depicted in Fig. 7, to minimize interference between the energy control loop and the ZSCC control loop, the loop transfer function $H_w(s)V_{dc}/s$ is typically tuned to operate ten times slower than $H_z^0(s)/(R_0+sL_0)$. Moreover, the stability of the MMC and dc grid must be ensured, which requires that $Z_g(s)/Z_{dc}(s)$ satisfies the Nyquist stability criterion, where $Z_g(s)$ represents the dc grid impedance.

Taking into account the attenuation effect of the SM capacitors on high-frequency components [14], tuning $H_W(s)$ solely affects the dc impedance of MMC in the low-frequency range. As an example, Fig. 8 illustrates the dc impedances of MMC rectifiers with: 1) identical design of the ZSCC control with a 200 Hz crossover frequency and 45° phase margin, 2) similar design of the VI-based AFCL control, and 3) different designs of internally stored energy control. The impedance responses differ significantly below the fundamental frequency, while they remain virtually identical to each other above the fundamental frequency. This distinction, in conjunction with the discussion in Section III.B, enables separate design considerations for VI-based AFCL and EC-based AFCL when both methods are implemented. Specifically, the design consideration for the VI-based AFCL should focus on its impact on the MMC's dc-side stability in the high-frequency range above the second fundamental. In contrast, the design consideration for the EC-based AFCL should center on its influence on the MMC's dc-side stability in the low-frequency range below the fundamental. In addition, $H_W(s)$ introduces a magnitude peak at the crossover frequency of the energy control loop and introduces negative damping below and above this frequency. Increasing the crossover frequency curbs the magnitude peak and shifts the onset of negative damping to a higher frequency. Generally, a low crossover frequency is not preferred as the large magnitude peak, together with the negative damping around the crossover frequency, can easily develop SSO between the MMC and dc grid in that frequency range. It is also worth noting that the bypassing rate of SMs is primarily determined by the design of $H_z^0(s)$, indicating that the design of $H_W(s)$ has a small effect on the fault current limiting performance of the EC-based AFCL. Nevertheless, the design of $H_W(s)$ should focus on the stability of the dc grid.

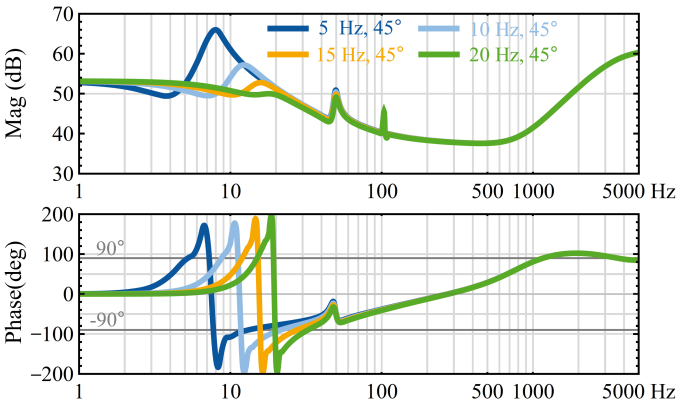


Fig. 8. Effects of energy controller $H_W(s)$ design on MMC dc impedance

## V. Simulation Studies

### A. System Description and Simulation Setup

In order to verify the efficacy of the proposed control methods, this section presents numerical simulation results obtained with MATLAB/Simulink. The simulation model is built based on a symmetrical mononpole system rated at 900 MW/ 640 kV, as shown in Fig. 9. During steady-state operation, the wind farm side MMC (WF-MMC) operates in an ac voltage control mode, while the grid side MMC (GS-MMC) operates in the dc voltage control mode. Each pole of the MMC features a dc smoothing reactor $L_{dc}$ set at 50 mH. For the sake of simplicity, the offshore wind farm and the onshore grid are modeled as ideal current and voltage sources in the simulation, respectively.

The key parameters for MMC control and dc cables are provided in Tables I and II, respectively. For the circulating current feedforward control, $K_v$ is set to 7, and $\omega_c$ is designated as $2\pi 5$.

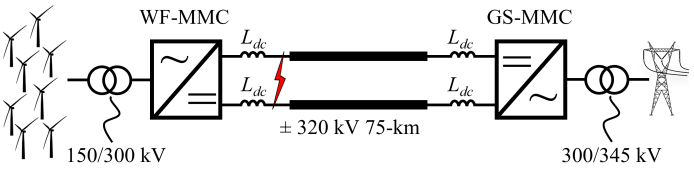


Fig. 9. Single-line diagram of the HB-MMC based symmetrical monopole HVDC transmission system

TABLE I
Control Specifications for WF-MMC and GS-MMC

| Control Mode | $K_p$ | $K_i$ | $K_d$ |
|---|---|---|---|
| dc voltage control | 0.0065 | 0.2 | NA |
| ac current control | 22.2 | 27915.5 | 7.85 |
| circulating current control | 44.4288 | 55830.9 | 31.42 |
| phase-locked loop | $1.48\times10^{-4}$ | 0.0093 | N/A |
| ac voltage control | 0.5 | 54.4 | N/A |
| ZSCC control | 44.4288 | 55830.9 | N/A |
| energy control | $1.04\times10^{-4}$ | 0.0098 | N/A |

TABLE II
Parameters of the ±320 kV 75-km dc cable

| Parameter | Series Resistance | Series Inductance | Shunt Capacitance |
|---|---|---|---|
| Values (per km) | $1.39\times10^{-2}$ Ω | $1.59\times10^{-4}$ H | $2.31\times10^{-7}$ F |

At $t$ = 1 $s$, a permanent pole-to-pole fault occurs at the dc bus of WF-MMC, specifically between the dc smoothing reactor and dc cables. For illustrative purposes, the SM

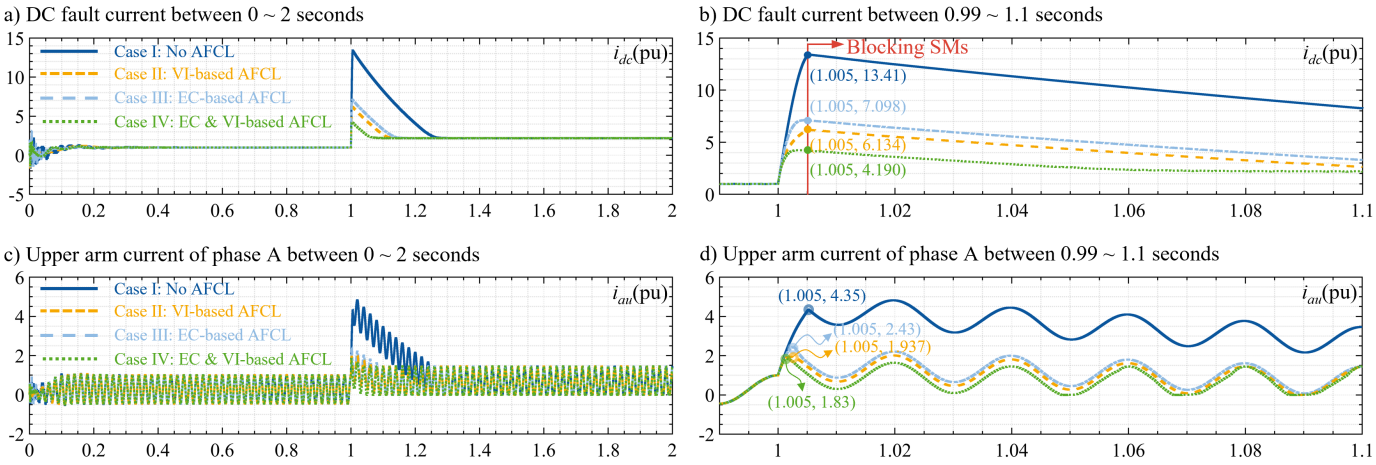


Fig. 10. Comparison of simualted responses of MMC: a) dc current of WF-MMC and its zoom-in view in b); c) upper arm current of phase A and its zoom-in view in d).

blocking operation is manually triggered at 1.005 *s*, and no DCCB tripping is implemented in the case studies. It should be noted that, in a practical scenario, the DCCB tripping-based protection is preffered more than the SM's blocking action . To demonstrate the effectiveness of the proposed VI-AFCL and EC-AFCL methods, the simulation is conducted under the following four scenarios:

- Case I: No active fault current limiting control is implemented, and fault current limitation solely depends on the 50 mH dc smoothing reactor on each pole of MMC (marked as 'No AFCL')
- Case II: The VI-AFCL control is enabled, while the EC-AFCL control is deactivated (marked as 'VI-AFCL')
- Case III: The EC-AFCL control is conducted, while the VI-AFCL is disabled (marked as 'EC-AFCL')
- Case IV: Both VI-AFCL control and EC-AFCL is enabled (marked as 'VI & EC-AFCL')

### *B. Simulated Responses*

The Fig. 10 illustrates the simulated dc current responses along with the upper arm current of phase A for the WF-MMC. The solid blue line represents the responses for Case I, where the MMC operates without any AFCL. The dashed yellow line corresponds to the responses for Case II, in which only the VI-AFCL is utilized. For Case III, where only the EC-AFCL is employed, the responses are indicated by the dashed light blue line. Lastly, the responses for Case IV, where both VI-based and EC-AFCLs are implemented, are represented by the dotted green line.

As displayed in Fig. 10, the dc current $i_{dc}$ increases from 1 pu (steady-state peak) to 13.41 pu within 5 *ms* in Case I, simultaneously causing the upper arm current of phase A $i_{au}$ to rise to 4.35 pu. Such an immediate increase in the currents poses potential threats to the dc-side equipment (e.g., DCCB and surge arrestor) as well as the MMC's switching devices. In addition, considering that SM blocking is typically triggered when the arm current reaches 2 times the rated current of IGBTs [11], the MMC with no AFCL in practice will block the SMs before the time that DCCB can interupt the fault current [19]. Blocked SMs, as mentioned earlier in the introduction, challenge the recovery process. Case II and III, employing VI-AFCL or EC-AFCL, limit $i_{dc}$ to 7.098 pu and 6.134 pu at 1.005 *s*, respectively, achieving a reduction of 47. 07% and 54. 26% in the dc fault current. These results show the effectiveness of both methods in fault current limiting without requiring the enlargment of dc smoothing reactors or the installation of additional physical fault current limiters. In Case III, the upper arm current peaks at 2.43 pu, exceeding the 2 pu threshold; thus, in practice the MMC will still trigger the SM blocking. In contrast, the exclusive application of VI-AFCL in Case II restricts the maximum upper arm current to 1.937 pu at 1.002 *s*, showing the desired effect in preventing blocking SM prior to DCCB interruptions if used in a practical scenario. As illustrated in Fig. 10 b) and d), $i_{dc}$ at 1.005 *s* in Case IV is reduced by 31.7% compared to Case III, and the peak $i_{au}$ occurs at 1.001 *s* with a value of 1.83 pu. This can be attributed to the bypassing of all SMs in the upper arm of phase A within 1 *ms* due to the combined regulation of VI-based and EC-AFCL. The simulation results for Case IV demonstrate that the hybrid EC- and VI-AFCL provides a better fault current limiting effect compared to the individual application of each AFCL.

Fig. 11 depicts the sum of the submodule capacitor voltages per arm for each case. In Case I, given the ac votlage control and CCSC act as their steady-state condition right after the fault occurs, all SMs across the six arms are alternatively inserted into the fault circuit. This causes a significant drop in sum capacitor voltages in all six arms until the SMs are manually blocked at 1.005 *s*. For Case II, despite a decrease in the sum capacitor voltages before the SM blocking, the drop is effectively mitigated by the VI-AFCL. As a result, the sum capacitor voltages remain within the range of $0.81 \sim 1.07$ pu. In Case III, depending on the control signal generated by EC-AFCL and the instantaneous value of the modulation index per arm at the time of the fault (see (14)), a portion of the SMs across the six arms are bypassed within $1 \sim 2$

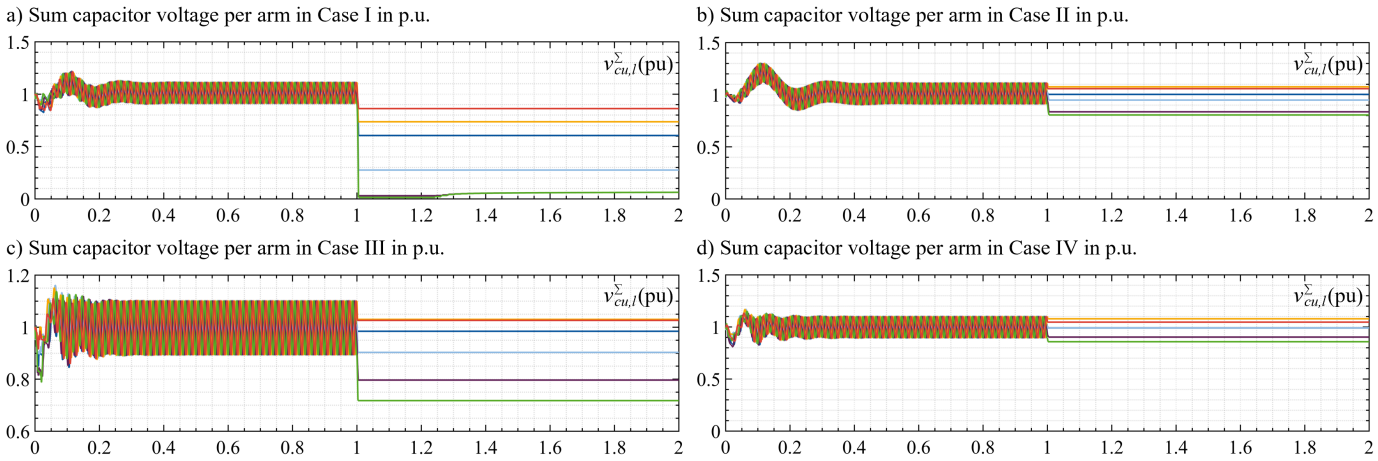


Fig. 11. Simualted responses of sum capacitor voltages of six arms in each cases.

*ms*, maintaining a higher sum capacitor voltage. However, for certain arms, the SMs are not completely bypassed until they are blocked, making the discharging process of the SMs in that arm lasting 5 *ms*. Even so, due to the effect of EC-AFCL, the number of discharged SM capacitors is limited, and the sum capacitor voltages remain within the range of $0.72 \sim 1.03$ pu. In Case IV, thanks to the regulation of both AFCLs, all SMs across six arms are bypassed after 1.003 *ms* (note that only SMs in the upper arm in phase A are bypassed at 1.001 *ms*), maintaining a higher sum capacitor voltage compared to Case II, within the range of $0.86 \sim 1.08$ pu. These simulation results further confirm the efficacy of the AFCL methods in limiting the discharge of the SMs' capacitors. Additionally, the ability to maintain a high voltage level in each arm could accelerate the recovery process.

## VI. Conclusion

This study presents two novel active fault current limiting methods, specifically using circulating current feedforward to introduce virtual arm impedance, and using energy control to automatically minimize the number of submodules that get discharged during a pole-to-pole fault. In addition, these methods do not require fault detection, thus avoiding the triggering delay, and the fault current limiting effect is adaptive to the rising rate of the fault current. The effectiveness and performance of the proposed AFCL methods are verified by EMT simulations.

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