SPOV Mechanism with Inverter-Based Distributed Energy Resources

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Abstract – Ground fault overvoltages can occur on 4 wire distribution feeders when distributed energy resources are unintentionally islanded with customer load and a phase to ground fault. The behavior of inverter-based distributed energy resources (IBDERs) is different than spinning machines under these conditions. In addition, IBDERs typically include internal fast Self Protection Over-Voltage (SPOV) which results in a cease-to-energize condition when the circuit voltage exceeds certain limits. This paper shows how the SPOV mechanism is effective in mitigating overvoltages to acceptable levels based on the 1547-2018 TrOV curve when installed with a wye-grounded / wye-grounded step up transformer.

Acronyms and Abbreviations

CHIL	Controller hardware in the loop
DER	Distributed Energy Resources
GFOV	Ground Fault Overvoltage
GLR	Generation to Load Ratio
GTR	Grounding Transformer
IBDER	Inverter-Based Distributed Energy Resources
LROV	Load Rejection Overvoltage
SLG	Single Line to Ground
SPOV	Self Protection Overvoltage
TrOV	Transient Overvoltage

I. Introduction

Increased penetration of inverter-based distributed energy resources (IBDER) has brought a renewed focus on the integration of distributed energy resources (DER) into existing utility distribution systems. The behavior of IBDERs during abnormal system conditions is vastly different than that of rotating machines. A major difference is that a grid-following IBDER acts as a current-controlled power source, not a voltage-behind-impedance source like a rotating machine.

Single line to ground (SLG) faults are one example of an abnormal system condition. SLG faults account for over 75% of all power system faults and can result in an overvoltage of up to 173% on the unfaulted phases. This overvoltage is referred to as ground fault overvoltage (GFOV) and is shown in Figure 1. When the DER is islanded with utility customers and the SLG, the overvoltage is a concern in the time period after the utility circuit breaker opens and before the DER ceases to energize.

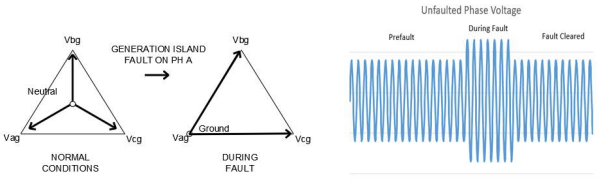


Figure 1 - Ground Fault Overvoltage Neutral Shift

Historically, a supplemental ground source would be used on a 4 wire distribution circuit to limit the coefficient of grounding to below 80% and the magnitude of the overvoltage to below 139%. When used with rotating machines, the calculation of the supplemental ground source is based on $X_0/X_1 \leq 3$ and $R_0/X_1 \leq 1$ criteria detailed in IEEE standard C62.92.2 [1].

However, IBDERs do not operate the same way as the rotating machines, and they do not have the physical mechanism that leads to overvoltages in rotating machines. IEEE Standard C62.92.6 [2] was developed to address current-regulated sources and is based on sequence component calculations using the impedance of phase to ground loads to complete the zero sequence current path.

IBDERs also typically include internal fast overvoltage protection mechanisms designed primarily to protect the inverter itself from damaging transients. These mechanisms are referred to as Self Protection Over-Voltage (SPOV). They have the added benefit of causing the inverter to cease energization very quickly (usually in hundreds of microseconds) when the instantaneous circuit voltage exceeds certain limits. These SPOV mechanisms thus can mitigate transient overvoltages (TrOV) including both GFOV and load-rejection overvoltage (LROV). The impact of the SPOV was not included in the C62.92.6 calculations.

The use of a generator step-up (GSU) transformer with a WYE-grounded / wye-grounded (YG:yg) winding configuration provides a continuous zero sequence path. This allows the IBDER to "see" all three sequence components of any abnormal voltage on the utility circuit. Therefore, the duration and magnitude of any transient overvoltage can be limited by the SPOV protection. When installed with an ungrounded wye or delta winding the zero sequence voltage will not be able to be measured by the IBDER when sensing phase to ground voltages, and these cases are not in the scope of this paper.

The principal focus of this work is to use control hardware in the loop (CHIL) simulations of the IBDER in a real time environment to show that a grounding transformer is not necessary when a YG;yg GSU transformer is used. Grounding transformers can lead to negative impacts on distribution circuits, such as desensitizing the utility ground relaying, increased arc flash energy and blinding of the DERs to single phase open circuits [3].

The CHIL approach adds complexity but it ensures that the response of the inverter is accurate for the positive, negative and zero sequence current components. CHIL simulation allows the use of actual controllers without requiring the manufacturer's proprietary design details.

II. System Model

The main purpose of this project was to perform a CHIL simulation to investigate inverter-driven TrOV during SLG faults. A Typhoon HIL 604 simulator coupled to an IEEE 1547 compliant ASGC controller was utilized. The simplified system schematic of the CHIL configuration is shown in Figure 2. The utility source was defined with an 8000 A available fault current, and the DER step up (GSU) transformer was a Wye-Ground / wye-ground winding. When the grounding transformer (GTR) is inserted in the model, it is sized at 500 kVA. Industry typically uses either a zigzag or Yg-△ transformer for supplemental grounding. A grounded wye / delta, 500 kVA GTR was used during this simulation. The size of the GTR is significantly larger than would be typically used to provide a very low zero sequence impedance and eliminate any concerns that the GTR was undersized.

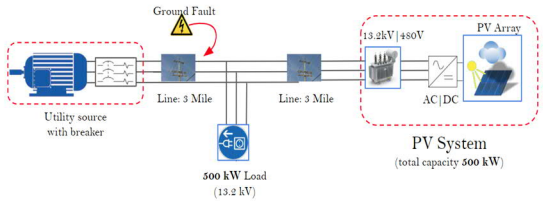


Figure 2: Model Schematic of the Simulation

For all the simulations, a three phase three level T-type inverter block was used for simulations. The T-type is also the recommended topology by Typhoon HIL's manual for smaller capacity systems with PV units. This architecture will allow for a grounded connection on the transformer secondary and is shown in Figure 3. Large central inverters typically use a standard H bridge topology which will not allow for a grounded wye connection and would not be adequate for the purpose of the project.

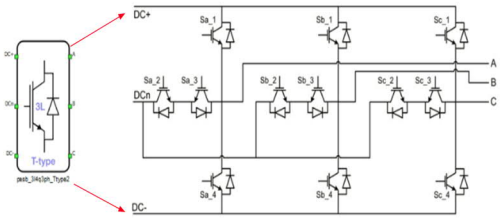


Figure 3: Three-phase three-level T-type inverter block diagram

Real time CHIL (or HIL) configuration enables the system for faster simulations. The runtime for a 1 second long simulation takes exactly 1 second in the RT-configuration (CHIL or HIL). This simulation could take minutes to execute in an offline simulation environment. This approach also ensures that the response of the inverter is accurate. Without CHIL the use of a proprietary black-box manufacturer-specific model is required. CHIL simulation allows the use of actual controllers without requiring these design details. The inverter anti-islanding was disabled for the simulations to achieve a longer and more stable islanded time period.

Initial simulations were performed with a generation to load ratio (GLR) at 1.0. This value was selected as the focus is on GFOV, with higher GLR values the LROV will begin to dominate.

The corresponding phase voltages are shown in Figure 4 below. It can be seen that there is an overvoltage of 8-9% after the utility disconnects. This is not unexpected as the maximum current output of the inverter would slightly increase the current through the fixed load impedance. The simulations resulted with the inverter disconnecting within 3 cycles of the circuit breaker opening. The fast disconnect is the result of an unmatched kVAR load. The timing is shown in Figure 5.

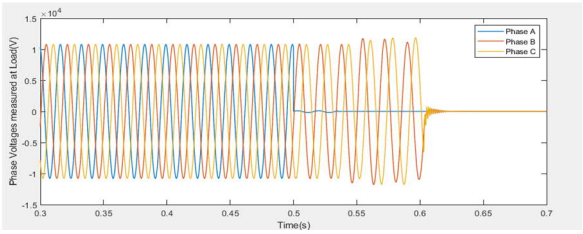


Figure 4: GFOV simulation at Generation to load ratio (GLR)=1.0

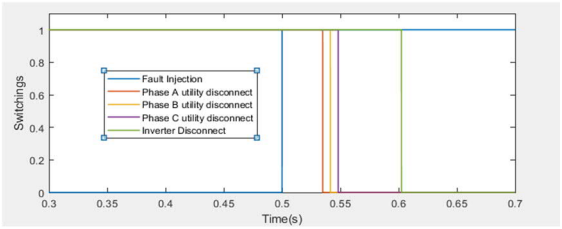


Figure 5: Initial GFOV simulation

During the 3 cycles the frequency is not stable at 60 Hz and the sequence components were not at fixed angles with each other due to the frequency movement. A fundamental assumption in applying sequence analysis is that the angles are not rotating with respect to one another. To stabilize the angles and the frequency, a capacitor bank was placed in parallel with the load. This capacitance accounts for the inductance in the GSU transformer. Multiple iterations showed the optimal capacitance to be 1.75 μF per phase. Figure 6 shows that the inverter was able to sustain in the islanded condition for 10-12 cycles after the tuning of the capacitor bank. This additional time allows a steady state period to assess the overvoltage as well as a stable 60 Hz frequency which allows for sequence component analysis. This capacitance value was adjusted when the GTR was included in the model.

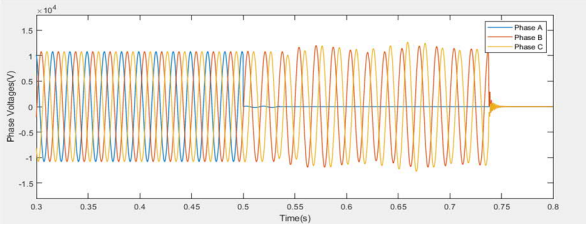


Figure 6: GFOV simulation with tuned capacitor bank, GLR=1.0

Figure 7 represents the angle between the positive and negative sequence components of the inverter current when GLR=1.0. The angle between the positive and zero sequence components of the inverter current were not considered because the magnitude of the zero sequence current was at zero and thus angle computation was mathematically not feasible. It is important to note that the relative angle between the sequence components of the inverter currents start oscillating around 0.7 second. Numerical observations used for sequence component analysis were taken between 0.6-0.65 second time period to capture values when the relative angles between the post-fault sequence components of the inverter current were relatively constant.

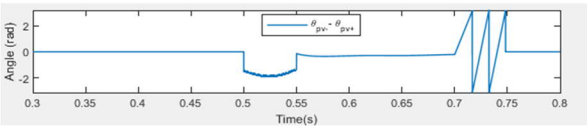


Figure 7: Inverter current sequence component angle difference

III. Initial Simulation with GTR

The sequence components of the inverter currents in the simulations align with the expected results. Grid connected transformerless inverters such as the one modeled do not typically provide zero sequence current. Off-grid inverters may provide zero sequence current to provide for unbalanced loads and are not included in this report. The inverter negative sequence current is highly variable based on the inverter design. This creates concern from protection engineers as modeling software requires this value.

As can be shown in Figure 8, the inverter phase currents are slightly higher than nominal and the sequence components match the expected values as shown in Figure 9.

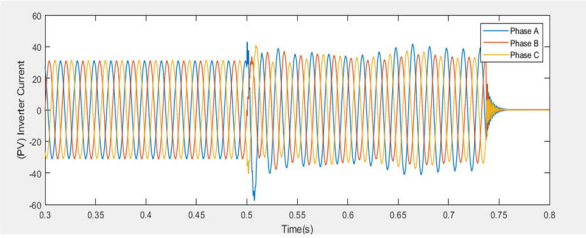


Figure 8: Inverter Current (3 Phase), GLR=1.0

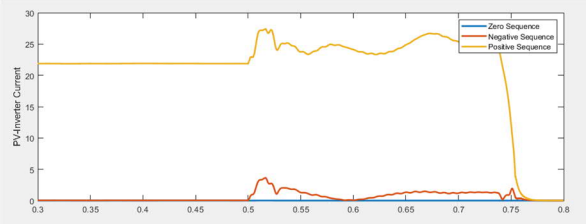


Figure 9: Inverter Current (Sequence Components), GLR=1.0

Figure 10 shows the inverter sequence components with a GTR installed. The increase in negative sequence current should be noted.

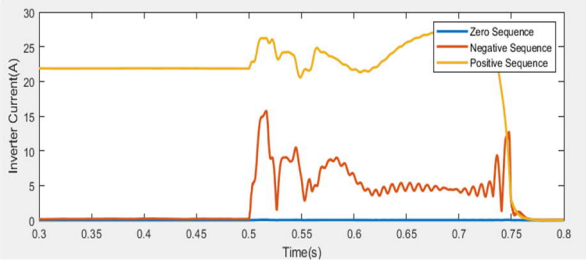


Figure 10: Inverter current (sequence components), GLR=1.0 with GTR

Figure 11 shows sequence-network diagrams of the island with the SLG fault, without (a) and with (b) the GTR. In both cases the inverter is shown as a positive sequence current source with an open circuit in the zero sequence network. The inverter negative sequence current behaves as a current flowing through a variable impedance. This variable impedance represents the negative sequence component of the inverter and it includes the actual filter impedance and the synthetic impedance of the controller.

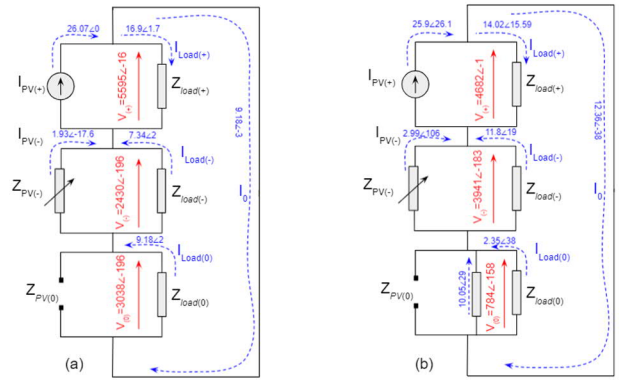


Figure 11: Sequence components

Figure 11(b) shows the GTR will lower the zero sequence impedance which results in the increase of the zero and negative sequence currents. It also shows that only the zero sequence network is modified by the GTR installation. The impedance of the negative sequence network is not changed. The increase in the zero/negative sequence current results in an increase in the negative sequence voltage.

In this scenario the inverter is current limited and behaving as a Thevenin equivalent voltage across the positive sequence load impedance. Figure 12 rotates the sequence component network, showing that with only a positive sequence current source, the sum of the negative and zero sequence voltages will equal the positive sequence voltage, assuming a bolted fault. Therefore, further reduction of the zero sequence voltage must result in a higher negative sequence voltage.

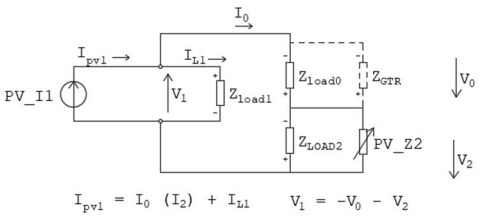


Figure 12: Inverter Based Sequence Component Network

The comparison of the positive and negative sequence components after the GTR is inserted shows the positive sequence voltage may be reduced slightly and the negative sequence values will increase. Recall the system was modeled with a GTR that provided a small zero sequence impedance which almost removes any zero sequence voltage contribution to GFOV. Figures 13-14 show the comparison.

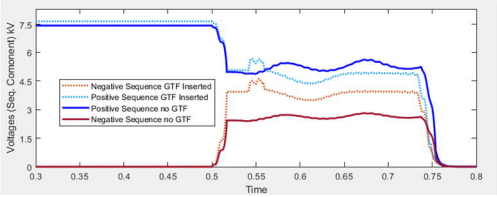


Figure 13: Voltage Sequence Components, GTR Comparison

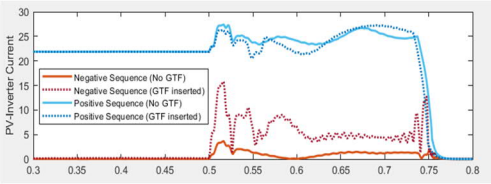
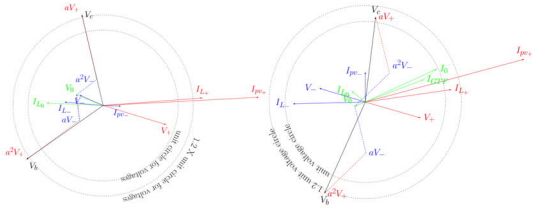


Figure 14: Inverter Current Sequence Components, GTR Comparison

The results show that the negative sequence voltage was a significant contribution to the TrOV. Since the addition of a GTR does not affect the negative sequence network, it cannot completely mitigate the phase overvoltage from the IBDERs.

IV. Higher Generation to Load Ratios

To examine the interaction of GFOV and LROV, a GLR of 1.2 was simulated. The maximum phase overvoltage is expected to increase with a higher GLR value. This trend is expected and similar results were documented in IEEE Standard 62.92.6. For a GLR = 1.0, the overvoltage was insignificant (<10%). For low GLRs below 1.0, some undervoltage is also expected due to the load reducing the resulting phase voltages. Figure 15 shows, by vector representation, how the GTR decreases the V_0 and increase the V_2 magnitude resulting in a minimal change on the V_b magnitude overvoltages for generation to load ratio of 1.2. All voltages are below the 138% threshold associated with effective grounding. It is important to note that the positive sequence voltage has increased apart from the significant negative sequence component. Thus, the resultant overvoltage has both GFOV and LROV components.



15(a) –No GTR 15(b) - GTR

Figure 15: Phasor Diagram Representation for GLR = 1.2

Table 1 shows the overvoltage values with different GLR values. The introduction of the GTR improves the situation of GFOV marginally. The table is limited to a maximum GLR of 1.2 as the inverter's 1.3 pu SPOV setting ceases operation on the higher phase overvoltages.

A closer observation of Table 1 reveals that the difference in overvoltage by incorporating a GTR gets less significant with increasing GLR. This can be explained by the fact that, with increasing GLR, the negative sequence component of the voltage keeps increasing, and the GTR can only modify the zero sequence network. Thus, for higher GLRs the overvoltage improvement provided by the GTR is minimal. These were simulated with a SPOV = 1.3.

Table 1: GLR Impact on Overvoltage

GLR	Over Voltage (No GTR)	Over Voltage (GTR)	Delta
0.6	0.67	0.62	5%
0.7	0.78	0.73	5%
0.8	0.88	0.84	4%
0.9	0.990	0.935	5.5%
1.0	1.093	1.071	2.2%
1.1	1.178	1.15	2.8%
1.2	1.296	1.265	3%

V. SPOV Mechanism

The primary function of the SPOV is to protect the inverter itself from damaging transients. It has the added benefit of causing the inverter to stop output when the IBDER's instantaneous terminal voltage exceeds the voltage limit. The SPOV is further defined in IEEE Std. 92.62.6 pp 25:

"The second mechanism is that most (but not all) inverters have a Self-Protection Overvoltage (SPOV) mechanism that operates on peak (not RMS) voltages and causes the inverter to cease output very quickly, typically in 1 ms or less, if the instantaneous voltage increases beyond a pre-determined limit"

The previous simulations were performed with the limit set to 1.3 per unit, and therefore the inverter is expected to disconnect when the overvoltage exceeds 130%. The SPOV threshold is fixed in the Typhoon HIL 604 and ASGC controller and there was no means to disable or change the setting, which limited the maximum GLR at which tests could be run. In order to broaden the range of GLRs that could be tested, a new firmware was provided by the inverter manufacturer to allow for a 600 Vac interconnection voltage. The SPOV voltage reference was then configured to use the 600 Vac level, effectively raising the 1.3 pu level to 1.625 pu (600*1.3/480).

With this change, the inverter will stay connected for a higher voltage as the SPOV is not triggered. Figure 16 shows the lower SPOV setting which disconnects the inverter quickly.

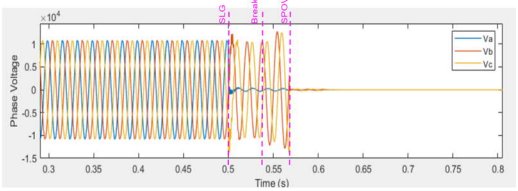


Figure 16: SPOV Mechanism Enabled (at 1.3)

The same simulation was carried out with the new firmware and the results are shown in Figure 17. The SPOV did not trigger in this case (the inverter tripped on overfrequency).

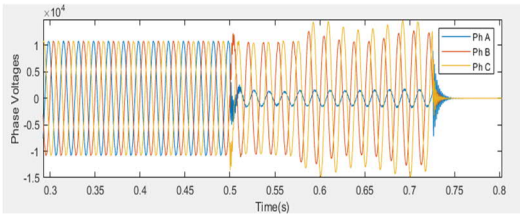


Figure 17: SPOV Mechanism Enabled (at 1.625)

VI. Ungrounded Loads

The main challenges with the implementation of the calculations in IEEE 62.92.6 is the determination of the percentage of phase to ground connected load. Due to customer three phase motors and potentially delta/wye step down transformers in commercial and industrial locations, this value is sometimes difficult to determine. A large percentage of delta connected load will increase the effective total zero-sequence impedance of the load, leading to higher zero-sequence voltages and higher GFOVs. Therefore, simulations were run with varying percentages of delta connected loads. The capacitor bank was re-tuned in each case.

Figures 18-19 show the system without a GTR and an increasing amount of delta connected load. As expected, the maximum phase to ground voltage increases as the delta connected load increases. Notice the inverter will not sustain the 75% level of delta load. The data was developed with a SPOV of 1.625 to identify the worst case with delta connected loads. With the lower SPOV setting the inverter immediately ceased to energize.

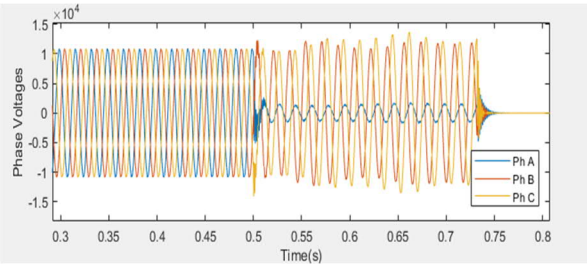


Figure 18: Voltages: GLR =1.0, Y=75%, △ =25%, no GTR

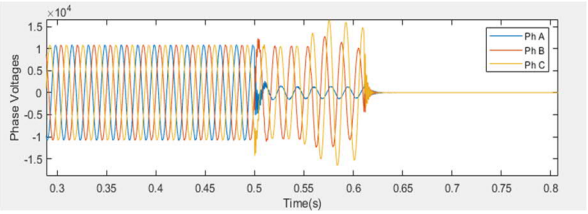


Figure 19: Voltages: GLR =1.0, Y=25%, △ =75%, no GTR

Using the higher SPOV setting, Table 2 summarizes the differences including a GTR with various percentages of delta connected load. As expected, the GTR's reduction of the unfaulted phase overvoltages increases as the fraction of delta load increases. The reader should recall that this GTR is especially large (low-impedance) to emphasize and better demonstrate the difference made by the GTR. However, even with the higher SPOV setpoint and without the GTR the overvoltage remains below the 139% effectively grounded COG standard for up to 50% delta load. This level which would be considered very high for most 4 wire effectively grounded circuits.

Table 2: Various delta load percentage, GLR=1.0 (SPOV = 1.625)

Unfaulted Phase Overvoltage	Y = 100%| △=0%	Y = 75%| △=25%	Y = 50%| △=50%	Y = 25%| △=75%
Overvoltage without GTR	1.089	1.19	1.32	1.48
Overvoltage with GTR	1.05	1.07	1.07	-------

The results in Table 2 were obtained with the higher SPOV threshold. Further testing was performed to understand the impact of higher percentages of delta loads with increasing GLR levels. The results from these cases and the two SPOV settings are shown in Figure 20. A higher percentage of delta loads will result in disconnection of the inverter at a lower GLR ratio. The results show that the lower SPOV setpoint will prevent the inverter from remaining online for higher GLR values.

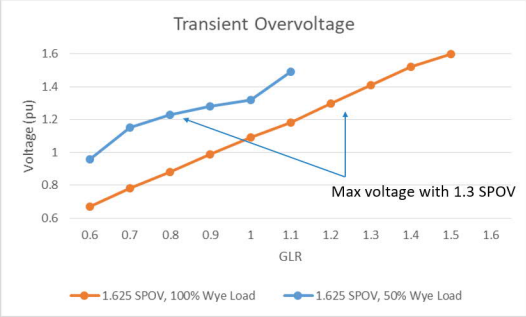


Figure 20: Overvoltages with varying GLR, SPOV setting and Phase Connected loads

Therefore, it is concluded that the SPOV mechanism is effective for mitigating overvoltages for both delta and Y connected loads, as well as for GFOV or LROV conditions.

VII. Cumulative Instantaneous Voltage Standards

Hawaiian Electric (HECO) began to require inverter TrOV-2 certification in 2018 to address their concerns with LROV. The LROV testing requirements were developed after UL1741SA and were listed as HECO TrOV-2 certification [4]. As this test was not included in UL1741SA, HECO required manufacturers to test and submit the inverter test run raw data for compliance verification. Any inverter connected to the HECO grid needed to pass this testing. The HECO overvoltage curve is shown in Figure 21. The same TrOV-2 certification levels have been used by utilities outside of Hawaii.

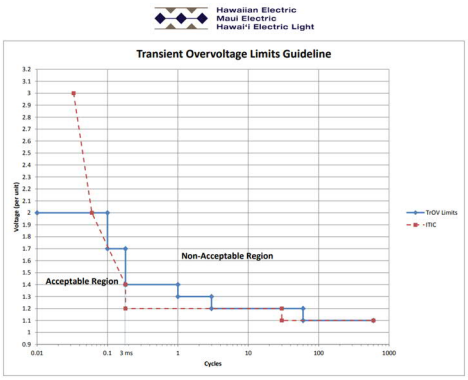


Figure 21: HECO TrOV Guideline

Similar to the HECO requirements, revisions in IEEE 1547-2018 [5] include requirements to define the cumulative instantaneous voltage limits for DER installations. The 75% delta load cumulative overvoltage is plotted vs. these limits in Figure 22. The plot shows that the lower SPOV setting was effective in preventing the limits of the curve to be exceeded. This plot utilized the worst overvoltage, Phase C to ground.

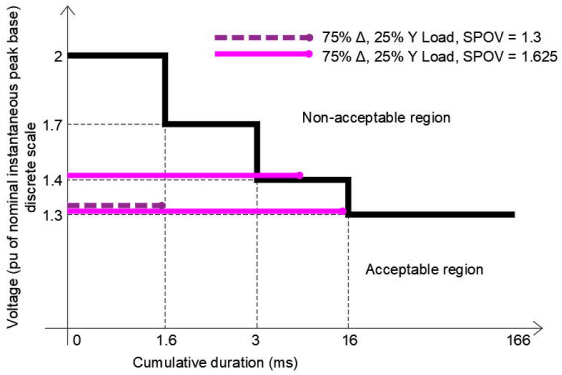


Figure 22: Cumulative Instantaneous Overvoltage

The waveforms for the two cases are shown in Figure 23 and Figure 24. The 1.4 pu voltage is approximately 15 kV. The time scales on these plots were shortened to clearly show how quickly the inverter SPOV function operates to minimize the overvoltage duration.

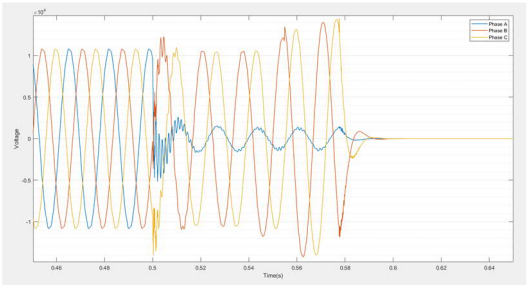


Figure 23: Lower SPOV Setting (1.3)

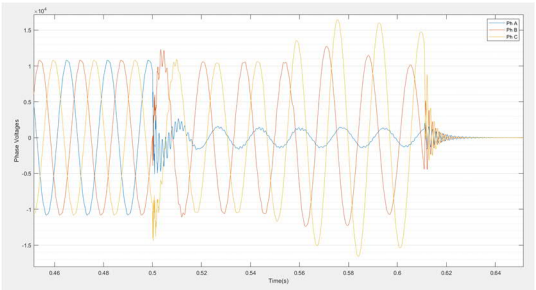


Figure 24: Higher SPOV Setting (1.625)

The certification in 1547.1 [6] splits the overvoltage requirements into LROV and GFOV test plans. The LROV test is required for UL1741SB certification and the test with a ground fault is listed as optional.

VIII. Conclusions

The results of this project support the theory that the SPOV function will mitigate TrOV during an SLG on a four-wire distribution

circuit when installed with a YG:yg interconnection transformer and for large fractions of delta load. The same function will also keep LROV below the TrOV curve in 1547-2018.

The analysis further demonstrates that a supplemental ground source will not completely eliminate IBDER-driven TrOV during SLG faults as only the zero sequence impedance is reduced. The zero sequence component of the TrOV only dominates at lower GLRs, where the LROV is actually negative and thus TrOV is less of an issue. At higher GLRs, where TrOV is an issue, the negative sequence component of LROV dominates. The GTR does not mitigate for that condition.

Without the supplemental ground source on the utility system, the negative impacts will not be present which include issues with increased arc flash incident energy, single phase open detection and the desensitization of utility ground relaying.

Additional benefit of the project was to further validate C62.92.6 as the symmetrical components analysis were in agreement. One of the main challenges in the C62.92.6 calculations is the determination of the inverter negative sequence current and the amount of phase to ground connected load. With the presence of the SPOV function, the specifics of these values become less important as the inverter will sense and prevent an overvoltage without requiring a specific negative sequence impedance to be identified.

IX. Acknowledgements

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X. References

[1] IEEE Std C62.92.2, IEEE Guide for Application of Neutral Grounding in Electrical Utility Systems, Part II – Grounding of Synchronous Generator Systems.

[2] IEEE Std C62.92.6, IEEE Guide for Application of Neutral Grounding in Electrical Utility Systems, Part VI – Systems Supplied by Current-Regulated Sources.

[3] M. Ropp, D. Schutz, S. Perlenfein, C. Mouw, “Single-Phase Open Detection in the Presence of Distributed Energy Resources”, Western Protective Relay Conference, October 2017, 9 pgs.

[4] Hawaiian Electric Grid Supportive Utility-Interactive Inverter Qualification Requirements, March 12, 2018 https://www.hawaiianelectric.com/documents/products_and_services/customer_renewable_programs/grid_supportive_utility_inverter_certification_req_20180312.pdf

[5] IEEE Std 1547-2018, IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces.

[6] IEEE 1547.1-2020 - IEEE Standard Conformance Test Procedures for Equipment Interconnecting Distributed Energy Resources with Electric Power Systems and Associated Interfaces

XI. Biographies

Michael Ruppert received his Bachelor’s and Master’s degrees in Electric Power Engineering from Rensselaer Polytechnic Institute in Troy NY. He has over 25 years of experience in power engineering and renewable energy which began in the System Protection Section at Central Hudson Gas & Electric and currently is the President and Principal Engineer of JEM Engineering in Poughkeepsie, NY. Mike is a Senior Member of the IEEE and is a registered Professional Engineer in multiple states.

Michael Ropp was born on Ellsworth AFB, South Dakota, in 1967. He holds a BA in Music from the University of Nebraska-Lincoln and the MSEE and PhD from the Georgia Institute of Technology. Dr. Ropp is the Principal Engineer of Northern Plains Power Technologies, Brookings, SD. His research interests include computer modeling of power systems; power system dynamics and control; power system protection; low-inertia power systems; power electronics; distributed energy resource integration; and electric transportation. Dr. Ropp is a registered Professional Engineer in SD and HI.

Luigi Vanfretti received the M.Sc. and Ph.D. degrees in electric power engineering from Rensselaer Polytechnic Institute, Troy, NY, USA, in 2007 and 2009, respectively. He was an Associate Professor with Rensselaer Polytechnic Institute, in 2017, where he is currently developing his laboratory and research team ALSETLab. He was an Assistant Professor, and an Associate Professor (tenured) and a Docent with the KTH Royal Institute of Technology, Stockholm, Sweden, from 2010 to 2013 and from 2013 to 2017, respectively, where he led the SmarTS Lab (a research group). He was with Statnett SF, the Norwegian transmission system operator, from 2013 to 2016, as a Special Advisor with the Research and Development Department and as a Consultant from 2011 to 2012 and in 2017. He currently serves as a consultant to Dominion Energy, Virginia, the SuperGrid Institute, Lyon, France, and CENACE, Ecuador. His research interests include synchrophasor technology applications, and cyber-physical power system modeling, simulation, stability, and control.

Prottay Adhikari is currently a doctoral student in the Department of Electrical, Computer, and Systems Engineering at Rensselaer Polytechnic Institute (RPI). Prior to joining RPI, Prottay completed his bachelor's in Electrical Engineering from IIEST Shibpur and Masters' in Electrical Engineering from IIT Bombay while working as a research assistant at EmSys Lab. He worked for ARM from 2016 to 2017. Prottay works in ALSET Lab and his current research lies on the interface of Smart Grid Technology and Embedded Systems. He spent the summer of 2021, as a research intern for Electric Power Research Institute (EPRI).