A Reconfigurable Hardware Prototype for Pre-compliance Testing of Phasor Measurement Units

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Abstract—**Pre-compliance tests are intended to be used to assess Phasor Measurement Unit(PMU)s' performance during their design and implementation before sending them for certification or using them for grid dynamic measurements. Methodologies for pre-compliance testing of PMUs based on the dynamic requirements of the IEEE C37.118.1-2014 standard are discussed and reported in recent literature. However, these tests are mostly performed through software simulations and there are limited test-hardwares available. To address this issue, a simple reconfigurable hardware prototype is proposed in this paper. The implementation is carried out using National Instruments' Compact RIO family of reconfigurable hardware and it provides a fast, time-synchronous and efficient way to perform all the compliance tests on the PMU under investigation.**

Index Terms—**Phasor Measurement Units, C37.118.1-2014 standard.**

I. INTRODUCTION

A. Motivations

The IEEE Std C37.118-2011 and its 2014 update specifies permissible error limits for PMUs under both normal and dynamic conditions. The standard phasor estimation algorithms are designed to work with perfect time invariant sinusoidal set of waveforms. However, most of those phasor estimation algorithms are not robust enough to deal with dynamic conditions. Thus, different tolerances are specified by the standard under nominal and dynamic conditions. According to the 5.5-5.7 subclauses of the standard, the PMU is expected to perform sufficiently well under certain test conditions. However, it is unrealistic to emulate these test conditions in the real-life power system. The authors in [1] incorporated these test-scenarios by feeding a PMU Software model with standard waveform files. We generated the same test scenarios in a low-voltage hardware prototype and tested two PMU systems with them. The main motivation of the current work is to provide a test-hardware prototype which can be programmed and used to test any PMU under certain conditions.

B. Related Works

Authors in [1] suggested and specified all the tests that needs to be carried out to characterize the performance of PMUs under both steady-state and various dynamic conditions in pre-compliance testing. These test conditions were provided to a PMU in [1] through standard waveform files/.csv files. In the current work we propose a hardware prototype which provides similar voltage and current waveforms in real time. Authors in [2] reported some important results of steady state compliance testing of phasor measurement units (PMUs) based on a standard industrialized relay-test set. [7] also reports similar experimental results, using a dedicated test-signal generator. However, these implementations do not include the dynamic compliance tests. In [5], all the compliance tests were performed using a Doble 6150 advanced relay test-set. Virtual Instrumentation (VI) based testing for PMUs were proposed in [4]. However, this work did not cover all the required pre-compliance tests suggested by [1]. The authors of [4] did elaborate experimental analysis for only one of the pre-compliance tests. Because, all the testing for PMUs need to be time-synchronized, time-requirements are crucial for these tests. This was explored by the authors in [6]. Overall, the literature survey revealed the lack availability for a completely autonomous and programmable test-suite for testing PMUs.

C. Contributions of this work

- A test-infrastructure is proposed. It uses low-voltage signals to validate the functionalities of a PMU under test. The test infrastructure is based on National Instruments' hardware.
- The test-hardware can be easily controlled by a user from the GUI-based software designed in LabVIEW.
- A prototype PMU is put under the tests (using our test-suite) and its performance is analyzed and compared with the others available in literature.

D. Structure of the Paper

In Section II, a brief review of the PMU compliance tests is presented. In Section III, the detailed description of the PMU-testing hardware is given. This section contains information about both the hardware and the software components of the proposed test-infrastructure. Special emphasis is given on the hardware components that were used to acquire the GPS signals. In the software section, the hierarchy of the source code is discussed, along with the monitoring tools used to oversee and capture the broadcasted PMU data. In section IV, the results of the PMU compliance tests (performed with the proposed test-hardware) by the PMU under test are reported.

II. PMU PRE-COMPLIANCE TESTING REVIEW

Broadly, there are four different pre-compliance tests as reported by [1], for which test conditions are briefly reviewed in this section.

- Steady-State test: Balanced three phase voltage of nominal frequency are provided to the PMU. The computed phasors must be within a specified limit set by the standard.
- Bandwidth test: In this test, sinusoidal amplitude and phase modulation is applied to a balanced set of three phase voltage and current waveforms. This can be mathematically expressed as below, where K_x is the amplitude modulation factor, K_a is the phase angle modulation factor, X_m is the amplitude of the signal, ω is the modulation frequency and ω_0 is the nominal frequency of the system.

$$X_1 = X_m[1 + K_x cos(\omega t)] \cos(\omega_o t + K_a cos(\omega t - \pi))$$

- Frequency Ramp test: A linear increase in the system frequency is provided. This increase is applied across all the three phases. Hence the positive sequence component of the system can be expressed mathematically as

$$X_1 = X_m cos(\omega_0 t + \pi R_f t^2)$$

  where X_m is the amplitude of the applied signals, ω_0 is the nominal system frequency and R_f is the ramp rate in Hz/sec.
- Amplitude/Phase Step Increase test: Sudden step change in phase and amplitude are applied to the signals and the response time, overshoot and delay time is determined in the PMU measurements. Mathematically the input signal for this test can be expressed as the following.

$$X_1 = X_m[1 + K_m f_1(t)] \times \cos(\omega_o t + k_a f_1(t))$$

  where X_1 is the positive sequence component of the signal, K_m is the step size in magnitude of signals, K_a is the step size in the phase of the signals.

III. PROPOSED TESTING INFRASTRUCTURE

Our basic testing infrastructure consists of hardware components and software components.

A. Hardware Description

The hardware is built on a National Instruments' compact RIO 9081 device with a NI-9263 voltage output module and a NI-9467 GPS acquisition module. The data acquisition for the GPS module and data transmission for the voltage output module is controlled by the code running on the Xilinx Spartan 6 FPGA that is the in-built (inside) the compact RIO 9081 device.

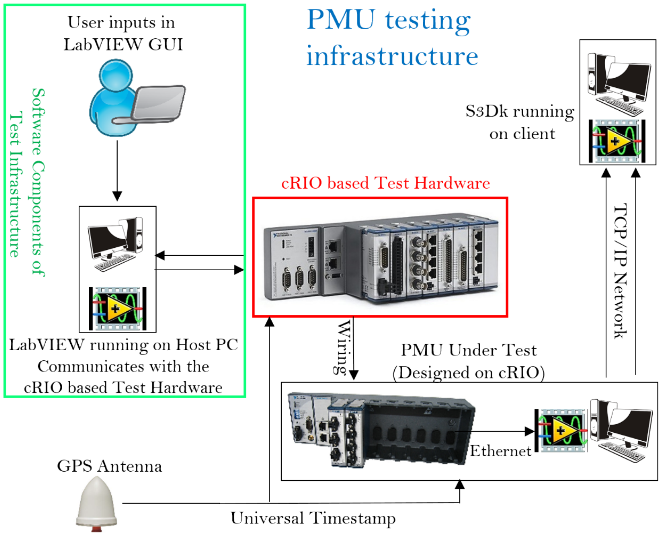


Fig. 1. PMU Testing infrastructure with all the Hardware (Red), Software (Green) components and the PMU Under test (Black)

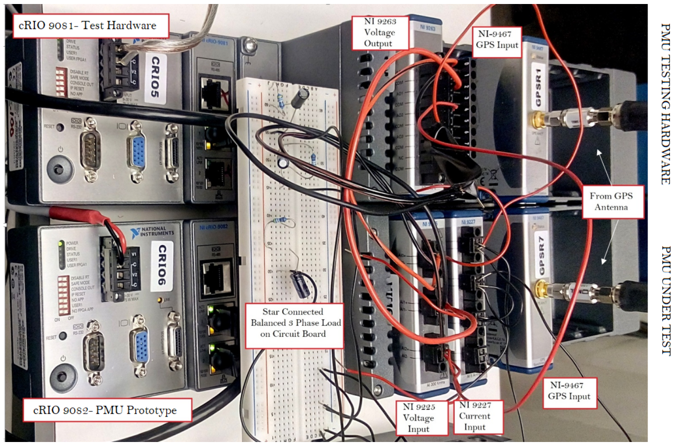


Fig. 2. PMU Testing Hardware Connected to the PMU Prototype

Figure 1 shows the hardware and software parts of the test infrastructure along with a PMU prototype, which is designed and implemented in a compact RIO 9082 device. The PMU algorithm implemented in the PMU prototype is National Instruments' proprietary design for phasor estimation, which is part of their advanced PMU development system [8]. To synchronize the test-hardware with the PMU, the universal GPS time-stamp which can provide an accurate time-stamp upto 10 ns range, was used. This range was set by the specifications of the C series module NI-9467. Both cRIOs 9081 and 9082 can access the GPS signal through the NI-9467 module. (Fig 2)

The PMU prototype under test includes a current input module NI-9227, a voltage input module NI-9225 and a GPS acquisition module NI-9467. The voltage input module is connected to the output of the test-hardware made with the compact RIO 9081. The output of the test-hardware is connected to a simple start-connected RC load. The NI-9227 current input module is used to sense the phase current in this load, which is processed by the PMU to compute current

TABLE I
SPECIFICATIONS OF THE PMU TESTING HARDWARE AND PMU UNDER TEST

Hardware	Voltage Rating	Current Rating	Time Accuracy
PMU Tester	0-10V (Output)	0-10mA RMS (Output)	up to 10ns
PMU Prototype	0-200V (Input)	0-5A RMS (Input)	up to 10ns

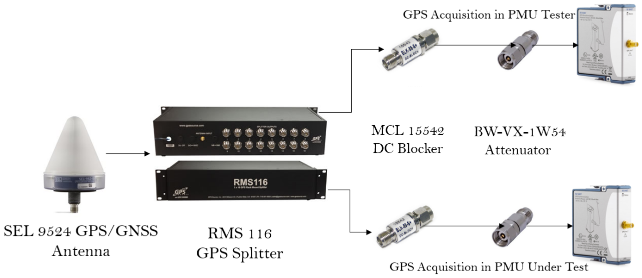


Fig. 3. Connection Diagram for GPS Signal Acquisition

estimates.

Figure 2 shows the compact RIO-based test-hardware connected to the compact RIO-based PMU prototype. Both of the compact RIO devices are receiving GPS signals from antennas via NI-9467 modules and attenuators. A three phased configurable voltage supply is configured using the NI-9263 module. On the bread-board a balanced 3 phase load is implemented using standard resistors and capacitors. For each phase a resistor of $1k\Omega$ and a capacitor $10\mu F$ was connected in series. The currents are measured from this load via the NI-9227 module by the compact RIO based PMU prototype.

The current and voltage specifications of the proposed test infrastructure and the designed PMU prototype under test are tabulated below. The voltage and current limits stated in columns 2 and 3 clearly exhibit that the PMU tester voltage and current limits are well within the that of the PMU prototype.

It can be seen from Figure 1 that a GPS antenna is used to provide timing information to both the PMU test hardware and the PMU under test. This connection requires a set of specific hardware as shown in Figure 3.

Connection Specifications for GPS Signal Acquisitions: In the current setup, a SEL 9524 GPS/GNSS antenna was used to obtain GPS signals. The antenna was connected to an RMS 116 GPS splitter since more than one GPS output are needed. To ensure that the GPS signal level from the RMS 116, is within the range of the NI-9467's input range, a DC Blocker and an attenuator were added to the connectors. All the connections were made with high quality LMR 400 cables.

A simple connection diagram for GPS signal acquisition system used in the lab is shown in Figure 3.

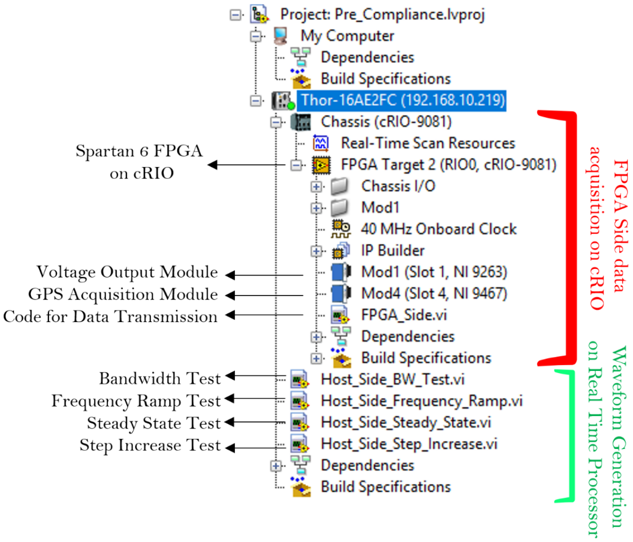
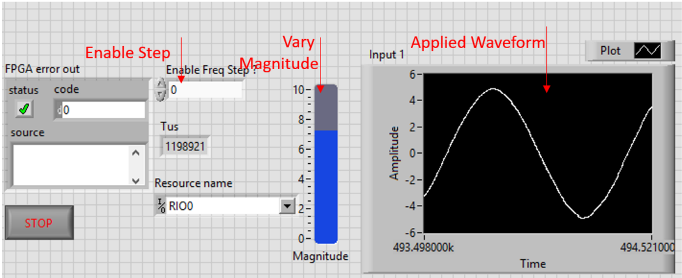

Project: Pre_Compliance.lvproj
My Computer
Dependencies
Build Specifications
Thor-16AE2FC (192.168.10.219)
Chassis (cRIO-9081)
Real-Time Scan Resources
FPGA Target 2 (RIO0, cRIO-9081)
Chassis I/O
Mod1
40 MHz Onboard Clock
IP Builder
Mod1 (Slot 1, NI 9263)
Mod4 (Slot 4, NI 9467)
FPGA_Side.vi
Dependencies
Build Specifications
Host_Side_BW_Test.vi
Host_Side_Frequency_Ramp.vi
Host_Side_Steady_State.vi
Host_Side_Step_Increase.vi
Dependencies
Build Specifications

Fig. 4. Organization of the testing software in LabVIEW including the real-time and FPGA dependencies



FPGA error out: status ✓, code 0

Enable Freq Step ? 0

Tus 1198921

Resource name RIO0

Fig. 5. Sample GUI to control/modulate a compliance test

B. Software Description

Figure 4 shows the detailed structure in which the test-hardware is programmed. Two programs run simultaneously on the compact RIO and they interact with each other. One of them runs on the FPGA and takes care of the GPS time-stamp acquisition and voltage signal transmission to the NI-9263 voltage output module. The host-side software VIs are used to generate those voltage signals. It can be seen from the figure that, we have four different codes for four different compliance tests discussed in the previous section.

Each of the four tests are controlled from their own graphical user interfaces (GUI). One such GUI is shown below in Fig. 5. It can be observed that, it has the necessary controls to enable or disable the applied function. Also, it can be used to control the input magnitude of the applied voltages to the PMU. As mentioned before the upper limit for this applied voltage is only up to 10V restricted by the ratings of NI-9263 voltage output module (see Table I). Any modification from this end, should be visible in the waveform window present in the GUI instantaneously.

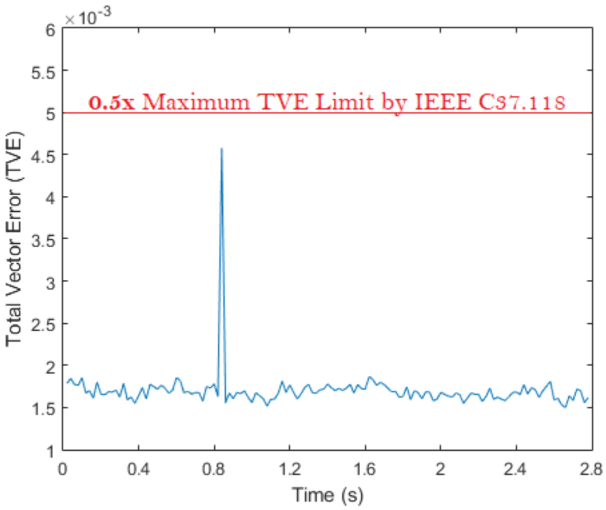


Fig. 6. Total Vector Error (TVE) of the PMU under test in Steady-State as tested by the Proposed PMU-Testing hardware

The PMU readings are broadcasted via the laboratory's managed TCP/IP network, and are available to be monitored by any client connected to the network. In this particular experiments, the Smart Grid Synchrophasor Software Development (S3DK) ToolKit [9] was used to monitor the PMU measurements from remote end.

IV. RESULTS

The performance of a PMU is quantified by two metrics in IEEE C37.118 standard. Those are (a) Total Vector Error (TVE) and (b) Frequency Error (FE). For a given complex variable, $X(n)$ the TVE is given by the following mathematical expression

$$TVE = \sqrt{\frac{(X_{Re_M}(n) - X_{Re}(n))^2 + (X_{Im_M}(n) - X_{Im}(n))^2}{(X_{Re}(n) + X_{Im}(n))^2}}$$

where the variables X_{Re_M} and X_{Im_M} denotes the real and imaginary part of that complex variable as measured by the PMU.

Another important metric to characterize a PMU's performance is FE, which can be computed by the following expression

$$FE = |f_{Measublack} - f_{Actual}|$$

A. Steady State Test

Ideally, the PMU under test should pass all the compliance tests. However, in reality, it has been reported that in most cases PMUs [1],[3],[5] fail to pass some of the dynamic compliance tests. The steady state compliance tests are successful for all PMU-s. In this section, the steady state compliance tests are first reported followed by, the results from dynamic performance testing.

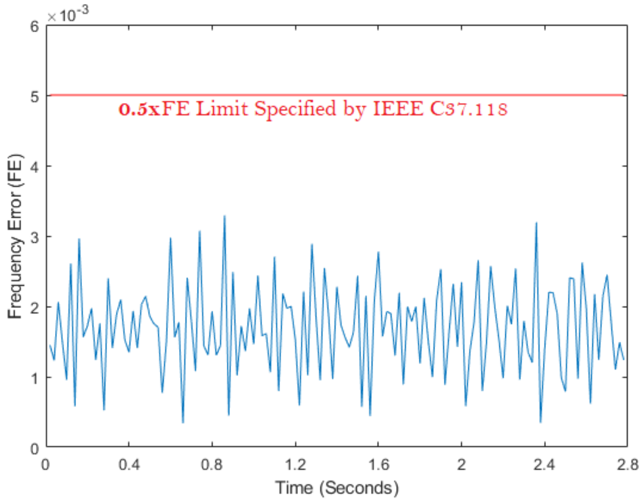


Fig. 7. Frequency Error (FE) of the PMU under test in Steady State as tested by the Proposed PMU-Testing hardware

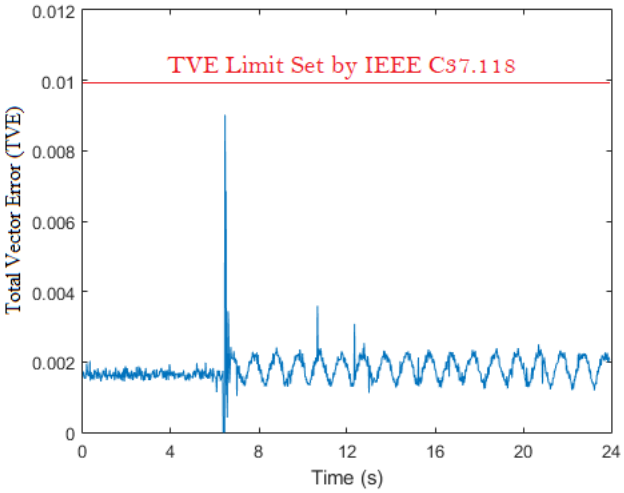


Fig. 8. Total Vector Error (TVE) of the PMU under Magnitude (0.1 pu) and Phase (10^o) Step Change

Figure 6 and 7 shows the steady state operation of the PMU under test. Since, this PMU is based on National Instruments' 'Advanced PMU Development System', it is expected to work satisfactorily at least in steady state. Figure 6 and 7 clearly shows that the performance of the PMU is well within the compliance limits expected in steady state. In fact, the errors were observed to be within half of the maximum permissible error limits at all times.

B. Step Change in Magnitude and Phase

The experiment for step change, was performed by applying 10^o step change in phase, and a 0.1 pu change in magnitude. The changes were applied in all the phases at the same side from the GUI. The data reporting rate was set at 50 samples per second.

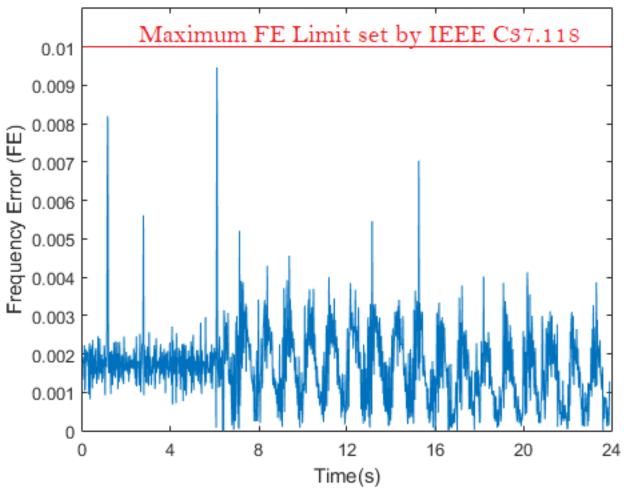


Fig. 9. Frequency Error (FE) of the PMU under Magnitude (0.1 pu) and Phase (10^o) Step Change

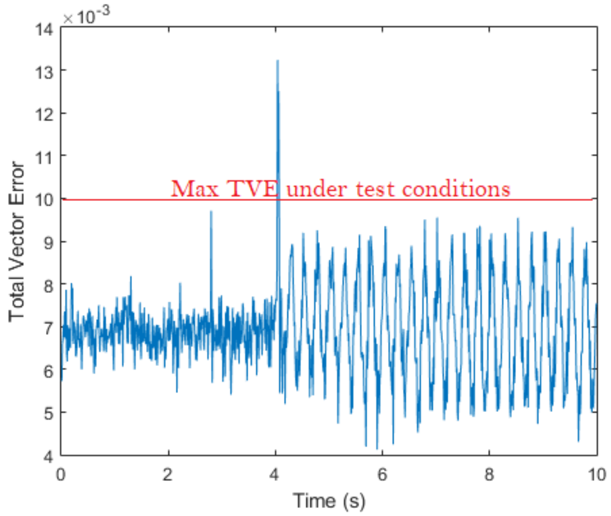


Fig. 10. Total Vector Error (TVE) of the PMU under Bandwidth Test

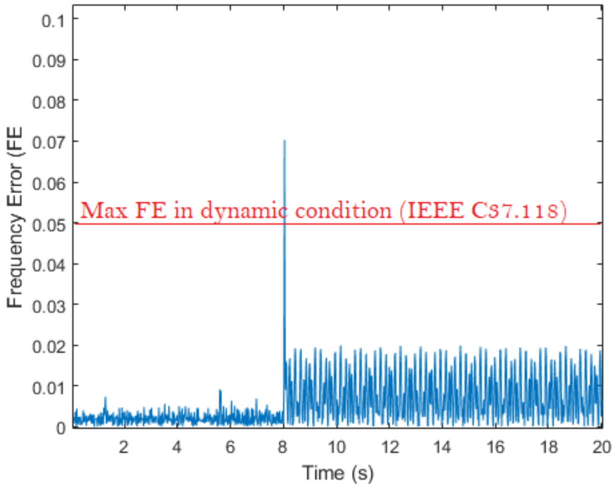


Fig. 11. Frequency Error (FE) of the PMU under test during Bandwidth Test

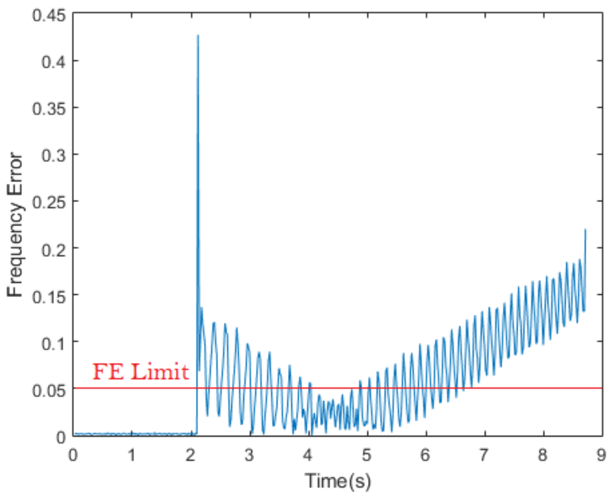


Fig. 12. Frequency Error (FE) of the PMU under test during Bandwidth Test

It can be clearly investigated from Fig 8 and Fig 9, that the quality of performance of the PMU deteriorates when compared to the steady state tests. However, the error of the TVE and FE are still within the specified range of IEEE C37.118 standard.

C. Bandwidth Test

For the bandwidth test, the modulation factor for both the phase angle and the magnitude are chosen to be 0.1. Fig 10 and 11 shows that there are very few instants during the beginning of the modulation, where the PMU performance is not sufficient to pass the compliance tests. However, the overall performance during the modulations seems satisfactory. In fact, during some test runs, the PMU under test manages to perform satisfactorily. The root cause of for this behavior merits further investigation.

D. Frequency Ramp Test

As shown in Fig 12 the PMU under test failed in the frequency ramp test. A 1 Hz/sec frequency ramp was applied to the signal. The range was from 48-55 Hz. The observed FE was more than 0.2 Hz, which is way above the certified limit (0.05) of Frequency Error set by IEEE C37.118 standard.

However, it must be noted that frequency ramp test is the most challenging test from the point of view of the PMU. Most of the literature existing in this domain reported a failed frequency test.

TABLE II
PMU FE performances during Frequency Ramp Test Available in the Literature

PMU Under test	Testing Hardware	Test Verdict	Max Error
PMU A as in [3]	Freja 300 Relay Set	Fail	0.015
PMU B as in [3]	Freja 300 Relay Set	Fail	0.006
PMU C as in [3]	Freja 300 Relay Set	Fail	0.022
PMU from [1]	Waveform Files	Fail	0.153
PMU Prototype on cRIO based on NI	PMU Testing Hardware proposed in this paper	Fail	0.22
PMU A as in [5]	Doble 6150 Relay Set Signals	Fail	0.35
PMU B as in [5]	Doble 6150 Relay Set Signals	Fail	0.44
PMU C as in [5]	Doble 6150 Relay Set Signals	Fail	0.08

Table II shows that this is not uncommon. In fact it can be further seen that, the PMU models in [1] and [5] also perform in a similar range as the PMU prototype tested in the experiments in this paper.

V. Future Work

In future work, the evaluation of dynamic performance of PMUs using this test hardware needs to be performed. More specifically, the study of time delay and settling time, upon the application of step changes in magnitude and phase as specified in IEEE C37.118.1-2011 and IEEE C37.118.1a-2014, needs further experiments and analysis. This paper only presents test results from an M class PMU provided by the NI Advanced PMU development system, even though the same proposed hardware can be used in evaluating the performance of a P class PMU as well, which will be subject of future work.

VI. Conclusions

The experimental results in this paper shows that the PMU under test performs satisfactorily in steady state condition, and performs reasonably well under all dynamic conditions except the frequency ramp test. Even though the frequency ramp test failed for the PMU, it is clearly a limitation in the PMU technology and product of the test-infrastructure. The proposed contribution of the current work was to provide a user friendly test-infrastructure, which would be able to evaluate the performance quality of a PMU under test. The presented experimental results clearly show that the test-hardware for testing PMU functionalities can be used for PMU pre-compliance testing with confidence. One of the advantages of the testing infrastructure proposed is that it is completely configurable from the software side. This makes it a very attractive solution for testing PMUs in laboratory environment during their development process.

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