

PMU-based Real-Time Damping Control System Software and Hardware Architecture Synthesis and Evaluation

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Abstract—Low-frequency, electromechanically induced, inter-area oscillations are of concern in the continued stability of inter-connected power systems. Wide Area Monitoring, Protection and Control (WAMPAC) systems based on wide-area measurements such as synchrophasor (C37.118) data can be exploited to address the inter-area oscillation problem. This work develops a hardware prototype of a synchrophasor-based oscillation damping control system. A Compact Reconfigurable Input Output (cRIO) controller from National Instruments is used to implement the real-time prototype. This paper presents the design process followed for the development of the software architecture. The design method followed a three step process of design proposal, design refinement and finally attempted implementation. The goals of the design, the challenges faced and the refinements necessary are presented. The design implemented is tested and validated on OPAL-RT's eMEGASIM real-time simulation platform and a brief discussion of the experimental results is included.

I. INTRODUCTION

The growth of power system interconnections between previously isolated areas has given rise to the phenomenon of inter-area oscillations. These are low frequency (0.1-2 Hz.) oscillations where the generators of one synchronous area oscillate against those of another area. Damping for these oscillations is generally poor and if they are allowed to grow, they can lead to disconnection of the ties or a collapse of the power system. A famous example of the latter was the August 1996 blackout of the WSCC system in the USA [1]. Although the purpose of system interconnection was to increase stability, the present situation of the power system incorporates renewable energy sources and power trading corridors, both of which impact system stability.

A. Previous Experiences

Modern solutions to this problem involve using Power System Stabilisers (PSS) with locally available signals. These are effective at damping intra-area modes with good observability but may not be as effective at damping inter-area modes [2] [3]. A theoretical analysis of the advantages of using wide-area signals as a damping input is presented in [4]. Field-test experiences with WAPOD controllers from Norway and China are presented in [2] and [5] respectively. Although these initial field tests show promising results, the wide-area control systems tested so far have been implemented by

extending the installed control system of an existing device (e.g. an SVC, see [2]) to receive synchrophasor data, process it and to then feed the control algorithm. To the knowledge of the authors, there has not been any reported attempt at designing a general purpose, wide-area control system, starting from specifications and considering different hardware and software constraints. Such an approach is attractive as it can easily be adapted to different controllable elements thereby reducing implementation costs and facilitating straightforward development.

B. Contributions

The goal of this paper is to document the software development process and challenges faced in the real-time implementation of a wide-area control system. Ängquist and Gama's [6] Phasor Power Oscillation (Phasor POD) algorithm was chosen based on the operational requirements and control system design constraints. The developed prototype is termed a Wide Area Power Oscillation Damper¹ (WAPOD). For purposes of comparison, the real-time SIMULINK implementation of the Phasor POD algorithm by Almas and Vanfretti [8] is used as a benchmark. The performance of the developed hardware prototype will be tested and compared to the performance of this implementation of the algorithm. The two-area four-machine model developed by Klein, Rogers and Kundur [9] is used as a test-case and is modified to fit the requirements of experimental testing. A Hardware-in-the-loop experiment is constructed around the eMEGASIM real-time simulator from OPAL-RT [10] with the two-area model running in real-time, physical PMUs and a synchrophasor-based Phasor-POD algorithm running on a cRIO (Figure 1).

C. Paper Outline

This paper is organised as follows. Section II outlines the hardware and software components used together with an overview of the Phasor POD algorithm implemented. Section

¹Historically, damping stabilizers have been termed WAPOD where the P represents a measurement of active power through the line. In such context, active power is used as a controller input signal. Although this term is not accurate when other quantities are used as control inputs or feedback signals, the term is used here to maintain consistency with existing literature.

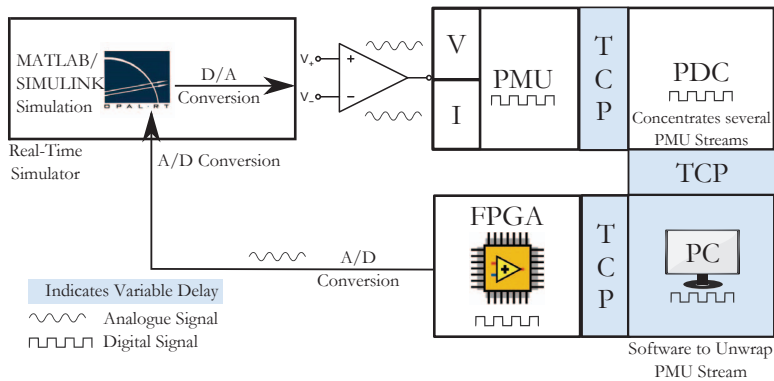


Fig. 1. Data flow path with digital and analogue components indicated. Note that data to the FPGA flows through the real-time section of the cRIO though this is not shown for simplicity.

III examines the details of the architecture developed for this controller and the various stages of refinement and changes made to it. Section V presents the results of the Hardware-in-the-loop experiments performed and conclusions are drawn in Section VI.

II. BACKGROUND

A. Phasor POD Algorithm

This algorithm [6] was selected due to its wide applicability and the fact that it does not depend on the network model or updated knowledge of the network topology. Typical model-linearisation based damping algorithms rely on computer-intensive calculations and are often valid for a particular network operating point. In contrast, the Phasor-POD algorithm only requires knowledge of the inter-area oscillation frequency, which is generally known from system studies or can be determined from synchrophasor measurements [7]. Consider Equation 1, which represents a general signal $s(t)$, as an average valued component and an oscillating component.

$$s(t) = s_{avg} + \text{Re} \left\{ \vec{s}_{ph} \cdot e^{j\omega t} \right\} \quad (1)$$

where \vec{s}_{ph} is a complex phasor, rotating at the frequency ω [6]. The Phasor-POD algorithm uses the known oscillation frequency to set up a co-ordinate system rotating at this frequency and continuously extracts a phasor representing the oscillation magnitude [6]. The implementation of the algorithm used here is based on Almas and Vanfretti's SIMULINK implementation [8].

B. Hardware and Software

Real-Time Controller: The real-time implementation of the Phasor-POD algorithm in this work is based on the Compact Reconfigurable Input Output (cRIO) controller from National Instruments. The cRIO 9081 is used to implement the algorithm. It has an on-board Field Programmable Gate Array (FPGA) in addition to a 1.06 GHz Intel Celeron processor for real-time control applications [11].

Phasor Measurement Units: The inputs to the real-time controller were taken from an IEEE C37.118-compliant synchrophasor data stream. Measurement data for this stream was generated by two PMU's which monitor three-phase currents and voltages at different points on the power network. In this work, two cRIO9076 real-time controllers [11] were deployed as PMUs [12].

Real-Time Simulator: The eMEGASIM real-time simulator from OPAL-RT [10] was used for simulating the two-area network in real-time. This simulator allows for hardware-in-the-loop tests to be carried out using its analogue input and output terminals. Voltage and current signals were extracted from the simulator's analogue outputs and fed to amplifiers. These amplified signals were then wired to the current and voltage inputs of PMU's. Similarly, the damping signal generated by the Phasor-POD algorithm was wired back to the simulator's analogue input terminals for use in the simulation. Figure 1 presents the entire signal path including the external, closed-loop controller.

Software: The test-case network model used here was a version of the Klein-Rogers-Kundur two-area system implemented in a SIMULINK demo available with SimPowerSystems [13]. This was modified to include an average-valued SVC model, identical to that used in [8]. The software on the cRIO was written using LabView's Real-Time modules. Software development was done on a workstation computer. Code was loaded on the various devices (cRIO controllers, RT Simulator) over a TCP network.

III. ARCHITECTURE DEVELOPMENT PROCESS

Before beginning the development process, a software development methodology was adopted with the aim of streamlining the process². The approach followed here is based on the Waterfall method detailed in [15]. The approach broadly includes the four steps from [15]

²There are many software development methods that could be adopted. However, for this specific application (i.e a PMU-based WAPOD), none of them have been reported and used in available literature. The process here was favoured over the others due to the availability and limitations of the hardware-in-the-loop experimental testing facilities available at the SmartS Lab [14]

- 1) Initial Investigation
- 2) Requirements Definition
- 3) Architecture Design
- 4) Coding and Implementation
- 5) Experimental Testing to validate requirements

An additional fifth step could be avoided thanks to the availability and use of HIL testing. The linear waterfall method was modified to be iterative so as to account for various constraints and to also account for revisions in the initial definition caused by these constraints. This iterative process is illustrated in Figure 2 and is realised for the specific application here, as illustrated in Figure 2. Several reasons were behind the choice of an iterative design approach. Chief among them was the cRIO hardware itself. As an implementation on this hardware had not been attempted earlier, the limitations of the hardware were unknown. Based on the limitations faced during an implementation attempt, the design and features incorporated would be revised to fit within the limitations of the hardware.

A. Controller Hardware Analysis

A cRIO9081 [11] was chosen as the real-time controller. This controller has a real-time section running user-written code on an Intel CPU. Additionally, a Xilinx FPGA (400MHz.) is available for direct interfacing with hardware signals. The cRIO was chosen as a development platform due to the ease with which code could be written, tested and verified. An analogue voltage output module was also used to interface the controller directly with the real-time simulator. The primary constraint of this or any other controller is the storage space available for code.

B. Constraints

Before defining requirements, the possible constraints at each stage of the test set-up were considered. The test set-up shown in Figure 1 is used to illustrate the constraints faced.

Differing Loop Rates: The power system simulation running on the real-time simulator was executed at a loop rate of $50\mu s$. This meant that the simulator generated new values for currents and voltages every $50\mu s$, and would also expect data from the HIL system every $50\mu s^3$. The constraint here was the data reporting rate of the PMU's used which was a maximum of 50 samples per second or one sample every 20ms. This was much slower than the $50\mu s$ loop rate of the real-time simulator.

FPGA Accuracy: While the exact role of the FPGA in this implementation was not known in advance, it brought with it some limitations. Chief among these was the limitation on data accuracy due to the fact that all calculations would be implemented in hardware.

IV. ARCHITECTURE IMPLEMENTATION AND REFINEMENT

Figure 2-1 shows the three-stage design process with design proposal, implementation and revision. To begin with, only the

controller specifications were available. These were used to draft a design proposal. An implementation attempt was made using this draft proposal. When the additional limits imposed by the software and hardware platforms were included, some goals of the original implementation needed to be revised. With these limitations, the original design was modified to generate a revised design. An attempt was then made to implement this revised design. As further limitations were encountered, the design was further modified. This iterative process was repeated till a working implementation was reached.

1) Initial Design: Initially, an autonomous, independent controller was envisaged. Such a controller would be able to receive IEEE C37.118 synchrophasor data directly over the communication network and extract measurement data. The architecture block diagram is shown in Figure 2-2. This controller was completely autonomous, with automated signal selection and processing. This design also incorporated two control functions, a wide area control function and a local control function. The wide area control function selected was the phasor-based oscillation damping control algorithm [6]. The local control function would use locally available data in a manner similar to a Power System Stabiliser (PSS). Automatic switching between the two functions and automated input signal selection was also considered. If the signal to noise ratio in the wide area signal deteriorated or if the signal delay became prohibitively high, the controller would automatically switch to the local signal or another wide-area signal. The principal consideration in this design was the limited resources available on the FPGA and the complexity of the algorithms to be implemented. This required implementation of all algorithms and computation sections on the RT section of the cRIO with the FPGA being used for interpolation only.

Challenges: This design was faced with a problem of differing loop rates. The real-time simulator runs at a $50\mu s$ time step. The fastest that the RT controller could run was 1ms. Data would thus be generated faster than the RT controller was able to process. The second problem was producing control output at the rate expected by the real-time simulator. The speed constraint of the RT controller meant that it would not be possible to use it to generate a control signal. To address this issue, this architecture envisaged using the FPGA to perform interpolation between successive data points. The FPGA would run at a loop rate of $50\mu s$, to match the real-time simulator. The region between successive data points would be interpolated using a suitable interpolation algorithm. Data generated by the FPGA would be sent over the communication network back to the real-time simulator for use in the simulation. This design needed to be changed due to limitations of different components.

One, no software was available to receive a synchrophasor stream and extract measurement data directly on the RT controller. This process had to be performed on a desktop computer running a real-time data mediator (Statnett's Synchrophasor Software Development Tool-kit, S^3DK [16]) and LabVIEW. Once measurement data from the synchropha-

³In a real-life application, the controller output may not have this constraint. However, the subsequent control system must sample the WAPOD controller's output at a rate faster than the PMU reporting rate.

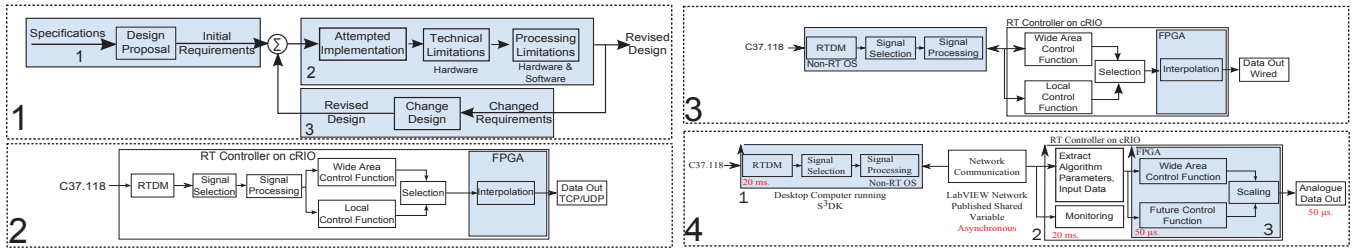


Fig. 2. 1. Three-stage architecture refinement process. 2. Initial architecture attempted 3. First architecture refinement 4. Final architecture as implemented

stream was available, it could be streamed to the real-time controller over the TCP/IP network using LabView's Shared Network Variables. Two, data generated by the FPGA could not be sent to the real-time simulator directly over the communication network. Though theoretically possible, further work is required. Also, for each successive data point received by the real-time controller, the FPGA would generate 400, interpolated, data points. Synchronising the process of generating the control signal and the use of the generated data on the real-time simulator is a complex task. Three, the process of data interpolation on the FPGA is computationally intensive. To achieve results better than with a simple linear interpolation, a history of past data points is required. This process is, in itself, complex and introduces further delay. It is, however, simpler than implementing the damping control algorithm on the FPGA. At this stage, FPGA limitations were the principal factor behind choosing to implement the Phasor-POD algorithm on the RT controller.

Four, an algorithm for automated signal selection based on observability indices had not been developed. In principle, this too, is possible and can be implemented on the real-time controller in the future when such an algorithm is developed and verified. The Phasor POD algorithm input parameters also change depending on the input used. An approach to determine these parameters iteratively or calculate them from input data is required.

2) *Development and Revision:* With the limitations of the initial architecture in mind, the architecture was refined. The process of extracting data from the synchrophasor stream was shifted to a workstation computer along with the processes of signal selection and processing. Once data was available, it was sent to the RT controller, over the network. The damping control was kept on the RT controller with the FPGA performing the interpolation required to match the read-interval of the real-time simulator. Besides the damping control algorithm, a local control function was included on the RT controller. This revision is shown in Figure 2-3. Here, the complexity of implementing an interpolation algorithm on the FPGA was examined in detail. An implementation of the damping control algorithm on the RT controller was also tested. The fastest loop rate that could be achieved was always in excess of 25ms. This was slower than

the reporting rate of the PMUs. Communication between the cRIO and the RT simulator using TCP/IP was also abandoned. Analogue output signals of the FPGA were instead hard-wired to the real-time simulator's analogue inputs.

3) *Final Implementation:* At this stage, the damping control algorithm was moved to the FPGA with the RT controller being used only for network communication and data monitoring. The Phasor POD algorithm parameters and monitoring data would be sent over the network to the RT section of the controller. The local control function was also discarded as it was found to reduce the response speed of the RT controller. If needed and if space permits, the local control function can be implemented on the FPGA. The desired 50µs data output rate could also be maintained as the FPGA was capable of response times of this order. The problem of differing data and loop rates was solved by implementing a basic sample-and-hold algorithm on the FPGA. Data would still be received from the RT controller every 20 ms. but the output would be held constant till the next data point was received and processed. With the Phasor POD algorithm implemented on the FPGA, resource utilization stood at 78%. As with the previous design, the process of extracting data from the synchrophasor stream was done on a workstation computer. This (Figure 2-4) was the final architecture as implemented.

V. HARDWARE-IN-THE-LOOP TEST

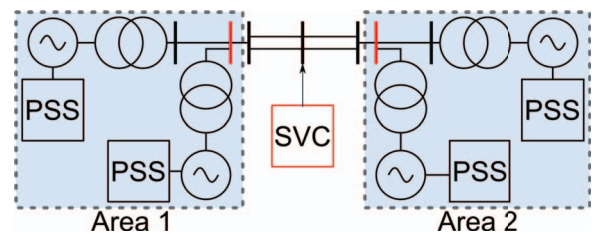


Fig. 3. Two Area Test network used. PMU measurements are taken from the buses indicated in red.

A set-up identical to that outlined in Figure 1 was constructed and used to verify the working of the real-time implementation of the Phasor-POD algorithm. The algorithm had previously been tested with the two area system within a SIMULINK environment (no HIL execution). It was verified to be able to keep the system in steady state stability and to restore the system to stability after the application of a minor disturbance. The benchmark for the real-time implementation

of the algorithm is thus established. The single-line-diagram of the two-area test network used is shown in Figure 3 with PMU locations shown by the red buses. The signal generated from the real-time Phasor POD implementation is reinserted in the model at the control system of the SVC. The hardware

prototype uses a real-time implementation of a wide-area control system. Issues and challenges faced in this implementation are documented and examined. The architecture development & refinement process for this implementation is also examined in detail. The success of the tests performed indicates that PMU-based wide area controllers can be exploited for multiple control applications in power system control and monitoring.

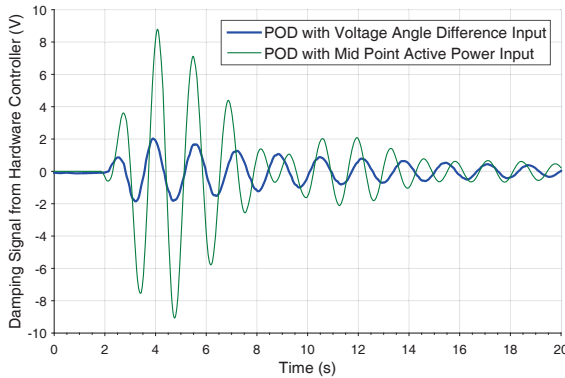


Fig. 4. Performance of Hardware controller with small disturbance. Note that the decreasing magnitude of the damping signal indicates that the oscillation magnitude is decreasing in correspondence.

implementation of the POD algorithm was verified to be able to keep the system stable in steady state. It was also tested with small perturbations applied at one generator to excite the inter-area mode and was verified to work satisfactorily. Figure 4 shows the performance of the controller with two different inputs, active power and voltage angle difference. It is immediately evident that using the voltage angle difference provides better performance. Though this performance is not identical to that observed in simulations, it indicates that the real-time implementation of the algorithm was successful. The damping signal generated by the hardware controller was captured on an oscilloscope and is presented in Figure 5.

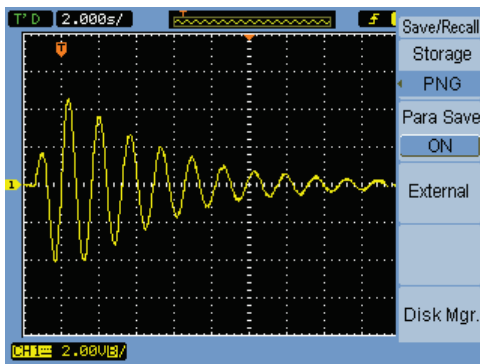


Fig. 5. Controller Response with Voltage Angle Difference input captured using an Oscilloscope

VI. CONCLUSION

A hardware prototype of a real-time power oscillation damping control system was developed and tested. The developed

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