# Hybrid Nearest Level and Open Loop Control of Modular Multilevel Converters

Naveed Ahmad Khan, Luigi Vanfretti, Wei Li and Arif Haider

*Abstract*— **In this paper a Nearest Level Control with open loop approach for modular multilevel converter (MMC) is proposed. By using open loop approach it is possible to suppress circulating currents without using feedback controllers. Moreover, with this method, both N+1 and 2N+1 levels (N=number of sub-modules) can be obtained at the output voltage. In addition, the voltage quality is improved and the total harmonic distortion is reduced at higher and lower modulation indices by increasing the number of levels up to 2N+1. Simulation results of 3-phase MMC are presented for both 2N+1 and N+1 levels together with the description of proposed Nearest Level Control scheme.**

## I. Introduction

Modular Multilevel Converters (MMC) offer an attractive topology with which the harmonic content of the output voltage can be significantly reduced as compared to conventional two level voltage source converters (VSC) [1]. Various multilevel topologies have been proposed, among them MMC is the most popular. This is due to its ability to process both active and reactive power with its terminals directly coupled to high-voltage networks [2]. The MMC outlined in Fig. 1 consists of an inductor in series with N sub-modules (SMs) in each arm. Each SM consists of a controlled half bridge and a dc capacitor [3] [4]. In high voltage applications N can vary up to several hundreds. The large number of SMs in each arm results in high quality output voltage waveform as well as increased efficiency [1]. Therefore MMC is considered very attractive for high power applications e.g. HVDC transmission, high power motor drives and railway supplies [1].

The MMC can be controlled with different modulation schemes. Each of them has several advantages and drawbacks. These schemes can be divided into two main categories: (a) High frequency PWM schemes and (b) Low frequency switching schemes. In (a) multiple carriers, either phase shifted or level shifted, are used (see [5] [6]). These schemes are now mature [6], but face the drawback of increased switching losses due to high switching frequency, especially for high power applications. Category (b) mainly consists of space vector modulation (SVM) with reduced switching frequency, Selective Harmonic Elimination (SHE), Nearest Vector Control (NVC) and Nearest Level Control (NLC). SVM and SHE offer good performance regarding switching losses, however, for a high number of levels their implementation complexity increases. NLC and NVC are suitable for a high number of levels, for lower number of levels and lower modulation indices the total harmonic distortion (THD) increases due to low and variable switching frequency [6]. NLC is attractive in terms of simplified implementation and low switching losses. However, proper sampling frequency is required to obtain the staircase reference waveform. Furthermore feedback controllers are required to suppress the circulating currents.

This paper proposes a new NLC method that aims to mitigate the above-mentioned drawbacks with the following modifications: (1) Staircase reference waveforms are obtained with an alternative approach, i.e. without taking into account sampling frequency. (2) The circulating currents are suppressed by using the open loop approach [4] instead of feedback controllers. This paper describes the methods utilized to obtain the stair case reference waveforms and how the circulating currents are suppressed without feedback controllers.

The reminder of this paper is organized as follows. Section II describes the topology of the converter and the mathematical model. Section III describes the proposed control scheme. Both conventional and modified nearest level controls, are explained. Section IV presents the proposed modulation process. Simulation results are shown in Section V. Conclusions are drawn in Section VI.

## II. MMC Topology

A three phase MMC is shown in Fig. 1. Each phase leg of this converter consists of two arms (upper and lower). In each arm $N$ number of SMs are connected in series with one inductor. The SM in each arm consists of capacitor and two IGBTs with antiparallel diodes. Each SM holds two states: on-state when the upper IGBT is on, i.e. $U_{Sub} = U_{dc}/N$, and off state when the lower IGBT is on, i.e.$U_{Sub} = 0$. The arm voltage can therefore be controlled by controlling $N$ number of SMs in each arm. If the capacitor voltage in each SM is assumed constant then the arm voltage can be described as,

$$u_{arm_i} = n_{arm_i} . u_{c_i}^{\Sigma} \quad (1)$$

where, $n_{arm_i}$ is the insertion index of each arm, $u_{c_i}^{\Sigma}$ is the total capacitor voltage in each arm and $i$ represents the upper or lower arm.

Naveed Ahmad Khan and Arif Haider are with ABB AB Ludivika., Sweden. (e-mail: naveed.ahmad-khan@se.abb.com & arif.haider@se.abb.com)
L. Vanfretti and W. Li are with KTH Royal Institute of Technology, Stockholm, Sweden. (e-mail: luigiv@kth.se)
L. Vanfretti is with Statnett SF, the Norwegian transmission system operator, Oslo, Norway. (e-mail: luigi.vanfretti@statnett.no)

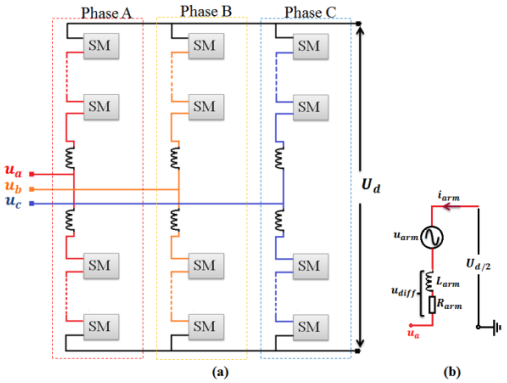


**Figure 1a and 1b Topology of a three phase MMC**

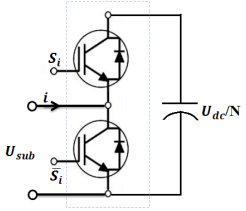


**Figure 2: Structure of a Submodule (SM)**

*A. Operation Principle*

The output voltage in each phase leg of the converter can be determined by the voltages produced by each arm. The voltage in each arm can be controlled by varying the number of SMs to be inserted or bypassed. A signal that keeps the information of how many SMs from both upper and lower arms should be inserted or bypassed is termed as insertion index $n_{arm_i}$ and is defined in (1). The voltage that each arm can produce depends upon the sum of capacitor voltages in each arm. The total capacitor voltage in the upper and lower arms is represented as $u_{cu}^{\Sigma}$ and $u_{cl}^{\Sigma}$ and the corresponding insertion indices are $n_u$ and $n_l$. By keeping the capacitor voltages balanced with proper insert/bypass operation, the instantaneous arm voltages can then be represented as [3]

$$u_{cu} = n_u . u_{cu}^{\Sigma} \quad (2)$$

$$u_{cl} = n_l . u_{cl}^{\Sigma} \quad (3)$$

In ideal conditions each arm carries half of the AC side current and a direct component that circulates between the arms and dc link voltage. The arm current can be expressed as [4],

$$i_u = \frac{i_v}{2} + i_{diff} \quad (4)$$

$$i_l = \frac{i_v}{2} - i_{diff} \quad (5)$$

where $i_{diff}$ is termed circulating current and should be a dc quantity. In case it is alternating it causes substantial variation in the total capacitor voltage in each arm [4].

The desired AC voltage produced by the converter can be written as,

$$u_{ref} = \hat{u}_{ref} \cos(\omega_1 t) \quad (6)$$

The voltage that the upper and lower arm can produce in terms of the dc-link voltage and the desired AC voltage can be expressed as

$$u_{cu}^{ref} = \frac{U_d}{2} - u_{ref} \quad (7)$$

$$u_{cl}^{ref} = \frac{U_d}{2} + u_{ref} \quad (8)$$

As it can be seen from Fig. 1b, the voltage $u_{diff}$ across the impedances in each arm also contributes in the total arm voltages. This term should be included in (7) and (8) as,

$$u_{cu}^{ref} = \frac{U_d}{2} - u_{ref} - u_{diff} \quad (9)$$

$$u_{cl}^{ref} = \frac{U_d}{2} + u_{ref} - u_{diff} \quad (10)$$

The term $u_{diff}$ controls the circulating current according to (see [4])

$$u_{diff} = L_{diff} \frac{di_{diff}}{dt} + R_{arm} i_{diff} \quad (11)$$

## III. Control Scheme

*A. Nearest Level Control (NLC)*

The control diagram for NLC is presented in Fig 3. The scheme is divided into three main stages, which are

- Sampling of reference waveform
- Dividing the samples by average voltage across each SM capacitor, i.e. $\frac{U_d}{N}$, and rounding the resulting values
- Voltage balancing of SMs capacitors and gate pulses generation for power switches

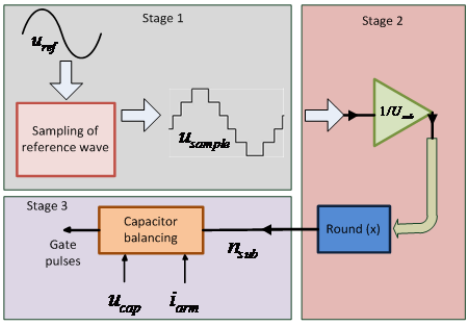


**Figure 3: Nearest Level Control**

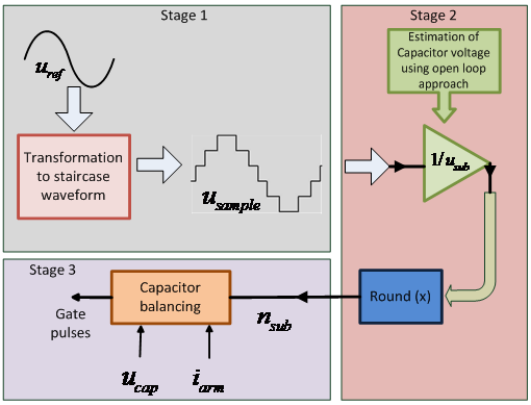


**Figure 4: Modified Nearest Level Control**

*B. Modified NLC*

The control diagram of the Modified NLC (MNLC) scheme proposed in this paper is presented in Fig. 4. The stages of the modified NLC are

- Transformation of reference waveform to staircase waveforms
- Computation of insertion indices for upper and lower arms

- Capacitor voltage balancing and gate pulse generation for switches

The main differences between NLC and MNLC are: transformation of reference waveform to stair case reference waveform and employing the open loop approach, which are described below.

*C. Transformation of reference wave to stair case waveform*

In the conventional NLC the reference waveform is converted to staircase waveform by sampling. The sampling frequency is of importance since it influences the number of levels and total harmonic distortion [7]. To avoid the complexity in sampling, an alternative approach is adopted to obtain the staircase waveform. With the modified approach the resulting waveform is a staircase waveform with a voltage step of $U_{dc}/N$ and basic NLC operating principles remain the same. The method is as follows,

a) The output reference waveform is split up into a reference waveform for the upper and lower arms by using (9) and (10).

b) The reference waves are then converted to staircase waveforms by using the following equations for the upper and lower arms,

$$u_{cu\_level}^{ref} = round\left(\frac{u_{cu}^{ref}}{u_{sub}}\right) * u_{sub} \quad (12)$$

$$u_{cl\_level}^{ref} = round\left(\frac{u_{cl}^{ref}}{u_{sub}}\right) * u_{sub} \quad (13)$$

where $u_{cu\_level}^{ref}$ represents the staircase reference waveform for the upper arm and $u_{sub}$ is the instantaneous voltage across one of the submodule's capacitor.

The SM's capacitor voltage can be defined in two different ways: i.e. $u_{sub} = \frac{U_d}{N}$ and through the estimation of the capacitor voltage in each arm with which the variation of capacitor voltage can be included.

The rounding process in (12) and (13), and the multiplication with $u_{sub}$ results in *N+1* levels for the upper and lower arms reference waves with a voltage step of$U_{dc}/N$, as shown in the Fig. 5.

The staircase waveform based on sampling frequency can result in voltage step higher or less than $U_{dc}/N$, if appropriate sampling frequency is not used [7]. However with (12) and (13), the voltage step for reference waves will always be $U_{dc}/N$.

The key advantage of using equations (12) and (13) is that the upper and lower arms can be controlled independently. In this way it is possible to achieve *2N+1* levels at the output voltage.

*D. Insertion index*

The insertion index is used to determine the number of SMs that should be inserted or bypassed. There are two ways to compute the insertion index. a) Direct modulation, in which the capacitor voltages in each arm are assumed constant [3] and b) open loop approach [3]: [4] in which the insertion index is computed by taking into account the variation of the capacitor voltages in each arm.

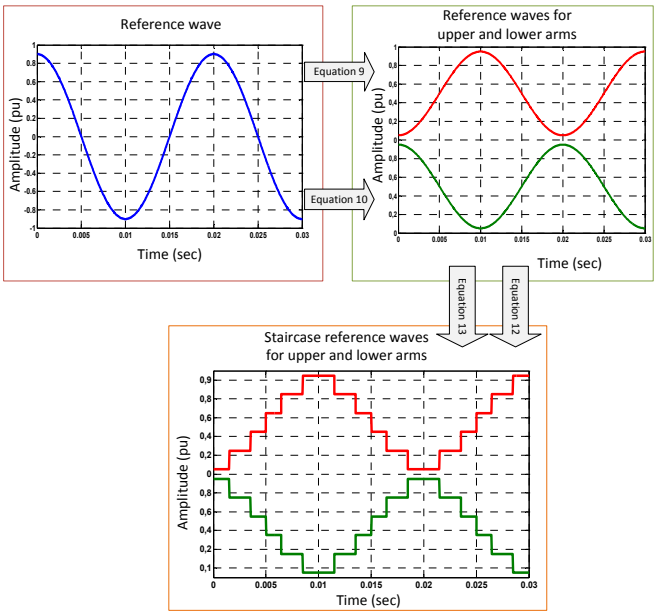


**Figure 5: Computation of reference waves for upper and lower arms**

*E. Direct Modulation*

The inserted voltage in each arm depends upon the sum of capacitor voltages (also known as available voltage). In direct modulation, the total capacitor voltage in each arm is assumed constant and equal to the dc-link voltage [3]. The variation of the capacitor voltages is not taken into account, therefore the insertion indices are computed as [3],

$$n_u = \frac{1-\hat{m}.\cos(\omega_1 t)}{2} \quad (14)$$

$$n_l = \frac{1+\hat{m}.\cos(\omega_1 t)}{2} \quad (15)$$

where $\hat{m}$ is the modulation index and can be defined as,

$$\hat{m} = \frac{\hat{U}_{ref}}{U_{dc}/2} \quad (16)$$

$n_u$: insertion index for the upper arm
$n_l$: insertion index for the lower arm
$\omega_1$: fundamental frequency in rad/sec

This modulation approach provides a line-line voltage with low voltage distortion. However, its drawback is substantial harmonic components in the arm currents, which circulate between the phase legs, between the phase legs and dc-link voltage [3] and are a source of additional losses.

*F. Open-loop approach*

In the open loop approach the variation of the capacitor voltage is taken into account to compute the insertion index [3], [4]. This method is based on the estimation of the capacitor's energy. In this way, the dynamics of the arm capacitor voltages can be included to compute the insertion index without feedback controls. This approach is useful to suppress circulating currents.

The equation to estimate the energy for upper arm in the steady state is given as [3],

$$W_{cu}^{\Sigma}(t) = W_{cuo}^{\Sigma} - \hat{e}_v.i_{diffo}.\frac{\sin(wt)}{w} + \left(\frac{U_d}{2} - Ri_{diffo}\right)\hat{\imath}_v.\sin(wt+\phi) - \hat{e}_v.\hat{\imath}_v.\frac{\sin(2wt+\phi)}{8w} \quad (17)$$

The circulating current is assumed as a pure dc-current,

$$i_{diffo} = \hat{e}_v.\hat{\imath}_v.\frac{\cos(\phi)}{U_{dc}+\sqrt{U_{dc}^2 - 4R\hat{e}_v\hat{\imath}_v\cos(\phi)}} \quad (18)$$

where, $\hat{e}_v$ is the peak value of output voltage, $\hat{\imath}_v$is the peak value of load current, $R$ is the arm resistance, $\phi$ is the phase difference between load voltage and current, $W_{cuo}^{\Sigma}$is the integration constant which can be used as a reference for the total arm average energy.

The total capacitor voltage in the arm voltage can be estimated as,

$$u_{cu}^{\Sigma} = \sqrt{2W_{cu}^{\Sigma}(t)/C_{arm}} \quad (19)$$

where,

$$C_{arm} = C_{sub}/N \quad (20)$$

The insertion index can now be computed by using the estimated capacitor voltage in each arm as,

$$n_u = \frac{u_{cu\_level}^{ref}}{u_{cu}^{\Sigma}} \quad (21)$$

Equation (21) represents the insertion index which is used to determine the number of SMs to be inserted or bypassed.

### *G. Capacitor Voltage Balancing*

With capacitor voltage balancing operation, the energy can be distributed equally among all the arm capacitors. The insert/bypass operation depends upon the fast monitoring of the SMs voltages and direction of arm current. The SMs are inserted or bypassed according to the following principle [8]:

- When the arm current has a direction that it charges the arm capacitors, the sub-modules with the minimum energy should be switched-on to achieve the desired arm voltage.
- When the arm current discharges the capacitors, the SMs with the maximum energy are switched-on to achieve the desired arm voltage.

## IV. MODULATION

### *A. N+1 Modulation*

For *N+1* modulation the SMs in the upper and lower arm of each phase leg are switched at the same instant, see Fig. 6. The switching instants for both the upper and lower arms are defined by $\theta_i$ $(i = 1,2,3 \dots n)$ in Fig. 6. Hence, *N+1* levels can be obtained at the output.

The different stages of the *N+1* modulation approach are shown in Fig 6. In the first stage, the staircase reference waveforms are obtained by using equations (12) and (13) for the upper and lower arms, respectively, as in Fig. 5.

In the second stage, the insertion index is obtained by using equation (21); i.e. applying the open loop approach. The obtained insertion index is then multiplied with the total number of submodules (N), i.e. $N.n_{up/low}$, and then the term is rounded to the closest integer. This process gives at any time the number of SMs from 0 to *N*, which are to be inserted. In the third stage by using capacitor-balancing algorithm, the gate pulses are sent to the dedicated SMs for insert/bypassed operation.

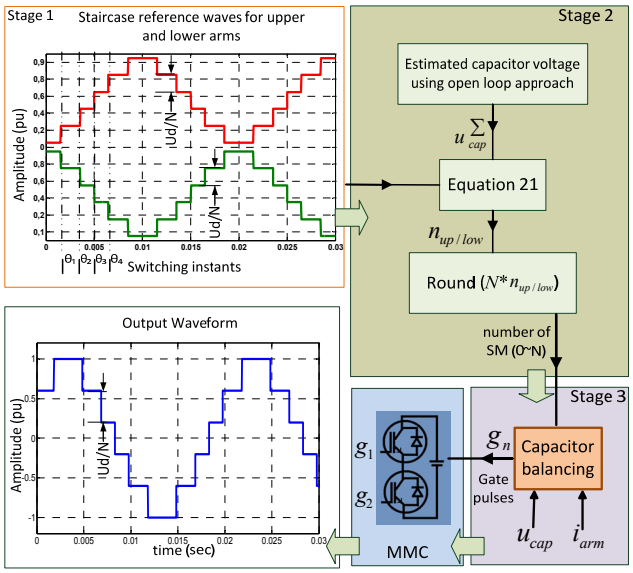


**Figure 6: Different stages of the N+1 Modulation approach**

### *B. 2N+1 Modulation*

In *2N+1* modulation, the upper and lower arms of each phase leg are treated independently. The switching instants are defined separately for upper and lower arms, i.e. $\theta_{ui}$ $(i = 1,2,3 \dots n)$ for the upper arm and $\theta_{lowi}$ $(i = 1,2,3 \dots n)$ for the lower arm, as shown in Fig. 7. By switching both the arms individually, the switching instant of one arm takes place in the midpoint of two successive switching instants of the other arm.

The output voltage of the MMC can be analytically defined as the difference between the upper and lower arm voltage, as given by

$$u_{phase,i} = \frac{u_{cu} - u_{cl}}{2} \quad (22)$$

By applying (21) to the reference waves of the upper and lower arms, the output voltage results in *2N+1* levels, as shown in Fig. 7. To separately define the switching instants for upper and lower arm, modifications are made in (12) and (13). The term $u_{sub}$ in the denominator is redefined as

$$u_{sub\_new} = u_{c\,u/l}^{\Sigma}/(N + \Delta E) \quad (23)$$

where $u_{cu/l}^{\Sigma}$is the estimated capacitor voltage for the upper or lower arm, $N$ is the number of SMs and $\Delta E$ is a small value that can be selected to achieve 2N+1 levels.

Equations (12) and (13) are redefined for *2N+1* modulation by using (23) as

$$u_{cu\_level}^{ref} = round\left(\frac{u_{cu}^{ref}}{u_{sub\_new}}\right) * u_{sub} \quad (24)$$

$$u_{cl\_level}^{ref} = round\left(\frac{u_{cl}^{ref}}{u_{sub\_new}}\right) * u_{sub} (25)$$

The term $\Delta E$ in (23) can be determined iteratively or can be chosen can be chosen depending upon the number of levels. For example in case of *N=6* SMs, *2N+1* levels are obtained by defining $\Delta E = 0.1$.

The reference waveforms defined by (24) and (25) are then used to generate the gate pulses with the modulation approach similar to *N+1* modulation as given in Fig. 6.

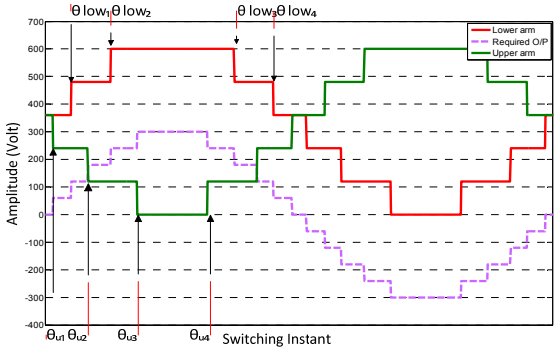


**Figure 7: Switching instants 2N+1 Modulation**

## V. SIMULATION MODEL AND RESULTS

To verify the proposed modulation scheme a detailed model of a MMC was implemented in MATLAB/Simulink using the SimPowerSystems Toolbox for *N=5* submodules. The configuration of the system is similar as in Figs. (1) and (2). The simulation parameters for the converter are given in Table 1.

In Fig. (8) and (9) the simulated waveforms using NLC for both *N+1* and *2N+1* modulation are shown in steady state. For *N=5* SMs, the output voltage is results in 6 levels using *N+1* modulation. On the other hand for *2N+1* modulation, 11 levels are obtained.

It can be observed Fig. (8a) that the circulating current is suppressed using the open loop approach. This shows that the circulating current can be suppressed using NLC without feedback control. Moreover, the number of levels at the output voltage level are *N+1* with balanced arm capacitor voltages. Capacitor voltage balancing is achieved using a sorting algorithm.

In Fig (9a) the circulating and arm currents for *2N+1* modulation are shown. Even though the open loop approach was adopted for this scheme yet the circulating currents were not suppressed. There is considerable ripple in the arm currents. The reason is that voltage spikes appear across the arm inductor due to individual control of each arm. The voltage spikes can be estimated by using (23) (see [8])

$$u_{arm_{ind}} = \frac{(U_d - u_{cu} - u_{cl})}{2} \qquad (23)$$

The voltage spikes for *N+1* and *2N+1* are shown in Fig 10 (left and right, respectively) for an ideal case. In *N+1* there are no voltage spikes across arm inductor whereas for *2N+1* they have considerable amplitude. As it can be observed in Fig. 10 (left), the amplitude of the spikes equals the voltage step of the output voltage. Increasing the number of SMs in each arm can reduce this voltage step. Consequently the amplitude of the spikes will reduce and also the ripple in the arm current. Moreover the circulating current can also be suppressed.

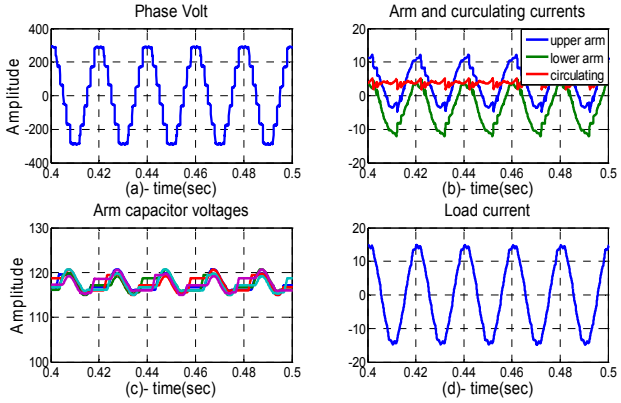


**Figure 8: Outputs for N+1 Modulation**

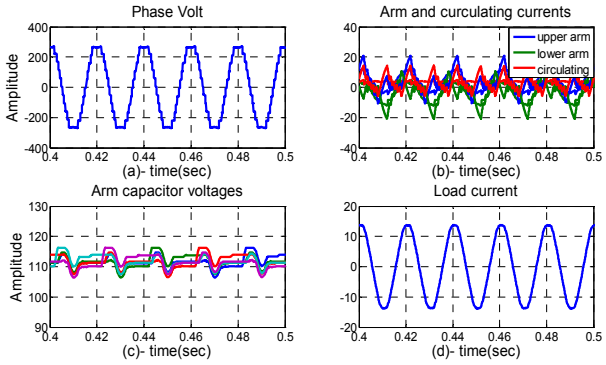


**Figure 9: Outputs for 2N+1 Modulation**

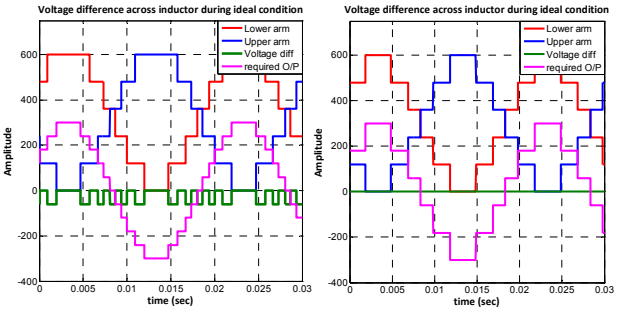


**Figure 10: Voltage difference at arm inductor for 2N+1 and N+1**

**Table 1: Converter parameters used for simulation**

| Parameters | Values |
|---|---|
| DC link voltage ($U_d$) | 600 V |
| Modulation index M | 0.9 |
| Arm Capacitance ($C_{sub}$) | 3.3 mF |
| Arm Inductance ($L_{arm}$) | 4.7 mH |
| Arm Resistance ($R_{arm}$) | 0.8 ohm |
| Load resistance ($R_{load}$) | 10Ω Three phase star connected |
| Load inductance ($L_{load}$) | 5.3 mH |

*A. Harmonic analysis*

Harmonic analysis is carried out to analyze the voltage quality of the output voltage waveforms for both *N+1* and *2N+1* modulation schemes. The operating parameters given in Table 1 are used for analysis.

The frequency components of the output phase voltage at different modulation indices together with THD for both *N+1* and *2N+1* are shown in Fig. (11). The total harmonic distortion was computed by using the following equation [7]

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} u_{an,n}}}{u_{an,1}} \qquad (23)$$

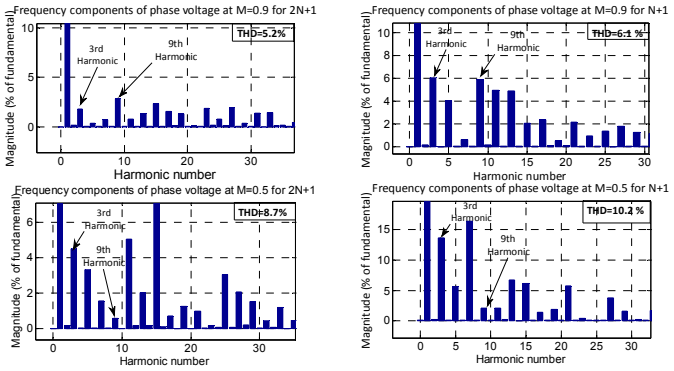


**Figure 11: THD at different at M=0.9 and M=0.5 for N+1 and 2N+1**

The THD for *2N+1* is slightly reduced as compared to *N+1*. The major difference is in the low-order harmonics, which are reduced three times using *2N+1* scheme. At low modulation index, low order harmonics are increased using *N+1* whereas for *2N+1* they still have low amplitude.

## VI. CONCLUSION

In this paper an NLC with open loop approach was presented for *N+1* and *2N+1* levels. The circulating current in the arms is suppressed for *N+1* levels by employing the open loop approach without any external controllers. However, for *2N+1* levels, the circulating current is not suppressed even when applying the open loop approach. The arm currents for *2N+1* can be improved by increasing the number of SMs. This may result in reduced voltage spike amplitudes across arm inductors and consequently reduced ripple and circulating current in the arm currents.

With the proposed method NLC can be suitable for a large number of SMs. This is because the low-order harmonics are high for low levels at the output voltage which is observed for *N=5* SMs. However, when the voltage levels are increased, the voltage quality is improved and the amplitude of the low order harmonics is reduced significantly.

Further work will focus on the analysis of the proposed approach applied to VSC-HVdc, with particular interest in its performance as compared to the approach used in the France-Spain VSC-HVdc-link.

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## REFERENCES


[1] A. Antonopoulos, S. Norrga, L. Ängquist, H.P. Nee, and L. Harnefors, "Dynamic Analysis of Modular Multilevel Converters," *IEEE Trans. on Industrial Electronics*, vol. 60, no. 7, pp. 2526-2537, July 2013.

[2] P. Wang, H. Zhu, Z. Chu, Y. Li and Z. Li, "An improved pulse width modulation method for Chopper-Cell-Based Modular Multilevel Converters," *IEEE Trans. on Power Electronics*, vol. 27, no.8, pp. 3472-3481, Aug. 2012.

[3] A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, H.P. Nee and L. Ängquist, "Inner Control of Modular Multilevel Converters – An approach using open-loop estimation of stored energy," in *The 2010 International Power Electronics Conference (IPEC),* pp. 1579 – 1585, 12-24 June 2010.

[4] A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, H.P. Nee, and L. Ängquist, "Open-Loop Control of Modular Multilevel Converters using Estimation of Stored Energy," *IEEE Trans. on Industrial Applications,* vol. 47, no. 6, pp. 2516 – 2524, Nov./Dec. 2011.

[5] A. Hassanpoor, S. Norrga, H.P. Nee, and L. Ängquist, "Evaluation of different Carrier-Based PWM Methods for Modular Multilevel Converters for HVDC Application," in *38th Annual Conference on IEEE Industrial Electronics Society (IECON 2012)*, pp. 388 – 393, 25-28 Oct. 2012.

[6] J. Rodriguez, J.I. Leon, S. Kouro, R. Portillo, M. A.M. Parts, L. G. Franquelo, "The Age of Multilevel Converters Arrives" *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28 – 39, June 2008.

[7] Q. Tu and Z. Xu, "Impact of sampling frequency on harmonic distortion for modular multilevel converters," *IEEE Trans. on Power Delivery*, vol. 26, no. 1, pp. 298 – 306, Jan. 2011.

[8] G. Konstantinou, *Harmonic elimination pulse width modulation of modular and hybrid multilevel converter topologies*, PhD Thesis, University of New South Wales, Australia, 2012. Available on-line: http://handle.unsw.edu.au/1959.4/51831