Generic High Level VSC-HVDC Grid Controls and Test Systems for Offline and Real Time Simulation

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***Abstract*— This article describes generic high level control models for VSC-HVDC grid systems. An average value model of the voltage source converter (VSC) is used; it includes the vector current control strategy. As an improvement to traditional conventional high-level control systems, this paper includes dc voltage, negative sequence current and dc voltage droop control loops. To validate the controller's performances, two tests systems were developed: a point-to-point link and a four-terminal DC grid. Both offline and real-time simulations are carried out for several test scenarios. A methodology for calibrating controller parameters is presented and used to tune the controls of each test system considering the different scenarios presented. All simulation models were developed in SimPowerSystem/Simulink and prepared using the RT-LAB software from Opal-RT for real-time simulation; real-time simulation performance of the simulation models is also discussed.**

***Index Terms*—Voltage Source Converter, High-level control, HVDC grid test system, controller calibration, Real-time simulation.**

I. Introduction

High voltage direct current (HVDC) transmission is an effective technology for transporting large amounts of electrical power over long distances and therefore may help to integrate renewable energies into the power grid. This technology has been employed to achieve the reduction of electric power losses for power transmission across long distances, and power exchange between asynchronous ac systems [1], [2]. The voltage source converter (VSC), a type of self-commutated converter, offers some advantages over the line-commutated converter (LCC) such as: independent power flow control and the flexibility to create multi-terminal DC grids with several converters [3].

To develop multi-terminal VSC-HVDC technology it is necessary to study the behavior and interaction of VSC controls. However, the lack of sufficiently detailed models and realistic equipment data limits research and development in this area. Therefore, the purposes and contributions of this article are the following: (i) to develop generic control models and test systems of two VSC-HVDC topologies; (ii) to calibrate and improve the high level control systems used by the VSC; (iii) to perform offline simulation for all of the developed models using SimPowerSystems/Simulink; (iv) to prepare the simulation models for real-time simulation using software libraries from Opal-RT; and (v) to perform real time simulation for all of the developed models using the eMegaSim real-time target from Opal-RT.

The remainder of this paper is organized as follows. Section II presents the average value model of the VSC and its control systems. In Section III, two test DC grid systems are introduced, a high level controller calibration methodology is proposed, and enhancements to the VSC control systems through additional control loops are described. Section IV provides off-line simulation results and analysis, while Section V discusses real time simulation aspects. Conclusions are drawn in Section VI.

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II. VSC and Its Control System

A. Voltage Source Converter Average Value Model (VSC-AVM)

An average value model of the VSC presented in article [4] has been adopted. The generic VSC model implementation in Simulink including an average value model is depicted in Fig. 1.

The VSC-AVM works on the basis of conservation of power. The total power consumed by the three controllable voltage sources (i.e. V_a,V_b and V_c) which are connected to the ac circuit, equal to the injected power by the controllable current source which are connected dc circuit of the converter, and provide direct current I_{dc} in to the dc link.

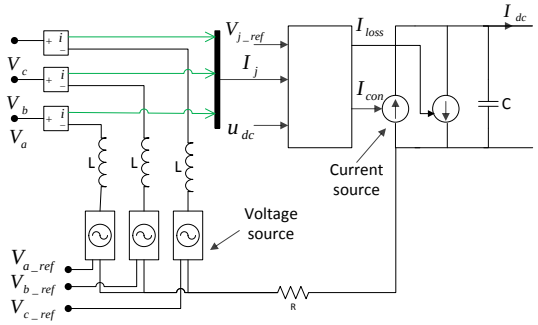


Figure 1: VSC-AVM Implementation in Simulink

B. VSC Control System

The control system of a VSC-HVDC link is classified into two levels: high level controls consist of dc voltage, active power, reactive power, and ac voltage control; while low level controls consist of pulse width modulation (PWM), current limiting and capacitor voltage balancing controls [5]. The main focus of this work is on high level control systems. A companion publication [6] details low level control systems developed by the authors. The vector control strategy comprised by outer and inner control blocks has been used in the high level control system. The vector control block diagram and Simulink implementation are shown in Fig. 2 and Fig. 3, respectively.

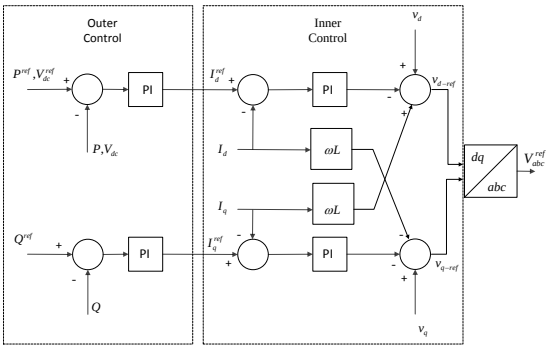


Figure 2: Vector control block

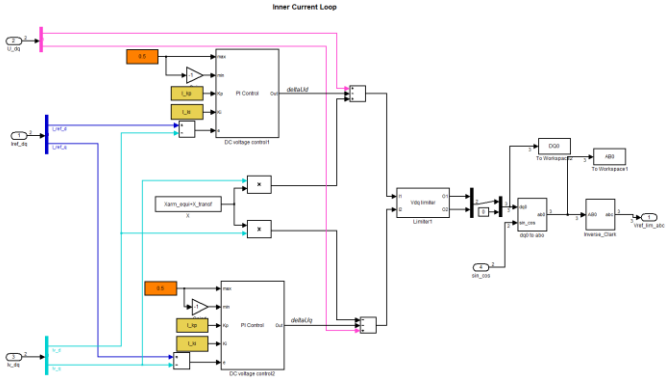


Figure 3: Inner controller implementation in Simulink

In the outer control block, active power, dc voltage and reactive power are controlled comparing with reference values by means of a PI controller and provides active and reactive current components as a reference to the inner control block. The measured grid voltage contains cross coupling components, which are removed by adding opposite components in the inner control block to facilitate independent control of active and reactive currents.

III. Calibration of High-Level Controls

A. VSC-HVDC Test Systems

This section introduces the developed point-to-point and four-terminal VSC-HVDC test systems, single line diagrams are shown in Fig. 4 and Fig. 5. Only the point-to-point test system implementation in Simulink is illustrated in Fig. 6, as the four-terminal implementation is similar. The average value model and control system of the VSC presented in Section II has been employed in both test systems with the same VSC-HVDC system parameters listed in Table1.

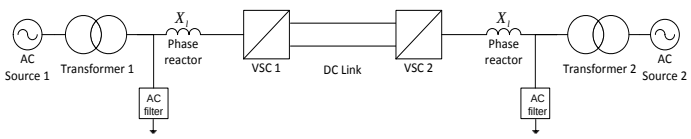


Figure 4: Point-to-point VSC-HVDC test system

Table 1 VSC-HVDC System Parameters

Converter rating	305 MVA
AC side voltage	380 KV RMS line to line
DC side voltage	320 KV
Reactance of transformer	0.18%
Arm inductance	0.075%
Capacitor energy in each sub module	40 KJ/MVA
Number of sub module in each arm	20
DC cable	750 km long

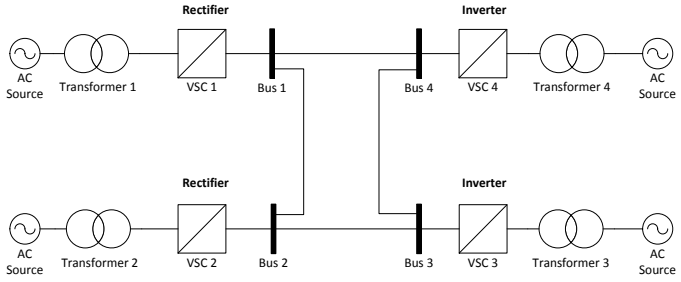


Figure 5: Four-terminal VSC-HVDC test system

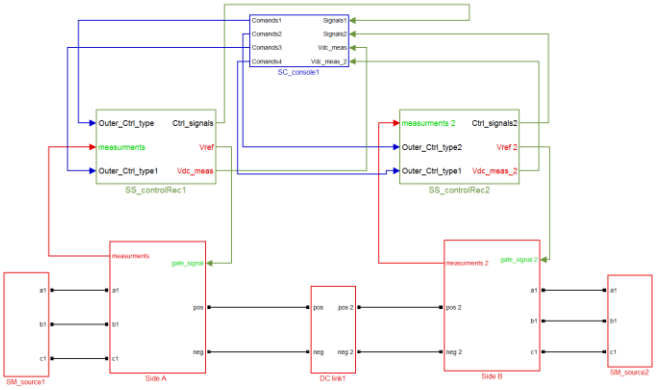


Figure 6: Point-to-point test system implementation in Simulink

B. Controller Calibration Methodology

High level controllers are constructed with PI blocks which regulate the system outputs according to their reference values. Therefore, proper tuning of the proportional and integral gain of PI controllers is significant to attain a satisfactory system performance. This article presents a controller calibration methodology. The methodology has been developed with the following design specifications: (a) to achieve a system response with less overshoot, (b) less undershoot during the transient period, and (c) less settling time of the controlled outputs, for both normal and fault conditions.

The method is illustrated using the point-to-point VSC-HVDC. Given that no analytical model is available, and the simulation models are ill-suited for formal mathematical derivations, the calibration method is developed using sequential steps, iterative parameter variation and numerical simulations.

The method is divided in three sequential steps. First, the active power controller is tuned to satisfy the active power flow in the system given by the active power reference value. Second, the dc voltage controller is tuned to assure constant dc voltage through the whole system. Finally, the reactive power

controller is tuned to keep the ac voltage of the system at the desired reference value.

In each of the steps above, step changes are applied in the control inputs and simulations for several proportional and integral gain values are performed. The final controllers' parameters are chosen by observing the controllers' responses and checking against design specifications. Simulation results are shown in Section IV. Converter control modes and reference values for the point-to-point VSC-HVDC test system are listed in Table 2.

C. Enhancement of the VSC Control System

The following enhancements are made to the standard VSC-HVDC control system.

1) Assessment of the Damping effect on DC Voltage Controller

The transfer function derived from ac-dc side balancing equation of the converter can be written as:

$$T.F = \frac{v_d}{u_{dc}} \frac{1}{s\, C_{dc}}$$

where, v_d is d component of ac side grid voltage, C_{dc} is dc link capacitance and s is Laplace operator. The pole at the origin creates difficulties for DC voltage regulation during unbalanced fault conditions. Therefore, a damping conductance (G_a) is modeled to provide damping during unbalanced fault conditions. The damping conductance models a resistive behavior in the converter output impedance which makes the grid less sensitive to harmonics and oscillations [7]. The modified DC voltage controller with damping effect is shown in Fig. 7.

With the goal of obtaining a damped DC voltage response, the damping conductance value needs to be computed. Damping conductance design and controller validation are presented in Section IV.

2) Negative Sequence Current Controller

Negative sequence current appears in the system during unbalanced fault conditions in the ac side of the system. Hence, it affects the ac line current and makes the system unbalanced. In our test system, a constant voltage source is connected with the converter through a Y/Δ transformer, and therefore the zero sequence current from the converter can be excluded [8], [9]. Hence, the controller should attempt to regulate both positive and negative sequence components.

The controller separates the measured grid current in to positive and negative sequence, and controls the negative sequence current in the inner control block so that it keeps at zero during fault conditions. The delayed signal cancellation (DSC) method proposed in [10] has been used for the sequence separation. The modified inner control block including negative sequence controller is presented in Fig. 8.

The negative sequence current controller block diagram shown in Fig. 9, observe that the reference values of current (i_d^{ref},i_q^{ref}) are set to zero.

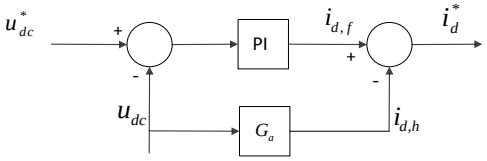


Figure 7: DC voltage controller with damping conductance

Table 2 Converter parameters for point to pint test system

Converter	Controlling type	Parameter reference value
VSC1 (rectifier)	Active power (P) Reactive power (Q)	$P^* = 1\ p.u$, $Q^* = 0\ p.u$
VSC2 (inverter)	DC voltage (u_{dc}) Reactive power (Q)	$u_{dc}^* = 1\ p.u$, $Q^* = 0\ p.u$

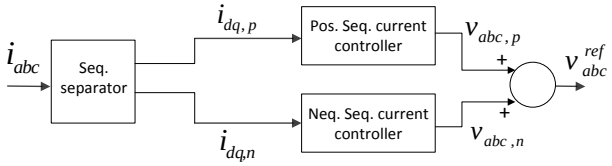


Figure 8: Modified Inner control block

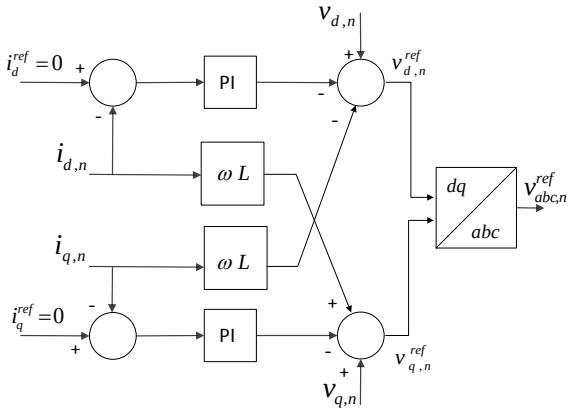


Figure 9: Negative sequence current controller block

A comparative performance assessment of the negative sequence current controller against the conventional inner controller is presented in Section IV.

3) DC Voltage Droop Controller

This control system combines constant active power and constant DC voltage controllers. From Fig. 10(a) it is observed how the active power controller keeps the power constant at the reference value in spite of changes to the DC voltage in the system. On the other hand, as shown in Fig. 10(b), the DC voltage controller keeps the voltage constant given changes in active power.

The DC voltage droop controller can regulate both active power and dc voltage in the same converter station with a pre-defined slope which is given according to the dc voltage response (R_{dc}) [2]. It provides a linear change to the dc voltage to a change in the reference of the active power. The droop controller block diagram and implementation are presented in Fig. 11 and Fig. 12 respectively. The performance of the droop controller is compared with the conventional dc voltage controller, employing both controllers in the four-terminal VSC-HVDC test system. The converter parameters that have been used for the simulation results shown in Section IV are listed in Table.3.

IV. Simulation Results

This section presents simulation results that validate the performance and calibration of the control systems presented in Section III. The simulations were carried out off-line, and several test scenarios were simulated for both test systems.

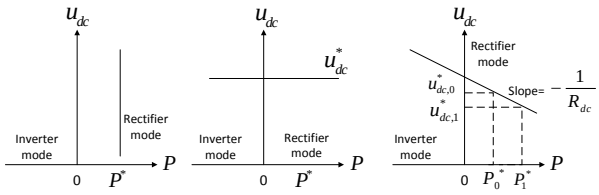


Figure 10: Active power and DC voltage characteristics of (a) active power controller, (b) DC voltage controller, (c) DC voltage droop controller

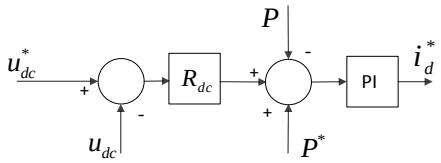


Figure 11: DC voltage droop control

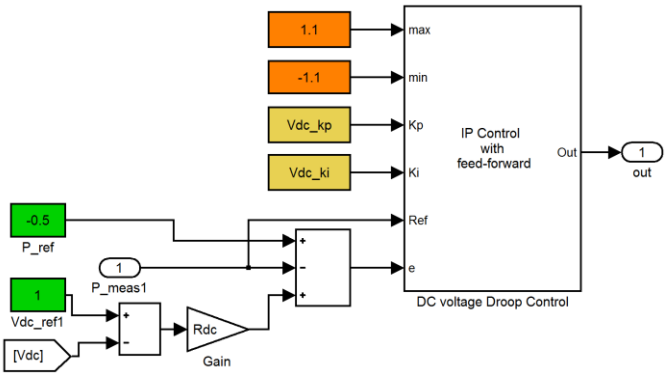


Figure 12: Implemented DC voltage droop controller

A. High Level Controller Calibration and Validation

High level controller parameters are calibrated and validated for the point-to-point test system depicted in Fig. 4 with the controller parameters listed in Table 2 in Section III.

A step change is applied in the Active power reference value of VSC1 from 1 to 0.5 p.u at 2 s for the active power controller calibration. The integral gain value (*Ki*) is increased in each simulation, and the active power responses on both converters are presented in Fig. 13. *P_Ki* = 10 is chosen as it provides less overshoot and undershoot.

In order to obtain calibrated parameters for the DC voltage controller, a step change in the dc voltage reference value from 1 to 0.8 p.u at 2 s is applied. Simulation results are shown in Fig. 14 for several values of the proportional (*Kp*) and integral gain (*Ki*). *Vdc_Kp* = 15 and *Vdc_Ki* = 300 are chosen given the small settling time of the controller response.

Similarly, a step change in reactive power reference value from 0 to 0.3 p.u is applied at 2 s at VSC1 side and simulations with increasing values of the integral gain (*Ki*) are performed to obtain the tuned gain value for the reactive power controller, simulation results are shown in Fig. 15.

In Fig. 15, the reactive power controller gives a smaller settling time for *Q_Ki* = 20 than *Q_Ki* = 15, but considering a 30% maximum overshoot, *Q_Ki* = 15 is chosen.

Table 3 Converter parameters for four-terminal test system

Control strategy	Converter	Control mode	Parameter set value
With DC voltage droop controller	VSC1 (rectifier)	P,Q	$P^* = 0.5\ p.u$ $Q^* = 0\ p.u$
	VSC2 (rectifier)	P,Q	$P^* = 0.5\ p.u$ $Q^* = 0\ p.u$
	VSC3 (inverter)	DC voltage droop, Q	$P^* = -0.5\ p.u$ $u^*_{dc} = 1\ p.u$ $Q^* = 0\ p.u$ $R_{dc} = \frac{1}{0.04}$
	VSC4 (inverter)	DC voltage droop, Q	$P^* = -0.5\ p.u$ $u^*_{dc} = 1\ p.u$ $Q^* = 0\ p.u$ $R_{dc} = \frac{1}{0.04}$
Without DC voltage droop controller	VSC1 (rectifier)	P,Q	$P^* = 0.5\ p.u$ $Q^* = 0\ p.u$
	VSC2 (rectifier)	P,Q	$P^* = 0.5\ p.u$ $Q^* = 0\ p.u$
	VSC3 (inverter)	u_{dc} ,Q	$u^*_{dc} = 1\ p.u$ $Q^* = 0\ p.u$
	VSC4 (inverter)	P,Q	$P^* = -0.5\ p.u$ $Q^* = 0\ p.u$

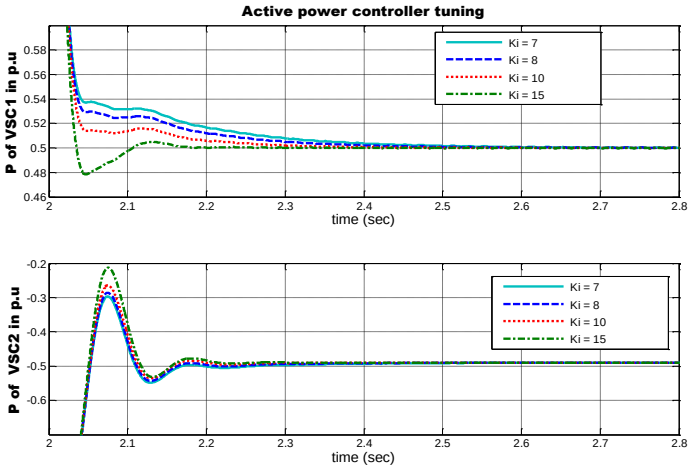


Figure 13: Active power flow of the converters

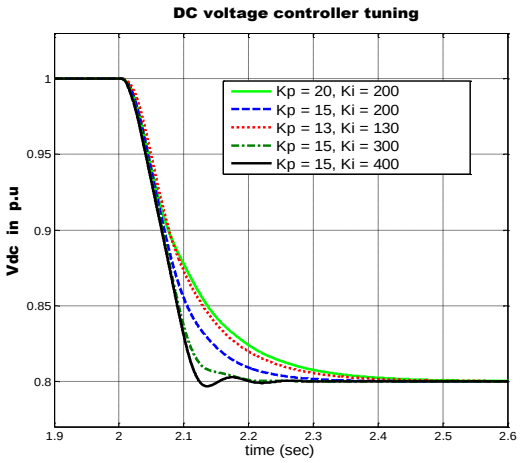


Figure 14: DC voltage

Table 4 PI controller parameters for different topologies

Parameter	Point-to-point test system	Four-terminal test system
P_Ki	10	15
Vdc_Kp	15	15
Vdc_Ki	300	200
Q_Ki	15	15

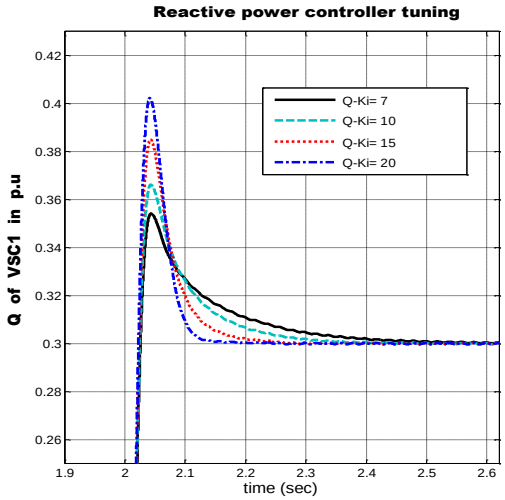


Figure 15: Reactive power flow of VSC1

The calibrated parameters for both point-to-point and four-terminal test systems are listed in Table 4. *Vdc_Kp*,*Vdc_Ki* are DC voltage controller proportional and integral gains; *P_Ki* and *Q_Ki* are active and reactive power controller integral gains.

B. Enhanced Controller Validation

The impact of using a DC voltage damping conductance is studied in the point-to-point test system under an unbalanced fault condition. An unbalanced fault is applied in the ac side of VSC1 at 2 s and clears at 2.5 s. The damping conductance (G_a) is computed to provide damped dc voltage behavior under fault conditions. From the simulation results shown in Fig. 16, it can be observed that with increasing conductance values the dc voltage damping improves, however the response time of the controller increases. Therefore, G_a = 10 is chosen, noting that greater values result in small (damped) oscillations.

To compare the performance of the negative sequence current controller against the conventional current controller, a single phase to ground fault is applied at 2 s and cleared at 2.5 s in the ac side of VSC1 in the point-to-point test system. Simulation results in Fig. 17 shows a significant improvement in the active power and dc voltage during unbalanced fault condition after using the negative sequence current controller. The bottom plot in Fig. 17 shows that the negative sequence current is kept at zero during the fault.

The dc voltage droop controller is assessed using the four-terminal test system of Fig. 5, where two converter stations act as rectifiers and the other two stations as inverters. In addition, the performance of the droop controllers are compared with the conventional DC voltage controller by considering the loss of converter station VSC2 at 2 s; simulation results are presented in Fig. 18, where P1, udc1 represents active power flow and dc voltage in VSC1 station and similarly for P2-P4 and udc2-udc4.

The controller parameters and the mode of operation set for conducting simulations in the four-terminal test system are listed in Table. 5. From the simulation results it can be observed that VSC1 and VSC2 provide 50% of the power to the system until 2 s. After 2 s, VSC2 is lost and only VSC1 provides 50% power. The dc voltage droop controller facilitates active power sharing between VSC3 and VSC4 by 25% when VSC2 is lost at 2 s, and therefore, dc voltage level of the terminals are reduced to 0.99 p.u. from 1 p.u. The change of dc voltage can be defined by the R_{dc} value. However, without dc voltage droop controller (conventional DC voltage control), the control systems attempt to keep the dc voltage level at the reference value of 1 p.u as shown in Fig. 18. After losing VSC2 at 2 s all of the power is consumed by VSC4 (active power), and thus, there is no active power flow in VSC3.

Offline simulation times for the three different topologies implemented in Simulink are varied; they depend on control loops, arithmetic operations and increase of converter terminals which are listed in Table 5. The total duration of the simulation is 5 s, noticeable speed-up is gained using real-time simulation when model complexity and size increases.

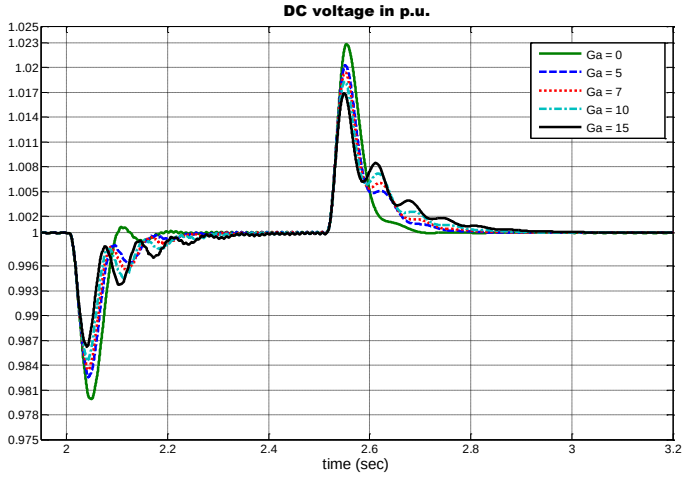


Figure 16: DC voltage for different damping conductances

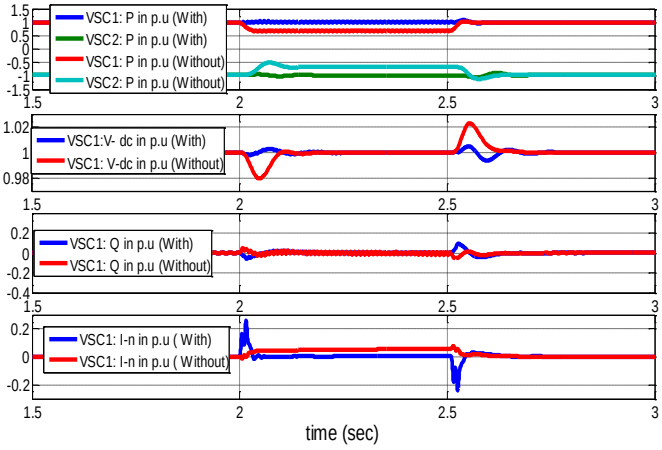


Figure 17: Negative sequence current controller response

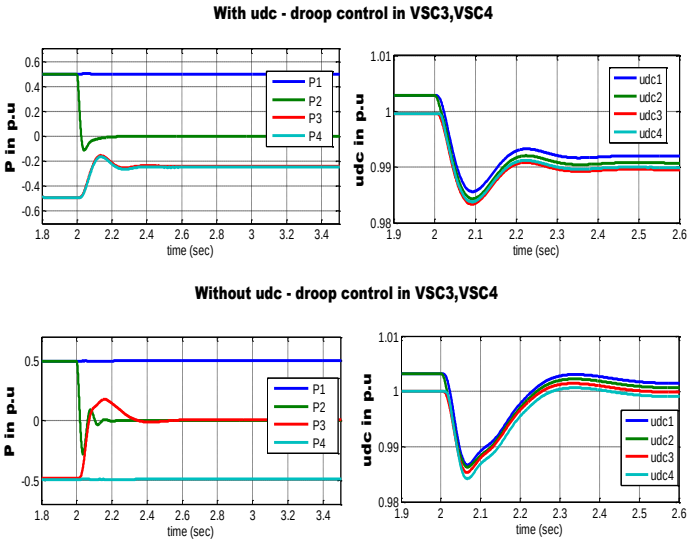


Figure 18: Controller responses in Four-terminal test system

Table 5 Offline and Real-time simulation time

Topology	Off-line (s)	Real-time (s)	Speed-up (%)
Point-to-point	100	5	20%
Point-to-point with Neg. Seq. controller	205	5	41%
Four-terminal	360	5	72%

Note: For off-line simulation, the computer used was a standard PC with the Windows 7 OS, Intel Core i5-2450M, 2.50 GHz Processor, and 4GB RAM.

V. Real-time Simulation

A. Model preparation for RT Simulation

This section describes how the simulation models have been prepared to make them compatible for real-time simulation using OPAL-RT's eMegaSim target. Only the point-to-point model preparation for real-time simulation is shown in Fig. 19. The models built in Simulink are regrouped in to a console, master and slave sub-systems. In the console (shown in Fig. 20), all user interface blocks such as scopes, displays, and switches are grouped for user interaction. The master includes computational elements, mathematical operation blocks, I/O blocks etc. The rectifier, voltage source, and controllers are placed inside the master sub-system as shown in Fig. 20. The slave sub-system is comprised by all inverter side elements and are identical to the master sub-system, hence, not shown here. Opcomm blocks from OPAL-RT's Simulink library are used to enable and save the communication setup between subsystems and are placed before all subsystem input signals [11].

Real-time simulations were carried out with similar test scenarios as in Section IV, and show similar controller behavior.

B. Simulation Results

Results of the active power, reactive power, DC voltage and enhanced controller real-time simulation are shown in this section. Simulation results of Fig. 21 (i), (ii),(iii),(iv),(v) are for point-to-point and Fig. 21 (vi) for four-terminal test system.

In Fig. 21(i), active power reference changes from 1 to 0.5 p.u at 5 s and set back to 1 p.u at 7 s. In Fig. 21(ii), reactive power reference of VSC2 changes from 0 to 0.3 p.u at 25 s and set back to 0 p.u at 27 s. DC voltage change from 1 to 0.9 p.u is applied at 15 s and set back to 1 p.u at 17 s is shown in Fig. 21(iii).

An unbalanced fault is applied at 45 s and cleared at 45.20 s for both with and without negative sequence controller and results are shown in Fig 21 (iv) and (v). In Fig 21 (v), active power reference value of VSC1 changes from 0.5 to 0.3 p.u at 5 s and set back to 0.5 p.u at 7 s.

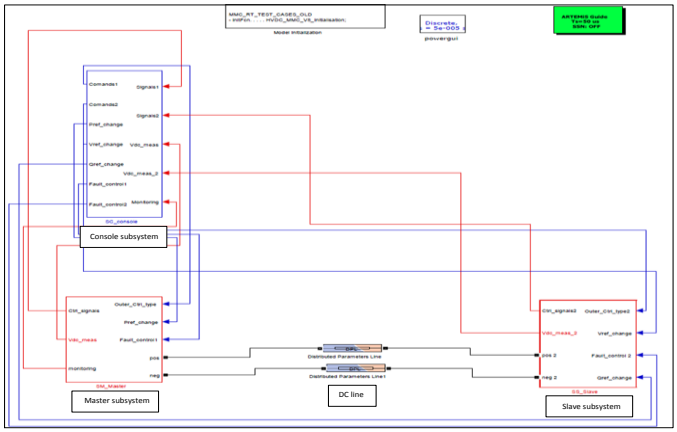
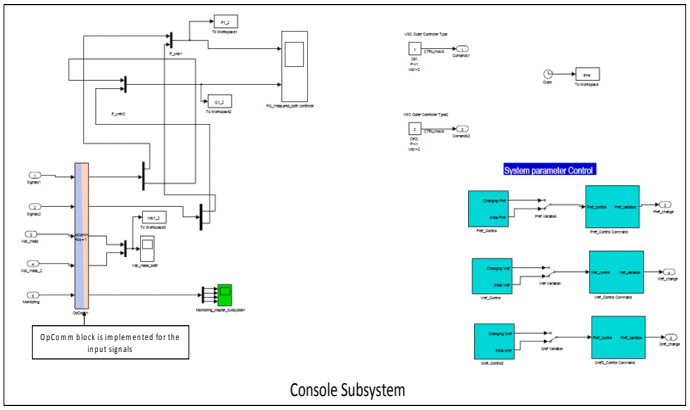


Figure 19 Modified point-to-point Simulink model for Real-time simulator



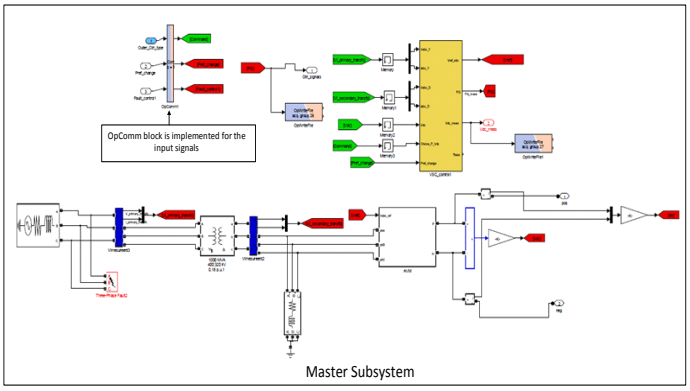
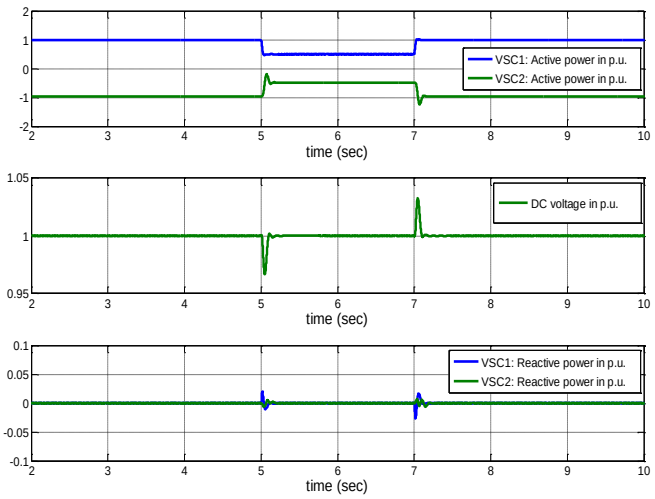
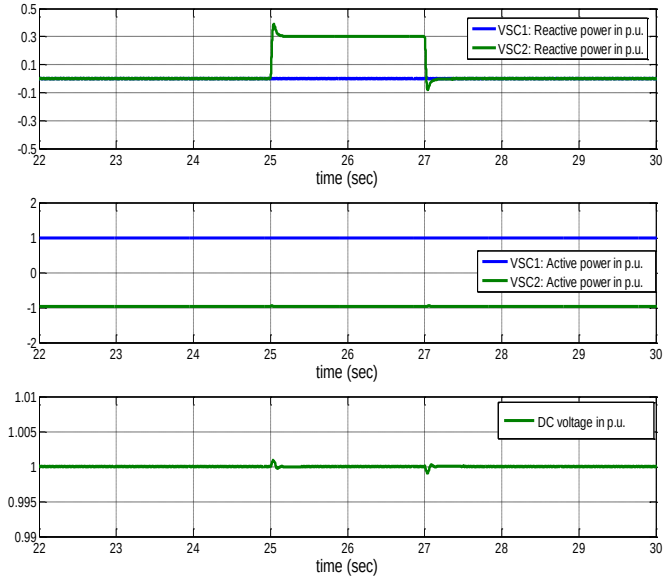


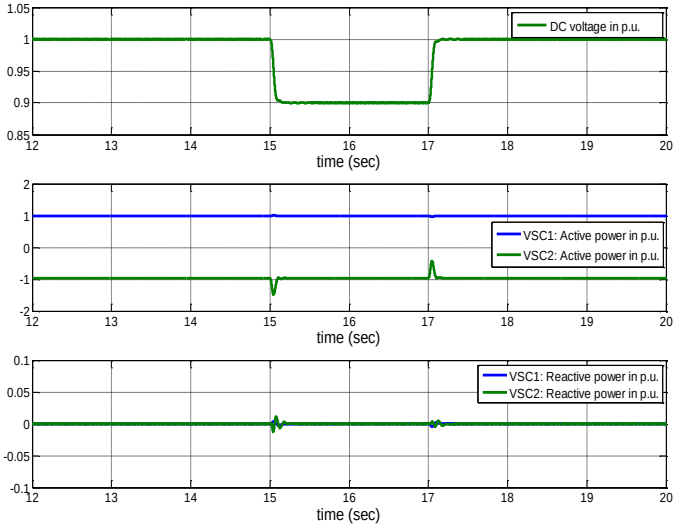
Figure 20 Console (upper) and master sub-system (bottom) implemented block diagram



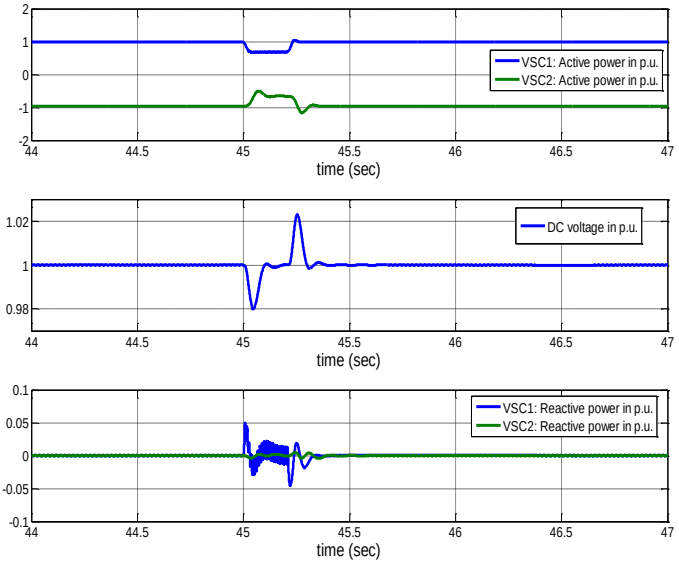
(i) Active power controller validation



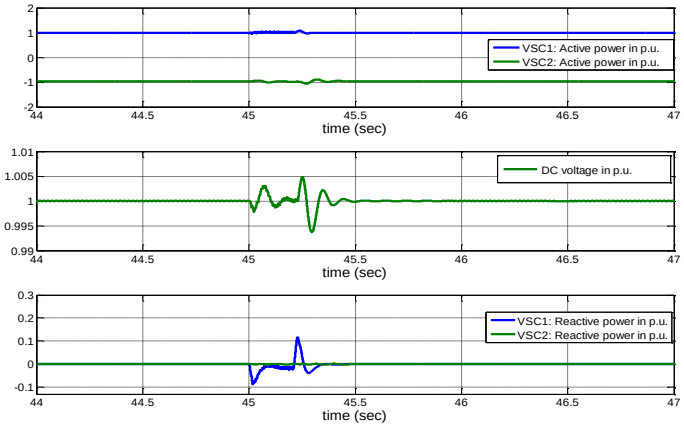
(ii) Reactive power controller validation



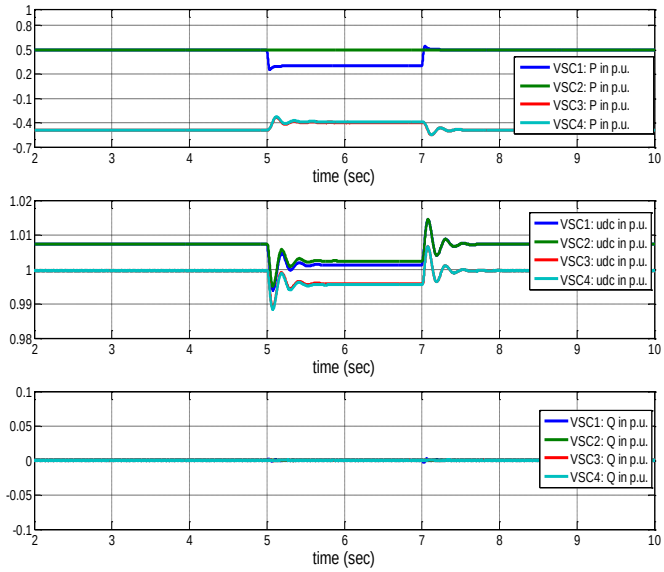
(iii) DC voltage controller validation



(iv) Unbalanced fault with conventional inner current controller



(v) Unbalanced fault with Neg. Seq. current controller



(vi) DC voltage droop controller validation

Figure 21: Real time simulation results for the point-to-point and four-terminal DC networks

C. Simulation Performance Analysis

Computational performance of the real-time simulations can be obtained from the information provided by the Opcomm monitoring block of RT-Lab library. Only the performance results for the four-terminal test system are shown here. Fig. 22 shows that the highest computational time is 10 (µs).

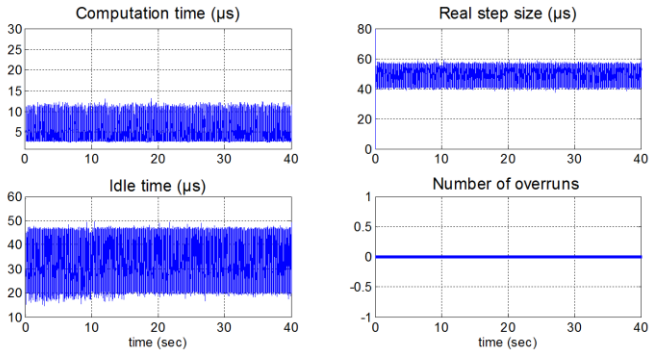


Figure 22: Real-time simulation performances

The computational time observed from Fig. 22 is much smaller than the step size which is 50 (µs), consequently there is still space to reduce the step size or to increase model complexity. Indeed, as four-terminal have been simulated in the real-time simulator with 10 (µs), and assuming linearity, with a time step of 50 (µs) a total 20 terminals could be simulated. Moreover, zero overruns shows that the test system has been simulated in real-time without any computational issues.

VI. Conclusion

This article shows that the response of the dc voltage, active power and reactive power controllers are swift and effective. However, it is shown that by modeling the damping effect of the dc voltage controller, the improvement of the dc voltage control during faults will be more difficult. This illustrates that proper modeling of high level VSC-HVDC controls is relevant for simulation studies on DC grids.

The article also indicates that the negative sequence current controller significantly improves the active power and dc voltage during unbalanced fault conditions. The dc voltage droop controller facilitates active power sharing between converter stations and also improves the performance of the multi-terminal VSC-HVDC system in case any converter is lost. Thus, the results in this paper show that when modeling high level controls of VSC-HVDC systems, negative sequence current and dc voltage droop controls should always be included.

It is worth noting that both test systems applied in this article have strong AC sources, which might be a potential limitation for our proposed generic high level control models [12], [13], [14]. More work will be carried out in the future to explore the effect of weak AC source on our high level controllers for VSC-HVDC grids.

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