Experiences with Dynamic PMU Compliance Testing using Standard Relay Testing Equipment

Jako Kilter Ivo Palu

Department of Electrical Power Engineering Tallinn University of Technology Tallinn, Estonia jako.kilter@ttu.ee

Abstract— This paper presents the results of dynamic compliance testing of phasor measurement units (PMUs) from three different vendors in a laboratory environment. Testing is performed by providing three phase voltage and current injections to the VT and CT inputs of the PMUs through Freja-300 stand-alone protection relay test set. Testing is performed according to the standard "IEEE C37.242-2013 - IEEE Guide for Synchronization, Calibration, Testing, and Installation of Phasor Measurement Units (PMUs) for Power System Protection and Control". The paper discusses the test setup, testing process, calculation of performance evaluation parameters and overall test results of this project.

Index Terms—Phasor Measurement Units, PMU calibration testing, stand-alone testing, synchrophasors.

I. INTRODUCTION

The reliability of power system applications based on synchrophasors leans on the accuracy of PMUs for phasor calculation and frequency estimation. The IEEE standard for Synchrophasor Measurements for Power Systems (IEEE C37.118.1-2011) [1] specifies requirements for PMUs for both steady state and dynamic operating conditions. The companion standard IEEE C37.118.2-2011 covers communication aspects of synchrophasor data transfer. Another standard "IEEE C37.242-2013 - IEEE Guide for Synchronization, Calibration, Testing, and Installation of Phasor Measurement Units (PMUs) for Power System Protection and Control" [2] provides guidance for test and calibration procedures for PMUs for laboratory and field applications. This paper presents results from dynamic compliance testing of PMUs from three different vendors as specified by the above mentioned standards. Results of the steady-state testing were reported in [3].

This paper covers the topic of dynamic compliance testing of PMUs. The paper is organized as follows: Section II provides information about the testing equipment and the architecture for PMU testing. Section III discusses PMUs performance evaluation criteria for dynamic compliance testing. Section IV presents results of frequency ramp, magnitude step and unbalanced condition tests performed with PMUs from three different vendors. Finally in Section V, conclusions are drawn and experiences together with lesson learnt from the project are summarized.

This work was supported in part by Nordic Energy Research through the STRONg²rid project and by Statnett SF, the Norwegian TSO. Support from Elering AS, Estonian TSO, and from Tallinn University of Technology under grant B22, are appreciated. Muhammad Shoaib Almas Luigi Vanfretti Electric Power Systems Department KTH Royal Institute of Technology Stockholm, Sweden msalmas@kth.se, luigiv@kth.se

II. PMU TESTING ARCHITECTURE

This section presents the details of the testing equipment, Freja-300 [4], used for this study. It is a standard stand-alone test set intended for protection relay testing. This test set can generate 4 \times 150 V (82 VA) and 3 \times 15 A (87 VA) or 1 \times 45 A (250 VA). The inaccuracy guaranteed for the voltage and current generations by the test set is (± 0.01 % of range) + (± 0.05 % of reading) which is within the accuracy limits for testing equipment specified by IEEE C37.242-2013 [2] which states that the uncertainty of test equipment should be lesser than 10% of the allowed error. The test set facilitates injecting harmonics, faults and unbalanced voltage / currents / frequency to the device under test.

The reporting rate of 50 frames per second is considered for all PMUs in this study while TCP is used as transport layer protocol for streaming out synchrophasors from PMUs over Ethernet. In order to perform dynamic testing of the PMU under test, at least two sequences are required: a steady state sequence for a specific period of time followed by the disturbance sequence which can be step change in voltage/current magnitude or phase angles along with frequency change. The three phase voltage and current injections are provided to the voltage and current input modules of the PMU under test. The voltage and current injections are set by using software interface [5] of the test set on the workstation which is serially connected to the test set. The PMU receives the analog inputs and streams out synchrophasor measurements through its Ethernet port. The PMU measurements are received in a Phasor Data Concentrator (PDC) to archive all the synchrophasor measurements as a CSV file for further analysis using MATLAB. The overall test setup illustration can be seen in [3]. The PMU is time synchronized by acquiring IRIG-B [6] signals from substation clock [7] which is connected to the GPS antenna. For all the PMUs, synchrophasors for positive sequence and all phases for both voltage and currents were acquired.

Some commercial protection relay test sets do have the provision to send time synchronization signals to the device under test in order to synchronize the whole testing process. However this feature is not available in the test set used in

this study and therefore IRIG-B signals were provided to the PMU by using substation clock. The reference phasors are calculated by injecting the three phase voltage and currents from the test set to a calibrator developed on National Instrument's based Compact Reconfigurable I/O controller (NI-cRIO) with 24-bit resolution of current and voltage modules and a GPS clock accuracy of $\pm 100 \mathrm{ns}$. The calibrator is configured to compute reference phasors based on interpolated DFT synchrophasor estimation algorithm reported in [8] with known uncertainties for magnitude and phase angle computations 1 .

III. PMU DYNAMIC TESTING PRINCIPLES

IEEE standard C37.118.1 recommends several tests to comprehensively analyse the dynamic performance of the PMUs along with their associated performance evaluation criteria. These tests include positive/negative step to the magnitude of input signal, positive/negative step to the phase of input signal, PMU response towards ramp of system frequency and measurement bandwidth.

In this paper, some additional tests that are not in the present standard like PMU dynamic performance testing with unbalanced conditions are also performed. Table I presents different tests performed on PMUs from three different vendors for their dynamic performance evaluation. These performance evaluation parameters are explained in the IEEE Standard C37.118.1-2011 [1].

#	Test Name	Parameter	System Condition	Performance
#	1 est Ivame	Changed	System Condition	Evaluation Evaluation
1	Positive	Frequency	System is balanced	FE, RFE
	Frequency	ramp up	at nominal frequen-	
	Ramp	(50 to 51 Hz)	cy	
2	Negative	Frequency	System is balanced	FE, RFE
	Frequency	ramp down	at nominal frequen-	
	Ramp	(50 to 49 Hz)	cy	
3	Magnitude	10% balanced	System is balanced	TVE, Response
	Positive	voltage	at nominal frequen-	Time, Delay
	Step	magnitude step	cy	Time, % Peak
		up		Overshoot
4	Magnitude	10% balanced	System is balanced	TVE, Response
	Negative	voltage	at nominal frequen-	Time, Delay
	Step	magnitude step	cy	Time, % Peak
		down		Overshoot
5	Magnitude	10% voltage	System is unbal-	TVE
	Step	magnitude step	anced at nominal	
	Unbalanced	in phases A	frequency	
		and C		

TABLE I. PMU DYNAMIC COMPLIANCE TESTS

IV. PMU TESTING RESULTS

A. Positive Frequency Ramp

PMU performance during system frequency change is tested with a positive ramp of frequency applied to balance three phase input signals (voltages and currents) to the PMUs under test. The frequency of the input signals is kept constant at 50 Hz which is followed by a frequency positive ramp at 1Hz/sec. The results are shown in Fig. 1. FE during

a frequency positive ramp shows that PMU A and PMU B meets this requirements, however PMU C violates this criteria and has a maximum FE of -0.0091Hz which is well above the allowable limit of ± 0.005 Hz. In case of RFE, only PMU A satisfies the requirement while both PMU B and PMU C violates this criteria with a maximum RFE of 0.095 Hz/sec and 0.05 Hz/sec which is much larger than the allowable RFE limit of ± 0.01 Hz/sec

B. Negative Frequency Ramp

In a similar way a negative frequency ramp is applied to balanced three phase input signals (voltages and currents) to the PMUs under test. The frequency of the input signals is kept constant at 50 Hz which is followed by a frequency negative ramp at 1Hz/sec. The results are shown in Fig. 2. FE during a frequency negative ramp shows that none of the PMUs meet the requirement for FE. PMU A, PMU B and PMU C show a maximum FE of -0.0009, -0.0057 and -0.0177, respectively which is much larger than the allowable FE limit of ±0.005 Hz. PMU B fails the FE criteria with a very small margin. In case of RFE, only PMU A fulfils the criteria. However it shows a straight line, which doubts the performance of the PMU when subjected to a negative frequency ramp. PMU B and PMU C shows a maximum RFE of 0.075 Hz/sec and 0.015 Hz/sec respectively, thus violating the allowable RFE limit of ±0.01 Hz/sec. PMU C fails the RFE criteria with a small margin.

C. Magnitude Positive Step (Balanced)

PMUs performance to a step change is evaluated at a single reporting rate of 50 msgs/sec. The influence quantity which is stepped is three phase voltage magnitude by 10% at system nominal frequency (50 Hz). %TVE, delay time, response time and % peak-overshoot is calculated for each PMU using the definitions discussed in Section III. Fig. 3 (plots d-f), shows the %TVE of all the PMUs for each phase and positive sequence measurement when subjected to a positive step change in voltage input magnitude (Fig. 3 plots a-c). All the PMUs violate the TVE limit of 1% during the time the step is applied to the voltage magnitude. However, once the post-step steady-state is reached, the %TVE of all the PMUs fall back within the limit. Response time, delay time and % peak overshoot is also calculated for each of the PMU. Fig. 4 shows calculation of these parameters for phase C of PMU C. Table II shows the results of these performance parameters for these PMUs. All the PMUs satisfy the requirements for response time and peakovershoot with PMU A having the best performance. However all the PMUs violate the limit of delay time.

D. Magnitude Negative Step (Balanced)

Similar to magnitude positive step, the PMUs performance is evaluated when subjected to a negative step in the voltage magnitude at nominal system frequency. Fig. 3 (plots j-l) shows the %TVE of all the PMUs for each phase and positive sequence measurement when subjected to a negative step change in voltage input magnitude (Fig. 3 plots g-i). All the PMUs violate the %TVE limit of 1% during the time the step is applied to the voltage magnitude. However, once the post-step steady-state is reached, the %TVE of all the PMUs fall back within the limit. Table-III shows the results of response time, delay time and % peak overshoot for these PMUs. All the PMUs satisfy the requirements for response time and peak-overshoot with PMU A having the best performance. However all the PMUs violate the limit of delay time. As compared to the

¹ According to the IEEE Standard C37.118.1-2011, a reference PMU should justify 1/10 of the accuracy limits as specified by the standard. The interpolated DFT based synchrophasor estimation algorithm deployed on an FPGA-based controller yields TVE and FE results within 1/10 of the accuracy limits for frequency sweep dynamic test and amplitude and phase modulation.

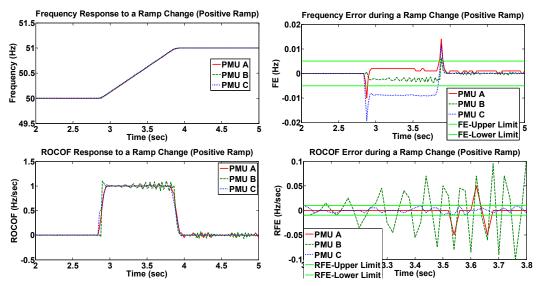


Fig. 1. PMUs response to a positive frequency ramp change. Top-left figure shows the frequency measured by the PMUs. Top-right shows the FE calculated by using (2). Bottom-left shows the ROCOF reported by the PMUs when subjected to the frequency ramp up. Bottom-right shows RFE calculated using (2). PMU C violates FE limits while PMU B and PMU C violate RFE criteria.

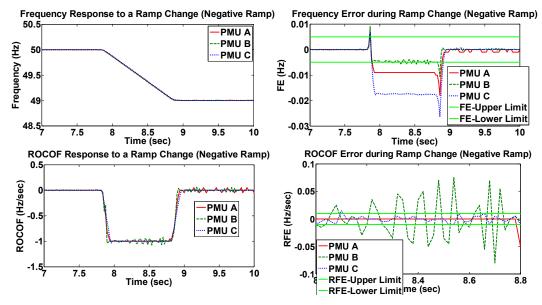


Fig. 2. PMUs response to a negative frequency ramp change. Top-left figure shows the frequency measured by the PMUs. Top-right shows the FE calculated by using (2). Bottom-left shows the ROCOF reported by the PMUs when subjected to the frequency ramp up. Bottom-right shows RFE calculated using (2). All PMUs violate FE limits while only PMU B satisfies the RFE criteria.

magnitude positive step, all the PMUs show a better response and delay time and lower %peak-undershoot when subjected to a magnitude negative step.

E. Magnitude Step (Un-balanced)

This is an additional test performed to evaluate the dynamic measurement performance of the PMUs. At nominal system frequency, the voltage magnitude of Phase A is increased by 10% and of Phase C is decreased by 10% simultaneously without affecting Phase B. This leads to an unbalanced power system condition. This typical imbalance results in the system frequency of 49 Hz. Thus this scenario can be used to determine the effect of both voltage magnitude steps (positive/negative) along with their subsequent effect on system frequency as measured by the PMUs. %TVE is considered for PMU's performance evaluation. Fig. 5 shows the measurement comparison of Phase C (on-

ly) and frequency as computed by all the PMUs. From Fig. 5, it can be noticed that when the PMUs are subjected to an unbalanced condition following a balanced steady state, they show interesting characteristics. From the plot of voltage magnitude measurement (Fig. 5-a), PMU A measures incorrect measurement for almost 1.5 sec and then settles to a steady state correct value. For this reason, its %TVE violates the limits even when both PMU B and PMU C settle within the limits. Such a behavior of a PMU can negatively affect the monitoring, protection and control applications based on the PMU measurements. From the frequency plot (Fig. 5-c), PMU C shows a bit slower response while PMU B shows a slight overshoot and undershoot in frequency measurement when subjected to an unbalance condition. The ROCOF plot (Fig. 5-d) shows a repetitive waveform by PMU B (about 2 Hz) due to which its ROCOF exceeds the RFE limits periodically even in a post-disturbance steady-state condition.

TABLE II. PMU PERFORMANCE REQUIREMENT ANALYSIS FOR MAGNITUDE POSITIVE STEP CHANGE

TABLE III. PMU PERFORMANCE REQUIREMENT ANALYSIS FOR MAGNITUDE NEGATIVE STEP CHANGE

PMU Name	Evaluation Parameter	Results	Allowable Limit
	Response Time (sec)	0.102	0.199
PMU A	Delay Time (sec)	0.032	0.005
	Peak-Overshoot (%)	0.310	10
	Response Time (sec)	0.106	0.199
PMU B	Delay Time (sec)	0.048	0.005
	Peak-Overshoot (%)	1.015	10
	Response Time (sec)	0.116	0.199
PMU C	Delay Time (sec)	0.045	0.005
	Peak-Overshoot (%)	1.99	10

PMU Name	Evaluation Parameter	Results	Allowable Limit
	Response Time (sec)	0.065	0.199
PMU A	Delay Time (sec)	0.056	0.005
	Peak-Undershoot (%)	-0.225	-10
	Response Time (sec)	0.075	0.199
PMU B	Delay Time (sec)	0.031	0.005
	Peak-Undershoot (%)	-0.415	-10
	Response Time (sec)	0.095	0.199
PMU C	Delay Time (sec)	0.028	0.005
	Peak-Undershoot (%)	-0.882	-10

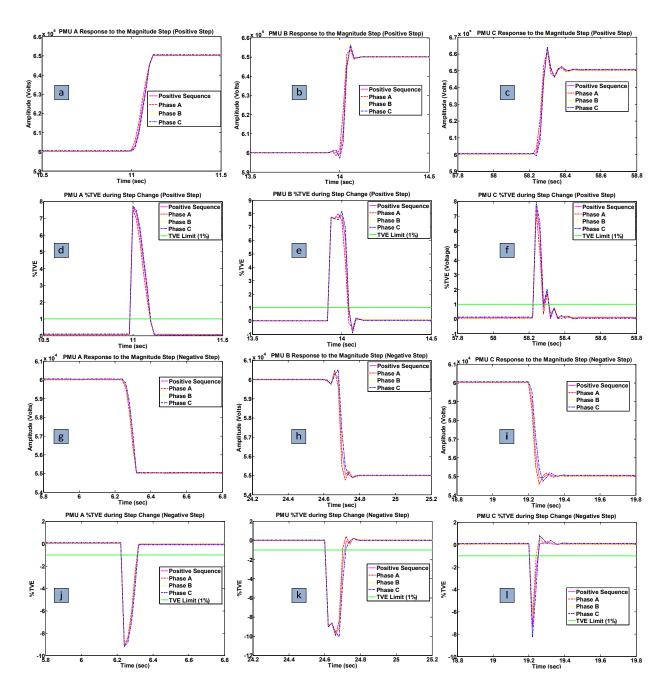


Fig. 3. PMUs response to a ±10% positive magnitude step change. All the PMUs violate the %TVE limit (1%) during the step. Once the steady state is reached after the step, the TVE falls back within the limit of 1% for all the PMUs. Plots (a-c) refer to the positive step of 10% on all phases of the voltage magnitude input to the PMUs while plots (d-f) refer to their corresponding %TVE. Plots (g-i) refer to the negative step of 10% on all phases of the voltage magnitude input to the PMUs while plots (j-l) refer to their corresponding %TVE.

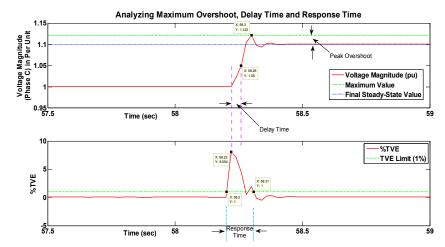


Fig. 4. Performance evaluation parameters calculation for Phase C of PMU C showing response time of 0.116 sec, delay time of 0.045 sec and the % peak-overshoot of about 2%. PMU C does not satisfy the criteria for delay time.

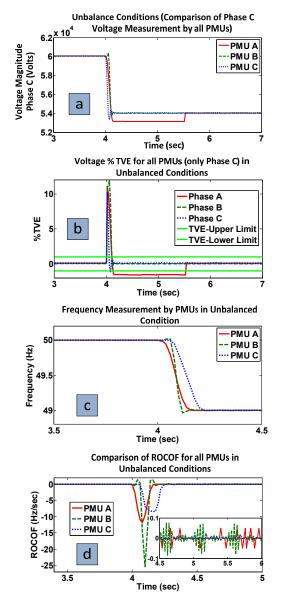


Fig. 5. PMUs response when subjected to a dynamic unbalance condition. Magnitude of phase A is stepped up by 10% while magnitude of phase C is stepped down by 10%. Top-left shows voltage magnitude of Phase C as computed by all the PMUs. Top-right is %TVE computed by using (2). Bottom-left is the frequency measured by all the PMUs. Bottom-right is ROCOF of all the PMUs in an unbalanced condition.

V. CONCLUSIONS

The PMU dynamic compliance testing process is presented for testing the accuracy of PMUs from three different vendors according to the requirements specified in the standard IEEE C37.118.1-2011 and IEEE C37.242-2013. Tests specified in the standard like frequency ramp and magnitude step along with an additional test for unbalanced conditions are carried out by using a standard protection relay test-set. The comparison of these PMUs is made on the basis of the Total Vector Error (TVE), Frequency Error (FE), Rate of Change of Frequency (ROCOF) measurement, ROCOF measurement Error (RFE) calculations, % peak-overshoot, response time and delay time as specified in the standard.

All the PMUs failed most of the dynamic compliance tests performed. When subjected to an unbalanced condition on a fly, one of the PMU measured incorrect voltage phasor for almost 1.5 sec. The dynamic compliance measurement bandwidth is not conducted in this study mainly due to some limitations of the test-set, which requires amplitude and phase modulation. This test will be performed by using Real-Time Hardware-in-the-Loop (RT-HIL) facility at SmarTS-Lab.

REFERENCES

- [1] IEEE Standard for Synchrophasor Measurements for Power Systems, IEEE Std C37.118.1-2011, Dec. 2011.
- [2] IEEE Guide for Synchronization, Calibration, Testing, and Installation of Phasor Measurement Units (PMUs) for Power System Protection and Control, IEEE Std C37.242-2013, Mar. 2013.
- [3] M. S. Almas, J. Kilter, and L. Vanfretti, "Experiences with Steady-State PMU Compliance Testing using Standard Relay Testing Equipment", in *Proc. 2014 IEEE Electric Power Quality and Supply Reliability Conf.* (PQ), Tallinn, Estonia, June 2014.
- [4] Megger, "Freja 300 Relay Test System," available on-line: http://tinyurl.com/Freja300.
- [5] Megger, "Freja Win- Graphical interface for Freja-300 test set", available on-line: http://tiny.cc/Freja-Win.
- [6] IRIG Standard 200-04, IRIG serial time code format, September 2004, available online: http://www.irigb.com/pdf/wp-irig-200-04.pdf
- [7] Arbiter, "GPS Substation Clock Model 1094B", available on-line: http://www.arbiter.com/catalog/product/model-1094b-gps-satellite-precision-time-clock.php.
- [8] P. Romano, and M. Paolone, "Enhanced Interpolated-DFT for Synchrophasor Estimation in FPGAs: Theory, Implementation, and Validation of a PMU Prototype", IEEE Transactions on Instrumentation and Measurement, vol. 63, no. 12, pp. 2824-2836, May 2014.