PERFORMANCE EVALUATION OF PROTECTION FUNCTIONS FOR IEC 61850-9-2 PROCESS BUS USING REAL-TIME HARDWARE-IN-THE-LOOP SIMULATION APPROACH

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ABSTRACT

With the evolution of Process Bus (IEC 61850-9-2), there is a need to assess the performance of protection schemes using process bus against those where traditional copper wires are implemented. Differential protection is the fundamental and most commonly used protection for transformers, motors and generators. In this paper a power system is modelled in SimPowerSystems and is executed in real-time using Opal-RT's eMEGAsim real-time simulator. Hardware-in-the loop validation of a process bus implementation for differential protection for a two winding transformer is done by using the differential protection feature in ABB's RED-670 relay. The event reports generated by the ABB relay during Hardware-in-the-Loop testing are compared for three different scenarios i.e. complete process bus, hybrid process bus and complete traditional topology.

I. INTRODUCTION

IEC 61850-9-2 Process Bus defines the data transfer between primary equipment and IEDs through a Ethernet network. This eliminates the need of costly copper wires and facilitates interoperability between equipment from different vendors in a substation [1]. Protection relay manufacturers are adding the feature of Sampled Values in their IEDs. The reliability of process bus is still being analysed and some pilot projects are being implemented world-wide to evaluate its performance as compared to the traditional copper wiring architecture.

Real-time simulators (RTS) are currently being used to simulate large power systems and to analyze their behavior in both steady state and faulted states. These RTSs are equipped with Analog and Digital I/Os and can be interfaced with real devices. Such kind of approach is called RT HIL simulation [2]. This approach allows performing complete functional testing of the protection relays. In this case an accurate model of the power system where the relay is to be placed is modeled and simulated in RT using the RTS with the actual hardware (protection relay) as HIL. The key benefit in RT HIL protection relay testing is that the impact of the fault on the entirety of the power system can be analyzed and the overall protection schemes including the backup protections, system integrity protection schemes (SIPS), Remedial Action Schemes (RAS) can be verified.

This paper presents a real-time Hardware-in-the-loop approach for assessing protection features through process bus implementation. Differential protection feature of ABB RED-670 [3] is evaluated for a two winding transformer model executing in the real time using eMEGAsim Opal-RT real-time simulator [4]. An assessment of differential protection is made by contrasting three cases;

1. Complete Traditional Topology: Analog current values for both primary and secondary side of the transformers are provided to the ABB RED-670 using traditional copper wiring. The MATLAB/Simulink model of a power system with two winding transformer is executed in real-time and three phase to ground fault is applied on primary side of the transformer to observe the tripping times for the differential operation. This represents the typical scenario of traditional power substations.
2. Hybrid Process Bus Topology: For the second case, the current values of the primary side of the transformer are presented to the ABB RED 670 using sampled values while the secondary side is kept hardwired. Opal-RT's RTS has the capability to simulate a Merging Unit inside it and stream out the Sampled Values (SV) for the voltages and currents at the buses of the model executing in the real-time. Similar faults are applied in the simulated power system model as in case 1 and the tripping times are computed. This exhibits the scheme of a hybrid power substation where traditional equipment is kept as such and the new merging unit is placed at a new bay (secondary side of transformer). This case is significantly important to study as most of the substations are expanding to meet power supply demands. In addition, the new equipment (IEDs / CT/ VTs) being supplied by the vendors are IEC-61850 compliant. This puts a requirement to exploit these features in order to make the substation more reliable, flexible and interoperable.
3. Complete Process Bus Topology: For the third case, both the primary and secondary current values at the transformer are presented to the ABB RED-670 as sampled values. A similar fault is applied as in case 1 and case 2 and the tripping times are computed. This scenario represents a new substation with all the equipment compliant to IEC 61850. This test is important to evaluate the selectivity and sensitivity of the protection IED which is being supplied of analog measurements from sampled values.

The remainder of the paper is arranged as follows. Section II presents the details of the design of test system modelled in SimPowerSystems (MATLAB / Simulink). Section III focuses on three different test scenarios and their results. Finally in Section IV, conclusions are drawn and the future work is outlined.

II. TEST CASE IN SIMPOWERSYSTEMS

Fig. 1 shows the single line diagram of the test case model designed in SimPowerSystems (MATLAB / Simulink) to investigate the performance of differential protection relay with both hardwired and process bus (IEC 61850-9-2) implementation. The major components of the test case are:

- Three phase voltage source, 50Hz, 11 kV
- Transmission Line (π-section), 2 km
- Step up transformer (11kV / 40 kV), 50 MVA
- Three phase fault block to introduce three phase to ground fault on the primary side of the transformer.
- Circuit breaker to disconnect load with trip signals from the differential protection relay
- Three phase series RLC load of 20 MW
- Simulation time step = 50 μ sec.

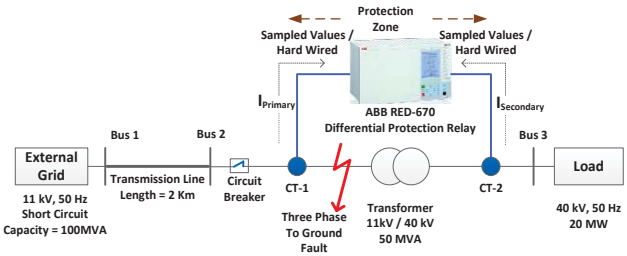

Fig. 1. Single Line Diagram of the Test Case

ABB's RED-670 can be configured for a two winding transformer differential protection by using its application configuration tool PCM600 [5]. Current differential protection applies Kirchhoff's law and compares the current entering and leaving the protected zone. Important settings for differential protection are primary and secondary side voltages, minimum differential current (Id_{min}) beyond which the differential protection should operate, fault recording and oscillography. To accurately set the value of Id_{min} in the relay, fault analysis of the test case was conducted. Three phase to ground fault was applied at the primary side of the transformer at t = 2 sec. The results are shown in Fig. 2. Table I shows the settings of the RED-670 for differential protection which are based on the results from fault analysis (Fig. 2). Fig. 3 shows the screen shot of the application configuration interface of PCM600 showing blocks for measurements, fault recording, differential protection, tripping, LEDs and Digital I/O settings.

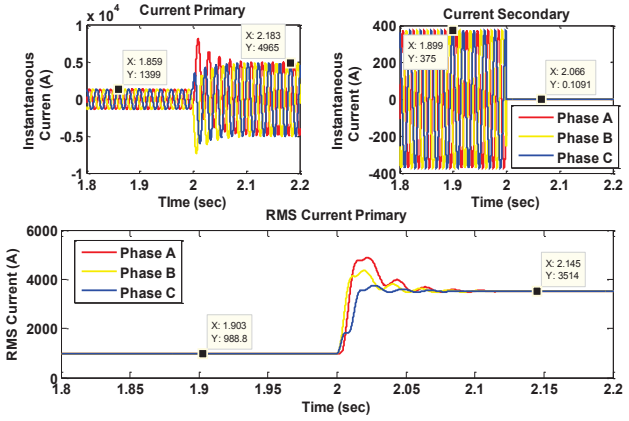

Fig. 2. Fault Analysis of Test Case

The digital output of the relay was configured to change its status from normal open to normal close as soon as the relays trips for differential protection. The digital output of ABB RED-670 was coupled with digital input of the simulator which was used to open the circuit breaker in the SPS model which was being executed in RT. Further calculations were performed to find the overall tripping time of the relay for RT HIL testing.

TABLE I
TEST SYSTEM ANALYSIS AND RELAY SETTINGS

Measurements	Full Load Current	1500 A
	Maximum Fault Current (Three Phase Fault)	7120 A
Relay Setting	Primary Voltage	11 kV
	Secondary Voltage	40 kV
	No. of Terminals	2
	Curve Type	IEC Definite Time
	Id_{min}	2000 A
	Pre-Fault Record	100 msec
	Post Fault Record	500 msec

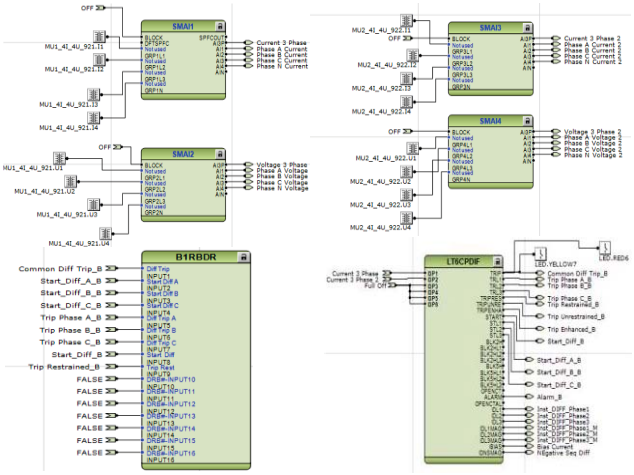

Fig. 3. Application Configuration Interface of PCM 600

III. TEST CASE SCENARIOS

Scenario 1: Complete Traditional Topology

In case 1, both the primary and secondary currents of the transformer windings were fed to the CT inputs of ABB RED-670 using copper wires. Some specific blocks from the RTS vendor Opal-RT were added to the SPS model to access the analog outputs and digital inputs of the RTS. These blocks are available in the RT-Lab library [4]. The modified SPS model for case 1 is shown in Fig. 4.

In order to amplify the low level current outputs from real-time simulator, amplifiers from Megger [6] are used. The analog outputs of the simulator are fed to SMRT-1 amplifiers which amplify the currents to a steady state value of 1 A (as the CT input of the relay are designed for 1 A input). These amplified current signals were fed to the CT inputs of ABB RED-670. As soon as the three phase to ground fault is applied in the test case (executing in real-time), the relay detects the fault and trips, thus changing its digital output contact from normal open to normal close. This change in status is detected by the digital input of the RTS which opens the breaker in the SPS model in real-time. The

overall workflow from building the model to simulating it in real-time and executing HIL validation is shown in Fig. 5. The results of RT-HIL validation are shown in Fig. 6 which shows a tripping time of 29.6 msec. This time is the difference between fault application time and the breaker opening time i.e. it also includes the time for the digital I/O of relay to change its status.

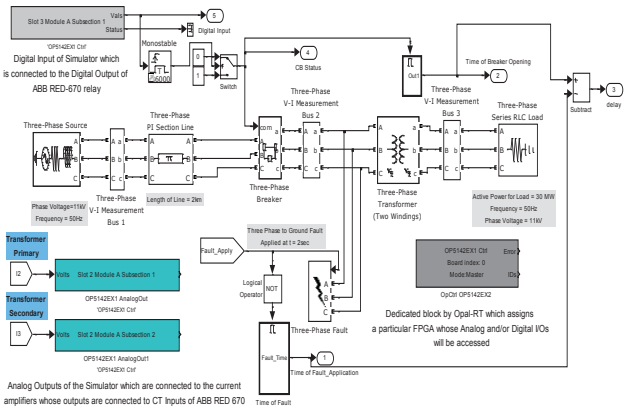

Fig. 4. Test case model with modifications for RT-HIL simulation

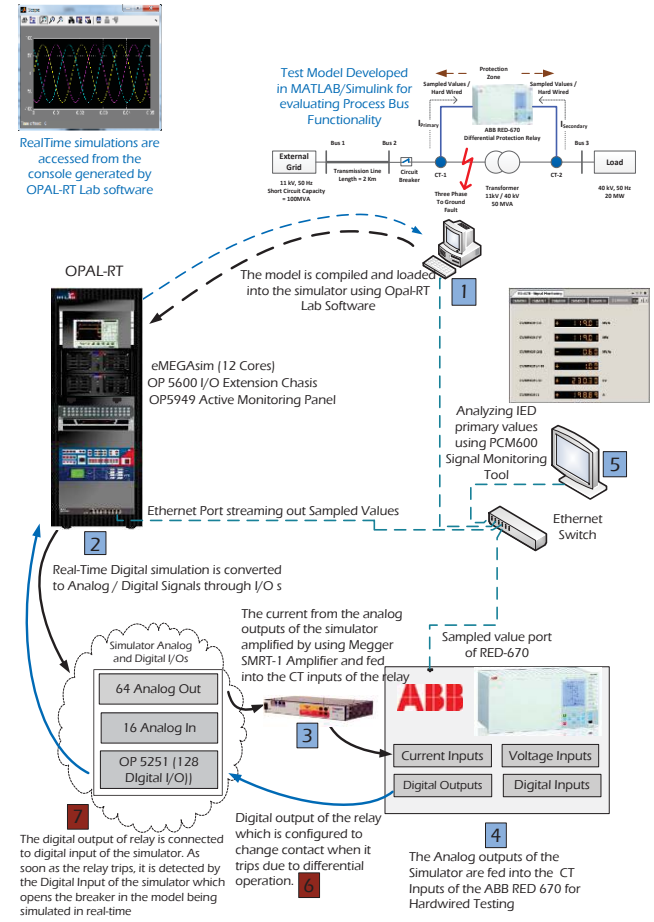

Fig. 5. Model-to-Data Workflow for HIL simulation. Solid lines indicate hardwired connections, dashed lines indicate digital data streams over Ethernet.

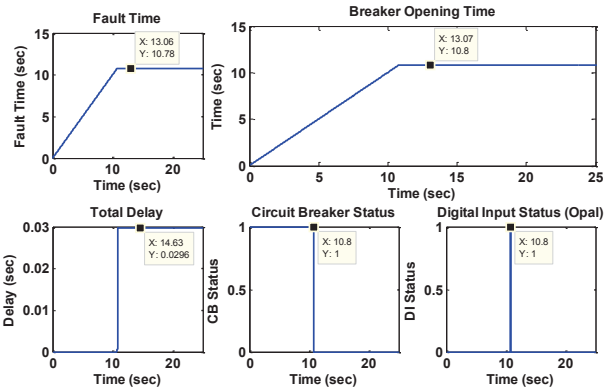

Fig. 6. Results for RT-HIL validation for differential protection when both primary side and secondary side currents are fed with copper wires.

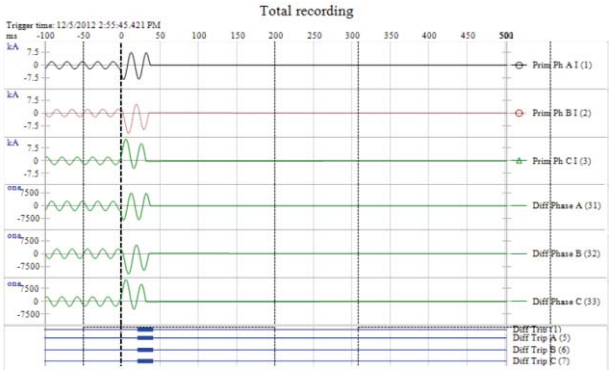

Fig. 7. Results from the RED 670 Even Report for differential protection when both primary side and secondary side currents are fed with copper wires.

The RT-HIL results are validated by comparing them with the event report of RED-670. Fig. 7 shows that as soon as the fault is applied, the transformer primary current increases to about 3500 A (RMS) and causes the relay to trip under differential protection.

Scenario 2: Hybrid Process Bus Topology

In case 2, the current values for the primary side of the transformer are fed to RED-670 using sampled values (SV) while the secondary currents of the transformer windings are fed to the CT inputs of ABB RED-670 using hardwired. Opal-RT's RTS has the ability to simulate a merging unit which streams out 4 Voltages and 4 Current measurements in IEC 61850-9-2 format. A similar approach as described in the previous scenario was adopted to perform the test except that the hardwire feeding analog current signals from simulator to the primary CT input of RED-670 were removed (as these measurements were now sent as SV over Ethernet). The results for RT-HIL are shown in Fig. 8 which shows the tripping time of 29.51 msec. The event report for this scenario is similar to Fig. 7 showing transformer primary current rising to 3500 A (RMS) when the fault is applied and secondary current dropping to almost 0 A.

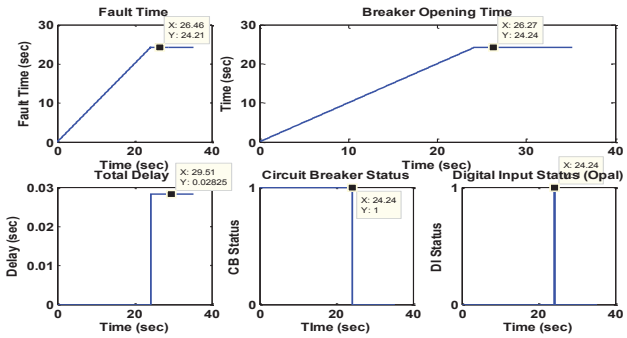

Fig. 8. Results for RT-HIL validation for differential protection when primary side is SV and secondary side currents are fed with copper wires.

Scenario 3: Complete Process Bus Topology

In case 3, the current values for both the primary and secondary side of the transformer are fed to RED-670 using sampled values. In this case two merging units were simulated in the model and the primary and secondary currents of transformers (i.e. currents at Bus 2 and Bus 3) were fed to these merging units. The modified model of test case is shown in Fig. 9. The two blocks named as ABB_MU_1 and ABB_MU_2 represent the merging units. The results of this test case scenario is shown in Fig. 10 which shows tripping time of 28.99 msec. Fig. 11 shows the pre-fault and post-fault differential current values as computed by RED-670.

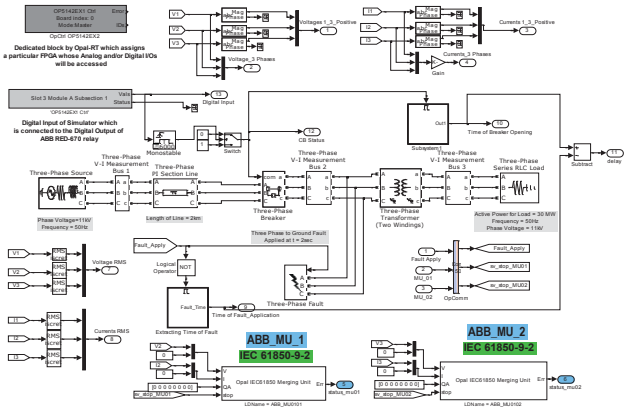

Fig. 9. Test case model with modifications for RT-HIL simulation for complete process bus implementation.

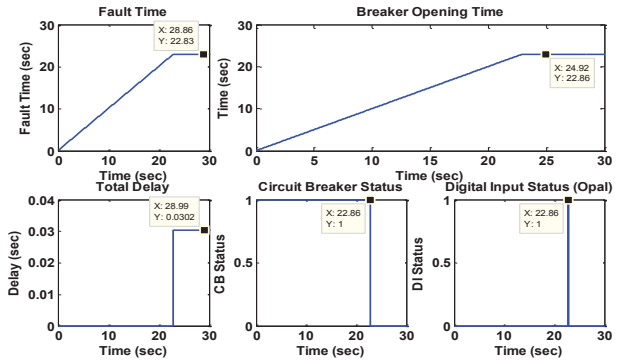

Fig. 10. Results for RT-HIL validation for differential protection when both primary and secondary side currents are fed as Sampled Values.

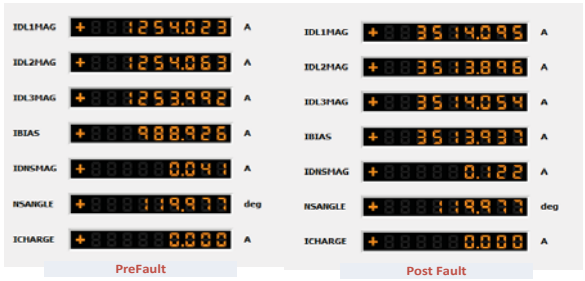

Fig. 11. Pre-fault and Post-fault currents as computed by ABB RED-670

TABLE II
COMPARISON OF THE RESULTS FROM THREE DIFFERENT TEST SCENARIOS

Comparison of Results (Fault Applied at t = 2 sec)	
Topology	***Tripping Time***
Both Primary and Secondary Hardwired	29.60 msec
Primary SV and Secondary Hardwired	29.51 msec
Both Primary and Secondary SV	28.99 msec

IV. CONCLUSION

By utilizing Opal-RT's eMEGAsim real-time simulator, Hardware-in-the-Loop testing of process bus performance for differential protection is presented for three different scenarios. The results are shown in Table II. For all the three scenarios, the tripping time is very similar which means that traditional hardwired implementation of differential protection for a two winding transformer can be replaced with process bus implementation. This paper does not show the effect of traffic jam, network congestion, data packet loss in Ethernet on the tripping times. This will be reported in a future publication.

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