Real-Time Implementation of an Automatic Voltage Stabilizer for HVDC Control

Kim Weyrich [*] **Walter Kuehn** [*] **Rujiroj Leelaruji** [**] **Luigi Vanfretti** [**]

[*] *Frankfurt University of Applied Sciences, Frankfurt, Germany*
[**] *KTH Royal Institute of Technology, Stockholm, Sweden*

Abstract: Classic HVDC systems are prone to voltage instability when operating on weak AC grids. Certain methods are available to cope with weak system conditions, one of which is VDCOL. This paper describes the implementation of a newly developed Automatic Voltage Stabilizer (AVS) in an existing CIGRÉ Benchmark Model for HVDC Controls and compares its performance with the VDCOL method. The tools used for the study are the OPAL-RT real-time simulator and the PSCAD/EMTDC digital simulator. With AVS, the power transfer can be optimized and kept at or close to the steady state stability limit thereby compensating for deficiencies of VDCOL. Using two different simulation environments provides important information on their capabilities to develop and improve future power system controls.

Keywords: Classic HVDC, VDCOL, Automatic Voltage Stabilizer, Real-Time Simulation

1. INTRODUCTION

1.1 Voltage Collapse in Classic HVDC Systems

Classic HVDC systems are prone to steady state voltage instability when at least one of the AC grids that converters are connected to is weak or the grid becomes weak through certain causes, e.g. switching off AC lines or reactive power supply limitations. In order to avoid voltage instability and power loss, certain operational measures are currently taken. Two important ones are event triggered power order reduction and voltage dependent current order limitation (VDCOL).

The first measure works reliably if the trigger signal is available for all probable events. This can only be ensured in a radial system while a meshed grid will be too complex to incorporate all forthcoming grid changes. With regards to the second measure which reduces the DC current order in response to decreasing AC or DC voltage, the problem lies in the difficulty to choose a suitable characteristic to reduce the DC current at a varying short circuit power ratio. An AC grid with a normally high ratio requires a different characteristic when the ratio goes down. However, there is no automatic adaptation, voltage instabilities may occur.

These challenges can be solved by applying the Automatic Voltage Stabilizer (AVS) Kuehn [2010a]. The AVS is based on an on-line steady state stability analysis using a dynamic stability limit detection method Kuehn [2010b]. The PV-characteristic in Fig. 1 provides information about a generic AC transmission system with regards to the voltage instability.

The uncontrolled AC voltage (V_{AC}) is at the receiving end of an AC transmission system. The voltage declines with increasing power up to the maximum transferable power (MTP) level, once the MTP-Point has been reached, it will decline with decreasing power. In general, this PV-curve holds also for an HVDC system being connected to an AC grid of moderate stiffness Kuehn [2009].
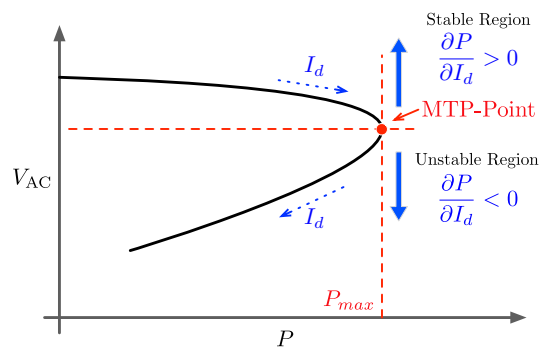

Fig. 1. PV-Curve and stability limit detection method

On the upper branch, DC current rises in proportion to the ordered DC power. If the MTP-Point is surpassed, the DC current continues to grow but the DC power declines. The conventional HVDC power controller is not able to detect this change, and the AC terminal voltage starts to collapse. The collapse can be halted through voltage VDCOL. VDCOL does, however, not recognize if the system has already passed the stability border and that it is operating on the lower branch of the PV-curve. Besides voltage depression this mode of operation has some other even more detrimental disadvantages as it became clear through theoretical analysis and preliminary PSCAD/EMTDC simulations using an own HVDC model. The results are summarized under Section 1.2.

1.2 Possible VDCOL Problems

Asynchronous machines, thermostatic loads and distribution transformers — With decreasing AC voltage, the operating point on the torque-slip characteristic of an asynchronous machine might move toward the critical slip value. It consequently increases the machine current which leads to voltage collapse and machine stalling because the VDCOL function is not able to limit the DC current increase on the upper branch of the PV-curve. A similar problem exists in connection with thermostatic loads and

distribution transformers controlling consumer voltage via on-load tap changers.

Synchronous Generators — If VDCOL does not stop the HVDC system from moving towards the lower PV-curve branch, electromechanical instability may arise. In this work two different basic scenarios were simulated. In the first scenario we assumed that at the sending end of an AC transmission system, a synchronous generator provides power for an HVDC system located at the receiving end of the AC transmission system. In the second scenario, we assumed that synchronous generators are located at both ends of the AC transmission system.

Particularly in parallel AC/DC transmission systems the interaction between AC and DC is very crucial Bunch and Kosterev [2000]. In Hammad [1999] the necessity to study steady characteristics to understand transient phenomena of parallel systems and to find remedial measures is stressed. Such studies were also conducted for the Blackwater Back-to-Back-Tie when for the first time the voltage sensitivity factor was applied to determine steady stability limits and a corresponding control concept Hammad and Kühn [1986].

Today's transient HVDC performance and control calibration needs are directly determined on a transient simulator without preceding static stability investigations Muthusamy [2010]. For strong AC grids this should not be a problem. However this approach is insufficient for weak grids, as described later in this paper.

Calibration — Calibrating VDCOL for a relatively strong system will not suffice when the system becomes weak in a non-anticipated way. Calibrating for a weak system and operating on a strong one will lead to unnecessary power curtailment.

Controls —The gain of the controlled converter station is negative on the lower branch of the PV-curve. Electromechanical swings are excited and power modulation, e.g. in Pacific HVDC Intertie, may act in the wrong direction.

The Automatic Voltage Stabilizer (AVS) Kuehn [2010a,b], which is described in Section II-B, does not experience the problems mentioned above. This is shown through various investigations, starting with building the model in Section II and model validation and comparative simulation results in Section III. Comparison refers to VDCOL versus AVS performance on the one hand, and PSCAD versus OPAL-RT simulations on the other hand.

1.3 Benefits of Real-Time Simulation

The PSCAD digital simulator permits the set-up and simulation of truly complex power systems including power semiconductor equipment and necessary controls. The simulation time increases in proportion to configuration size and the specific equipment needed. While for the comparison study in this article PSCAD is sufficient, additional real world circuitry would probably increase computation time to unacceptable values.

Further studies that consider the enhancement of the AC network model and the study of multi-terminal HVDC systems are planned. Thus, it is of value to simulate the AVS with a real-time simulator (OPAL-RT simulator)
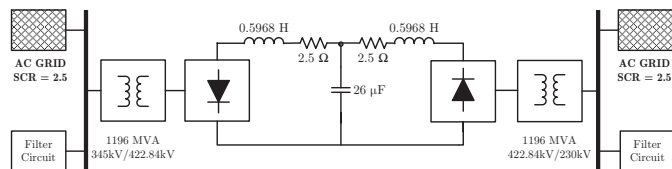

Fig. 2. CIGRÉ Model

already now and to get acquainted with real-time features before considering more complex configurations of multi-terminal HVDC systems.

Both the PSCAD digital simulator and the OPAL-RT simulator contain an implementation of the CIGRÉ Benchmark Model for HVDC Controls, including the VDCOL function. The main task of this work is the implementation and verification of AVS for both simulators.

2. MODELLING NEEDS

2.1 CIGRÉ Benchmark

The CIGRÉ Benchmark Model for HVDC Controls was constructed in April 1991 to provide a benchmark for control and HVDC studies (see Fig. 2). This benchmark model was used as a tool to test and optimize HVDC control systems for connecting weak AC grids. It contains a 12 pulse, 500kV, 1000MW mono-polar transmission system. It uses the marginal current control principle, where under normal conditions, the rectifier controls the DC current and the inverter the DC voltage. When the rectifier grid voltage becomes too low to control the DC current, this task is taken over by the inverter.

The model implemented by OPAL-RT has the same architecture as the original CIGRÉ Benchmark Model. In contrast to the original model it is enhanced with specific features regarding control and protection issues. Through this the the OPAL-RT model permits the connection of actual control and protection circuitry supplied in external control cubicles. However, as can be seen later, the difference with respect to the original model is actually not relevant for comparative statements regarding VDCOL vs AVS.

2.2 AVS Implementation in PSCAD

The PV-curve provides analytical means to distinguish between the upper and the lower branch by determining the derivatives of the DC power with respect to the DC current (see Fig. 1). Essential for a statement on steady state stability is the sign of the quotient $\partial P/\partial Id$.

Since $\partial P/\partial Id$ cannot be measured directly, it is determined by measuring the derivatives $\partial P/\partial t$ and $\partial I/\partial t$ with respect to time, and forming the product of these derivatives resulting in: $\partial P/\partial t \times \partial I/\partial t = $ crit (see Fig. 3(a)). If only one of the derivatives with respect to time becomes negative, which indeed occurs when moving along the lower branch of the PV-curve, the product "crit" becomes negative. If both derivatives with respect to time are either positive or negative - which happens when the operating point moves along the upper branch - the product is positive, so we know that the operating point is on the upper branch.

The value of "crit" is passed to a hysteresis buffer that triggers a mono-flop which in turn sets the stability limit detection signal "slds". Figure 3(b) illustrates how the
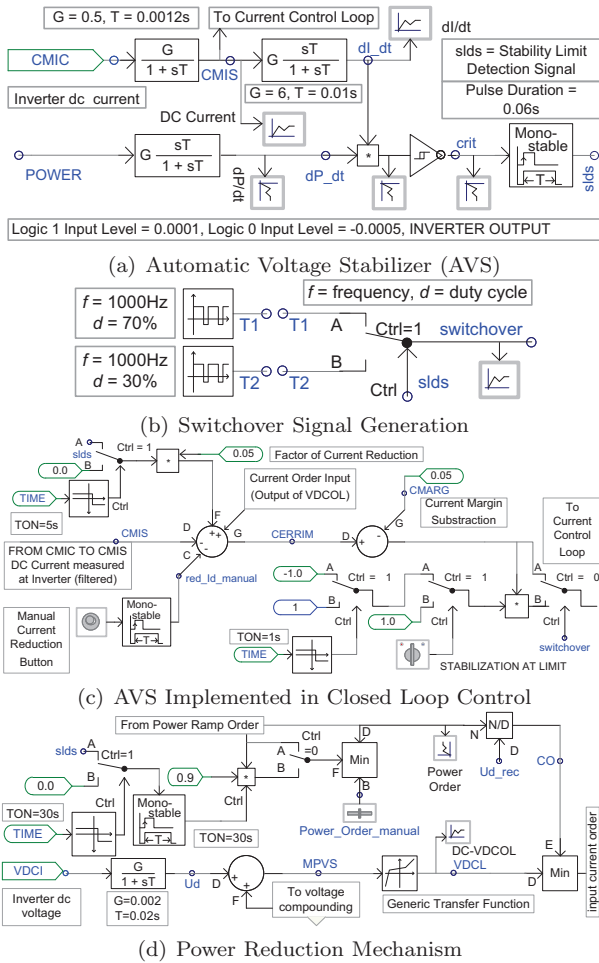
(a) Automatic Voltage Stabilizer (AVS)

(b) Switchover Signal Generation

(c) AVS Implemented in Closed Loop Control

(d) Power Reduction Mechanism

Fig. 3. PSCAD/EMTDC AVS Implementation

"slds" generates a pulsed signal called "switchover" which operates finally the sign reversal switch.

Two clock signals, T1 and T2, are embedded in the circuit. With T1 the operating point is pushed back up, with T2 it falls back to the lower branch. The displayed principle ensures a safe oscillation around the MTP-Point.

Figure 3(c) depicts the effect of the switchover signal. The two time-based switches can be disregarded. They are necessary to power up the system to nominal conditions without AVS control.

If the AVS is switched on ("Stabilization at Limit" in upper position), the feedback sign of the closed-loop current controller is switched between plus and minus depending on the switchover signal. A negative sign will change the current from increase to decrease. This leads the operating point back to the upper branch and then, since the "crit" value becomes positive, the sign is switched back to positive. In this way the operating point will revolve around the stability boundary.

Instead of bounding the operating point around the stability border, the power order can automatically be reduced at the first occurrence of the stability limit detection signal (slds) (see Fig. 3(d)). This signal triggers a mono-flop that in turn operates a switch which reduces the power order by a defined value. In Kuehn [2010a] this is a value adapting itself to the MTP level, but this value is fixed for the test purpose in this paper.

Figure 3(d) shows that VDCOL is DC based. This is indeed a limitation due to the fact that the AC voltage declines always earlier than the DC voltage.

However, for a weak AC grid with an SCR of around two there is only a very small AC voltage decline before the voltage collapses. That is, the difference whether using AC VDCOL or DC VDCOL is only marginal and not decisive for the functioning and the performance of VDCOL at weak grid conditions.

2.3 Real-Time AVS Model Implementation

The AVS was implemented within the inverter control subsystem of the original model. Fig. 4(a) depicts the details of the AVS which was embedded. The measured DC current (CDC) and DC voltage (VDC) are multiplied
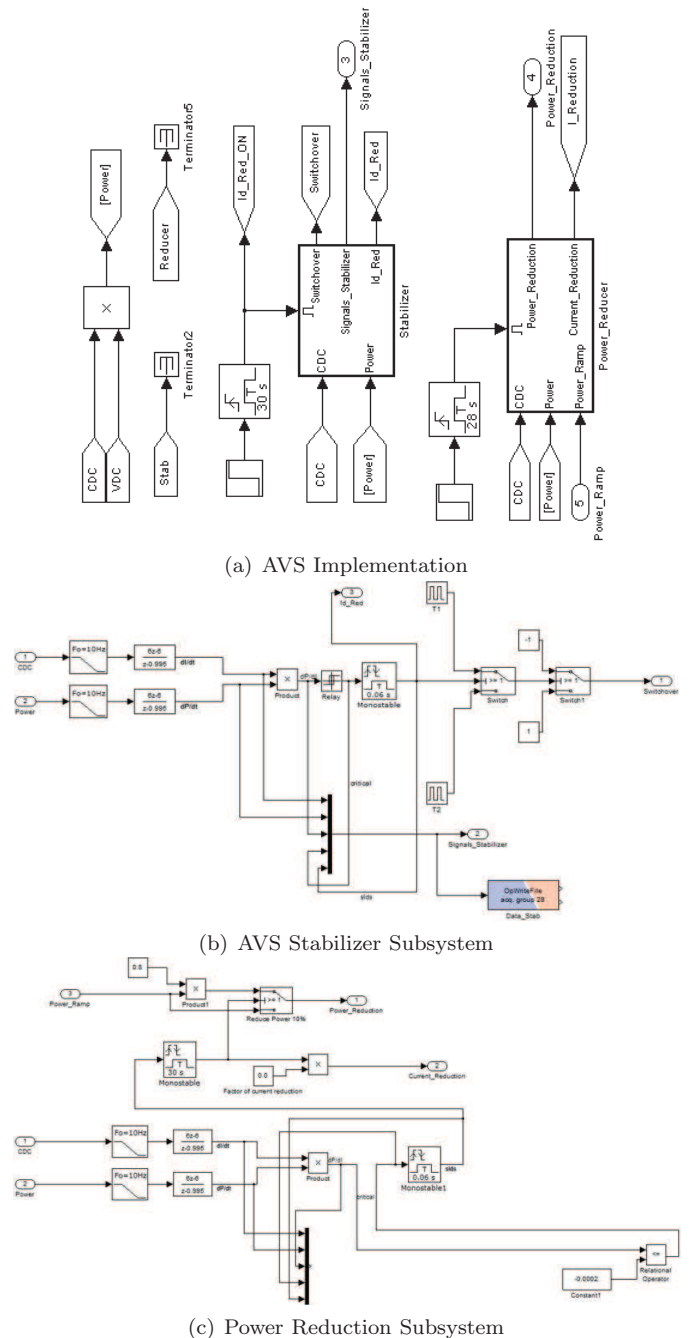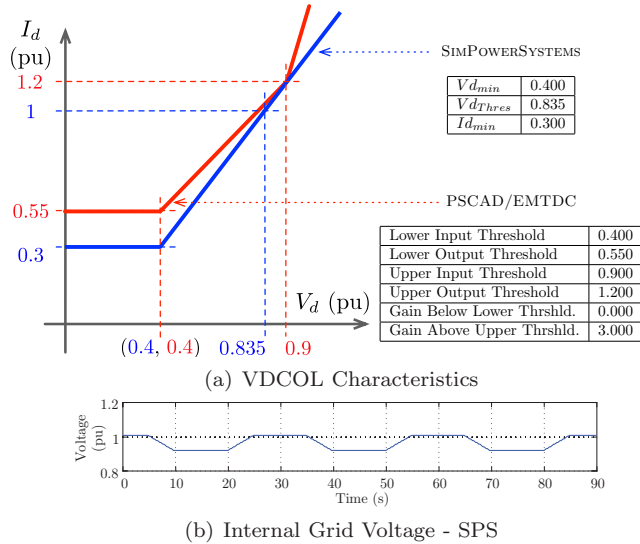

(a) AVS Implementation

(b) AVS Stabilizer Subsystem

(c) Power Reduction Subsystem

Fig. 4. AVS Implementation for Real-Time Simulation

(a) VDCOL Characteristics

SimPowerSystems	
Vd_{min}	0.400
Vd_{Thres}	0.835
Id_{min}	0.300

PSCAD/EMTDC	
Lower Input Threshold	0.400
Lower Output Threshold	0.550
Upper Input Threshold	0.900
Upper Output Threshold	1.200
Gain Below Lower Thrshld.	0.000
Gain Above Upper Thrshld.	3.000

(b) Internal Grid Voltage - SPS

Fig. 5. VDCOL Characteristics and Internal Grid Voltage Response

to get the power transmitted over the DC link. The subsystems for the stabilizer (Fig. 4(a) and 4(b)) and the automatic power reducer (Fig. 4(c)) are equipped with a switch to set them active or inactive.

The stabilizer is switched on after 35 sec. and stays active for 30 sec., while the automatic power reducer is switched on at 67 sec. and remains active for 28 sec. When the stabilizer is switched on, the "Id_Red_ON" function is set on too.

The OpWriteFile subsystem is a special real-time computation element, which is not part of the default SimPowerSystems (SPS) Toolbox. But it is used here to write the data of defined parts of the system into a file for further analysis. As for the PSCAD model automatic power reduction is implemented to avoid revolving around the MTP-Point.

3. COMPARATIVE SIMULATIONS

3.1 VDCOL Characteristics

Weak grid here means that the internal reactance of the grid is set to a value resulting in a short circuit power ratio (SCR) of 1.9 at an internal AC grid voltage of 380 kV. It is assumed that this SCR value results from a structural change with a SCR value of 3.33 before this change. For the calibration of the VDCOL characteristic the normally existing SCR value of 3.33 was taken to show the effect of inappropriate calibration.

The characteristic permits DC current overload of 1.2 at 0.9 p.u. AC voltage. This is either a temporary overload or can even be continuous overload depending on the prevailing ambient temperature. This is a realistic assumption: consider the Blackwater HVDC Back-to-Back-Tie with continuous control of the 60-kV-filter bus voltage and discrete control of the 345 kV terminal voltage via the on-load tap changer of the converter transformer. If the characteristic would be changed, such that the upper input threshold is 0.95, the results herein are still in an acceptable range.

The parameters given in Fig. 5(a) show that the VDCOL calibration differs considerably between PSCAD and SPS.

(a) AC Terminal Voltage
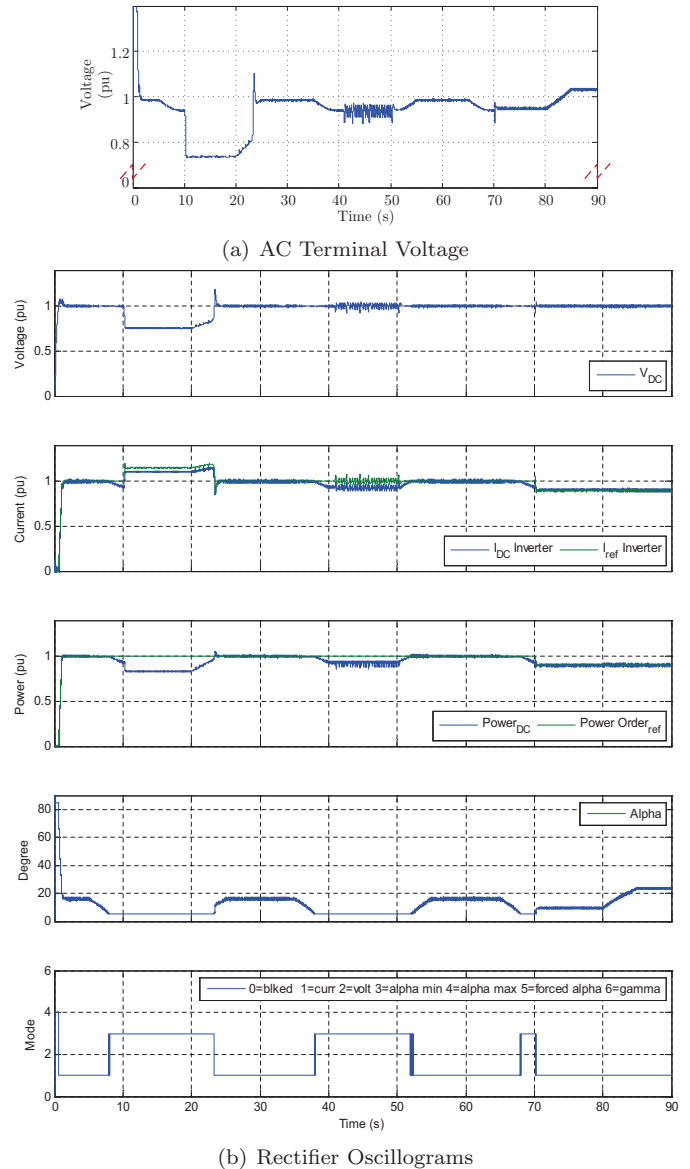

(b) Rectifier Oscillograms

Fig. 6. Weak AC Grid on Rectifier Side - SPS Results

However, the characteristics are similar as depicted also in Fig. 5(a).

Figure 5(b) shows a controlled variation of the internal grid voltage to test the behavior of VDCOL, AVS and the AVS with automatic power reduction in the listed order. In PSCAD simulation the variation of the internal grid voltage can be accomplished manually or via an automatic ramp. Manual ramping is not possible with SPS due to time lags between the monitoring console and the real-time target, automatic ramping is used.

3.2 Weak AC Grid on Rectifier Side

In this scenario the SCR at the Rectifier is 1.9 while the SCR at the Inverter is 2.5. Figure 6(a) shows the response of the AC terminal voltage of the rectifier as a result of a variation of the internal grid voltage as shown in Fig. 5(b). Only the VDCOL is activated during time 10-20 sec., which makes voltage drop to 0.75 p.u. The AVS is activated between time 40-50 sec., which retains voltage level above 0.9 p.u. The AVS with automatic power reduction is activated at time 70-80 sec. Figure 6(b)
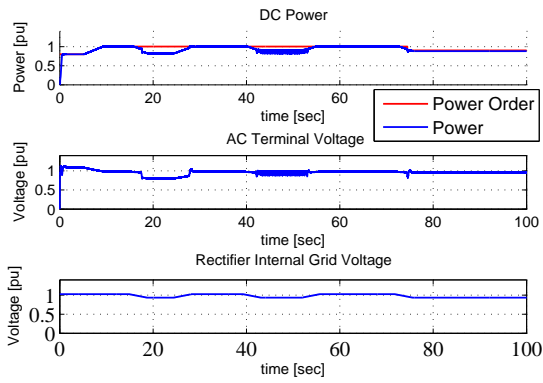
(a) DC Power and Rectifier AC Voltage
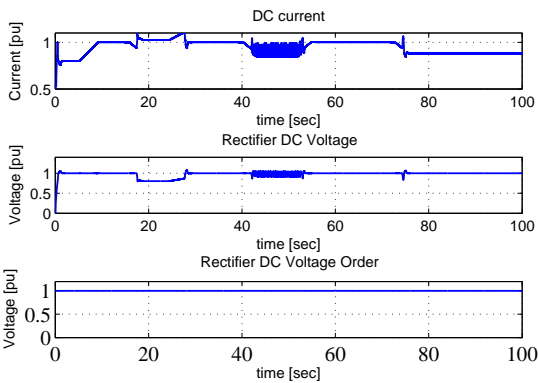
(b) DC Quantities

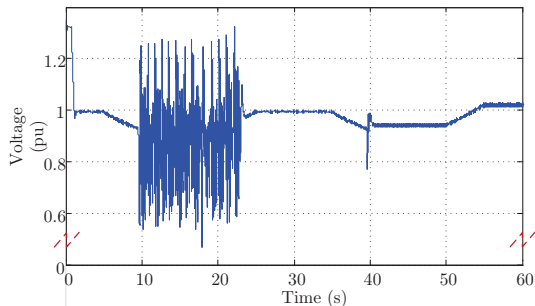Fig. 7. Weak AC Grid on Rectifier Side - PSCAD Results

Fig. 8. AC Terminal Voltage Inverter - SPS

illustrates the comparison of the DC quantities for the three different control methods.

The magnitudes of the DC voltage and the DC current provide an indication of the location of the operating point on the PV-curve. It is clear that without AVS, the operating point at VDCOL operation slides to the lower branch of the PV-curve. The operation of AVS without the power order reduction yields stable swings around stability limit and this swing can be removed by applying the automatic power order reduction.
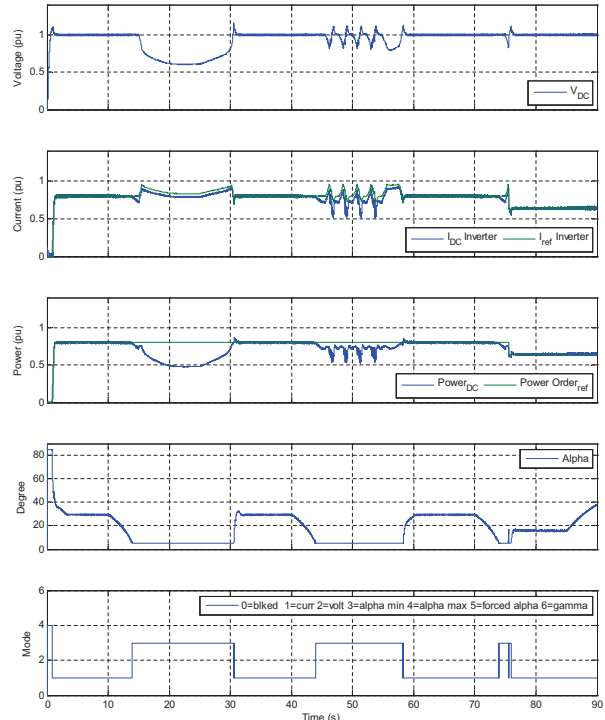
Figure 7(a) and 7(b) depict the similar test on PSCAD digital simulator. As seen from Fig. 6(b) to 7(b), we can conclude that the AVS implementation on both simulators provide similar responses.

3.3 Week AC Grid on Inverter Side

The internal grid voltage shown in Fig. 5(b) is applied at the inverter. In this scenario only VDCOL and AVS
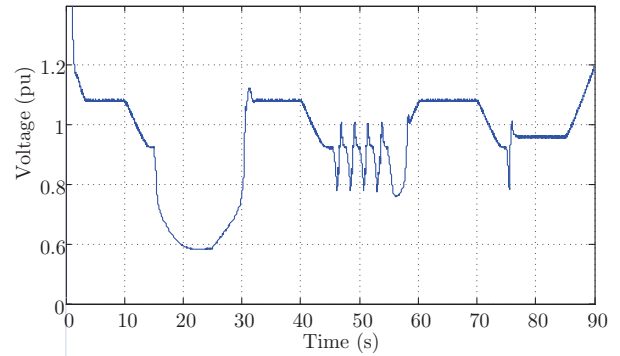

(a) AC Terminal Voltage at the Rectifier

(b) Rectifier Oscillograms

Fig. 9. Performance with Asynchronous Machine - SPS

with the automatic power reduction are tested. Only the VDCOL is activated during time 10-20 sec., the commutation failure occurs as shown in Fig. 8. In contrast to VDCOL, the operation of AVS, at time 40-50s, results to only a voltage dip and prevent the commutation failure. Similar simulation results from the PSCAD simulation were obtained.
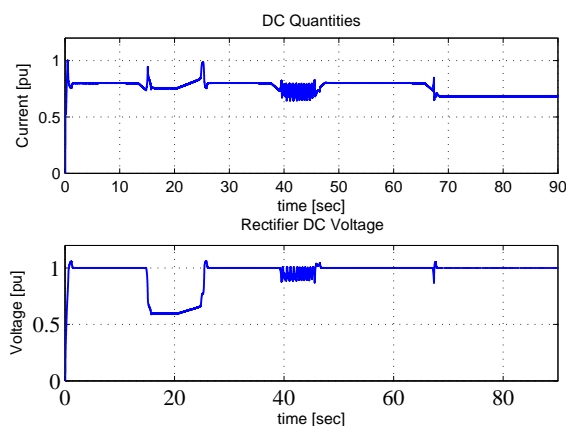
3.4 Performance with embedded Asynchronous Machine

In this scenario the SCR at the rectifier is set to 1.9 while the SCR at the inverter is set to 3.3. In contrast to the previous scenarios, the DC power is decreased to 0.8 p.u (taking into account the demand of an asynchronous machine). The total power transfer on the AC line before the test is approximately same level as previous scenarios. The AC terminal voltage of the rectifier shows a steep decline with solely VDCOL in operation ($t = 10$-30 sec.), dropping to 0.6 p.u. (see Fig. 9(a)). This low voltage level caused by the reactive power demand of the asynchronous machine pulling down the AC voltage.

Figure 9(b) shows that DC power decreases despite the DC current increase, this is a clear indication that the MTP-
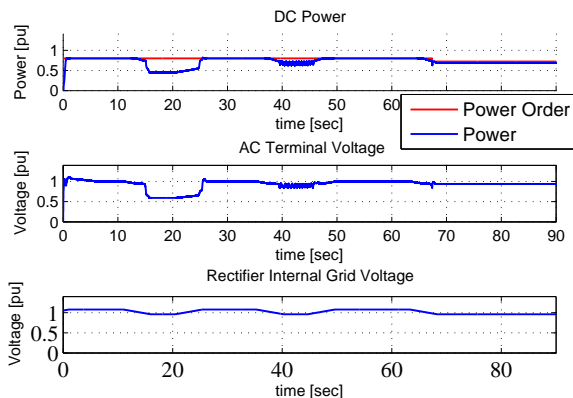
(a) DC Power and Rectifier AC Voltage

(b) DC Quantities

Fig. 10. Performance with Asynchronous Machine - PSCAD

Point is surpassed. As the previous test, the AVS and the AVS with the automatic power reduction are applied at time 40-60 sec. and 70-90 sec., respectively, where both of them prevent system collapse.

Figure 10(a) to 10(b) illustrate the similar response obtained from the PSCAD digital simulator. Fig. 11 shows the response of the asynchronous machine. VDCOL cannot stop the AC grid voltage decline. The asynchronous machine is sent over the pull-out slip causing further voltage decrease. AVS prevents this phenomenon either by keeping the operating point revolving around the maximum power point or by applying automatic power order reduction.

4. CONCLUSIONS AND FURTHER WORK

HVDC systems operating in weak environments can be stabilized by application of a dynamic stability limit detector, and an ensuing proper utilization of a stability limit detection signal generated by the detector. This stabilization works also when asynchronous machines are connected to the converter bus at the weak system.

The given system size could be handled with the PSCAD digital simulator without excessive simulation time requirements. The real-time simulator using SimPowerSystems (SPS) produces the same results as the PSCAD digital simulator although various non-relevant features had to be changed in the case of the real-time simulator.
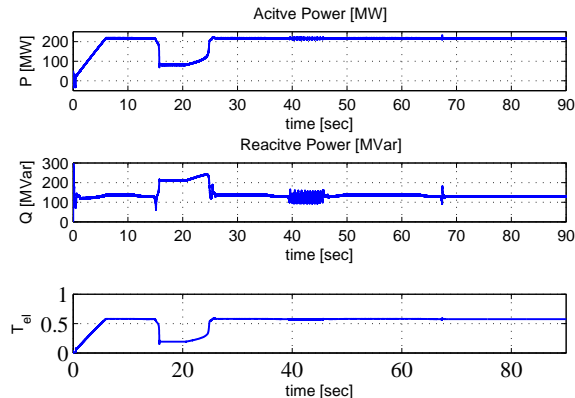

Fig. 11. PSCAD Oscillograms Asynchronous Machine

The way to obtain the results is considerably different with both the simulators. However, this is not the place to evaluate the various features and properties of both the simulators, particularly not so without explicit consent of the simulator suppliers. We apologize for not providing more detailed information on advantages or drawbacks holding for the simulators.

Real systems contain distributed generation and also, particularly in the future, more HVDC systems which can be Classic or VSC-HVDC. The work presented here has laid the foundation for expanding the present system model and using the PSCAD digital simulator as well as a Real-Time Simulator. Preliminary studies not yet included here prove that the AVS works also when synchronous machines are connected to the weak AC grid, and also when the AC transmission system transports power between a remote synchronous generators and the HVDC system.

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