Development, calibration and simulation of generic VSC-HVDC high level controls for DC grid Simulation

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Master Thesis

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Abstract

Energy security concerns and the environmental impact of conventional power generation sources has led to an increase in renewable energy penetration worldwide. Power transmission from remote generation sites to consumers over long distance is most efficient using high voltage direct transmission lines. Therefore, long distance power transmission and the integration of power generated by renewable energy resources are considered as key aspects in the development of sustainable energy systems capable of secure and stable electric power supply.

Voltage source converter based high voltage direct current (VSC-HVDC) long distance power transmission lines are needed to incorporate renewable energy sources to the grid. The significance of the research work in this field is obvious, however, advances in the area are detracted because of the lack of available VSC-HVDC system models. The purpose of this thesis is to provide generic models of VSC-HVDC controls and meshed networks. This thesis studies VSC-HVDC control systems and improves high level controls for the VSC. A point to point and four terminal VSC-HVDC systems are modeled in MATLAB/Simulink. Both offline and real-time simulation models are developed. The controllers are tuned and then tested in the developed test systems with several test cases through offline simulations in MATLAB/Simulink. All the models are modified and transferred to Opal-RT's real time targets and simulations are carried out for several test cases. Improved controller simulation results along with results from the conventional controllers are contrasted.

Acknowledgment

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Contents

Notation

ABB   Asea Brown Boveri

VSC   Voltage Source Converter

HVDC   High Voltage Direct Current

LCC   Line Commuted Converter

RT-LAB   Real Time Laboratory

DC   Direct Current

AC   Alternating Current

PI   Proportional Integral

MMC   Modular Multilevel Converter

SM   Sub Module

AVM   Average Value Model

IGBT   Insulated Gate Bi-polar Transistor

PLL   Phase Locked Loop

RPC   Reactive Power Controller

AVC   Alternating Voltage Controller

DSC   Delayed Signal Cancellation

Chapter 1 : Introduction

1.1. Background

High voltage direct current (HVDC) lines were developed for long distance power transmission. The use of long distance power transmission with HVDC started in 1954 by ABB, to connect the island of Gotland and mainland Sweden [1].

Long distance power transmission through HVDC links above 500 km [11] is the most economical and efficient technology due to lower power losses and less conductors compared to AC transmission lines [2].

The electrical power generation share of renewable resources has increased rapidly all over the world. The World Energy Outlook 2012 report indicates that this contribution is up to 24% in Europe in 2010 [3]. To facilitate the integration of large amount of power generated from renewable energy to the conventional grid, HVDC plays an important role. It offers fast and flexible control of the power flow to the grid to secure grid reliability [4]. In addition, power generation from offshore wind farms requires long distance transmission lines to transport the generated power to consumption areas and therefore HVDC lines are a key technology for this purpose.

HVDC transmission systems can be composed by two types of converters; Line Commuted Converters (LCC) or Voltage Source Converters (VSC) [5]. Mercury or thyristor based classical HVDC systems have limitations to control power flow direction; this type of converter consumes reactive power in both the rectifier and inverter mode of operation [1] [5]. Consequently, for reactive power compensation, large ac filters are needed in the converter stations which increase the cost of the HVDC system. Moreover commutation failure and communication loss between LCC based converters are considered the main drawbacks of this technology [1] .Voltage source converter based HVDC technology offers the following advantages over LCC-HVDC systems [6- 5] :

- ➢ Independent control of active and reactive power.

- ➢ Reduction of power quality disturbances.

- ➢ Reactive power support to the ac systems.

- ➢ No communication between converters is required.

- ➢ Suitable for creating multi-terminal DC grids with large number of converters.

Additionally, to facilitate the DC grid concept in the present power transmission system, VSC-HVDC transmission technology is essential not only to integrate large amounts of renewable energy to the conventional grid but also allows to interface multiple AC systems with the HVDC grids. This would also allow to relocate the power flow between terminals in case of any DC terminal outage [7].

1.2. Problem definition

Numerous advantages of VSC-HVDC transmission technology can facilitate renewable energy integration to the grid [8].

The point to point VSC-HVDC scheme is well-known, it allows to exchange power between two terminals [7]. This makes VSC-HVDC technology attractive to develop Multi-terminal VSC-HVDC systems connect several DC terminals, which may improve the flexibility and reliability of the power system [9].

VSC-HVDC system consists of two control systems, a high level and a low level control. High level controllers are responsible to regulate dc voltage, active power, reactive power, ac voltage and the frequency of the system [10].

To develop multi-terminal VSC-HVDC technology it is necessary to study the behavior and interaction of VSC controls. However, the lack of detailed models and realistic data limits research and development in the area.

Hence the main aspects of VSC-HVDC technology treated in this thesis are the following:

- ➢ Development of generic control models and test systems of a point to point VSC-HVDC system.
- ➢ Improvements to high level controls.
- ➢ Development of a four terminal VSC-HVDC test system.
- ➢ Real time simulation of the developed point to point and four terminal VSC-HVDC models.

1.3. Objectives

The main objectives of this thesis are the following:

- ➢ To perform a literature review.
- ➢ To study and improve the high level controls of VSC-HVDC.
- ➢ To develop a point to point DC link test system.
- ➢ To develop a tuning methodology to calibrate high level control model parameters.
- ➢ To develop a four terminal DC grid test system.
- ➢ To perform offline simulation for all of the developed models in Simulink.
- ➢ To prepare the simulation models for real time simulation
- ➢ To perform real time simulation in RT-LAB for all of the developed models.

1.4.   Contributions

This thesis is a part of the "Smart Power" project Action 2.1.1., funded by KIC InnoEnergy Collocation Center Sweden, within the European Institute of Innovation and Technology (EIT), the aim of the project to provide generic control models and corresponding DC grid test systems. The research work has been carried out at "KTH SmarTS Lab".

The contributions of this thesis are the following

- ➢ Develop point to point and four point DC grid test models.
- ➢ Calibrate the high level controller parameters.
- ➢ Implement dc voltage damping controller and simulate with the test model to analyze the effect of the damping controller.
- ➢ Develop and implement a negative sequence current controller for the point to point DC grid model and observe the behavior.
- ➢ Develop and implement a dc voltage droop controller for the four point DC grid model and run several test cases to observe the significance of using this control system.
- ➢ Perform real time simulation for all developed models and carry out the performance analysis.

1.5.   Overview of the Report

This report is organized in to two parts:

1. Literature review.
2. VSC-HVDC controls enhancement, Implementation and Simulation.

The first part includes Chapter 2 and Chapter 3. In Chapter 2, the basic concepts about VSC-HVDC technology has been presented, moreover Chapter 3, contains the overall control system structure and implementation.

The second part consists of Chapter 4, Chapter 5 and Chapter 6. In Chapter 4, the improvement of the high level control system has been described, whereas Chapter 5 and Chapter 6 includes the offline and real time simulation of the VSC-HVDC test models.

The report concludes by outlining conclusion and proposing future works.

Chapter 2 : VSC-HVDC system, model and operation

2.1. Configuration of VSC-HVDC systems

The VSC-HVDC system is a new technology to transmit power over a DC line. Based on the connection between converters stations, there are four major configurations of VSC-HVDC systems [11].

Monopolar VSC-HVDC system

In this configuration one side of the converter is grounded and another side is connected with a single pole line. Based on the application, the ground or the metal conductor of one converter can be used as a return path [11]. Following figure represents two types of the monopolar VSC-HVDC system configuration.
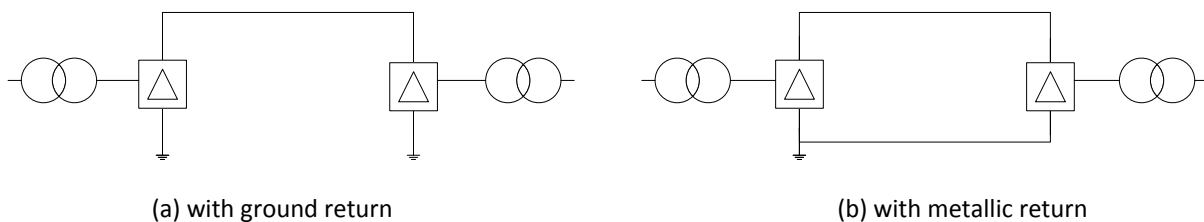

(a) with ground return   (b) with metallic return

Figure 2.1: Monopolar VSC-HVDC system.

Bipolar VSC-HVDC system

Bipolar configuration is the combination of two monopolar VSC-HVDCs. Here the common connection point of two sets of converters are grounded, therefore in case of the outage of one pole, another one still can transmit power. Hence two poles can independently transmit power [11].
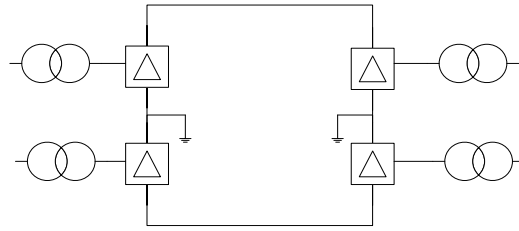
Figure 2.2: Bipolar VSC-HVDC system.

Back to back VSC-HVDC system

When two converter stations are located at a same place, and there is no need to connect the converters with the transmission line or cable; then this type of configuration is used [6]. The following figure shows a back to back configuration.

Figure 2.3: Back to back VSC-HVDC system.

This configuration is called as the point to point configuration, when the converters are located in different regions and need to be connected with a transmission line to transmit power form one converter side to another. In that case one converter acts as a rectifier, which provides the power flow and another one acts an inverter which receives that power. The point to point VSC-HVDC configuration is one of the mostly used dc link topologies so far [12].

Multi-terminal VSC-HVDC system

Three or more converter stations are connected together either in series or in parallel connection in this topology. Power flow can be directed towards or received by any converter station by defining the rectifier and inverter operation mode of the converter. Multi-terminal HVDC is other main type of the dc grid topologies, which can improve the flexibility and reliability of the HVDC system [9]. Multi-terminal VSC-HVDC configuration is shown in the following figure.
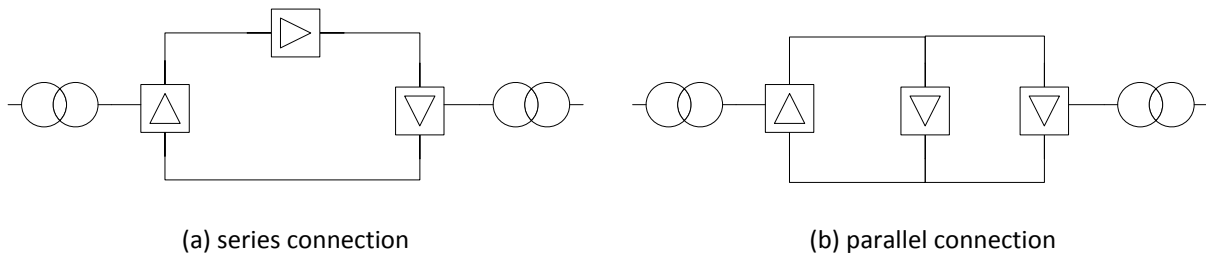
(a) series connection   (b) parallel connection

Figure 2.4: Multi-terminal VSC-HVDC system.

2.2. Elements of VSC-HVDC systems

Transformer

A transformer is used to provide the required voltage to the converter according to the converter capacity. In Figure 2.1, the VSC-HVDC system is connected with two ac sources with transformers on both sides.

AC filter

Higher order harmonics are generated from the switching device (IGBT), in the AC voltage. To suppress these harmonics, a high pass AC filter is installed in the system. Otherwise it will emit harmonics in to the AC system. In addition, this filter can act as a reactive power source.

Phase reactor

A phase reactor assists the control of active and reactive power of the system by controlling the current flowing through it. Besides, it compensates higher order harmonic of the current.

DC capacitor

There is a capacitor in the DC side of the converter. The main purpose of the capacitor is to store energy for the power flow control. Capacitor size mainly depends on the desired DC voltage of the system. This also helps to attenuate dc line voltage ripple.

Voltage source converter (VSC)

A two level three phase VSC with six pulse bridges is the simplest and mostly used configuration in HVDC technology [11]. This converter is known as voltage source converter because of the fixed dc voltage polarity as the dc link capacitance connected in parallel to the bridges keeps the dc voltage level constant [13]. Figure 2.5 depicts a two level three phase voltage source converter.
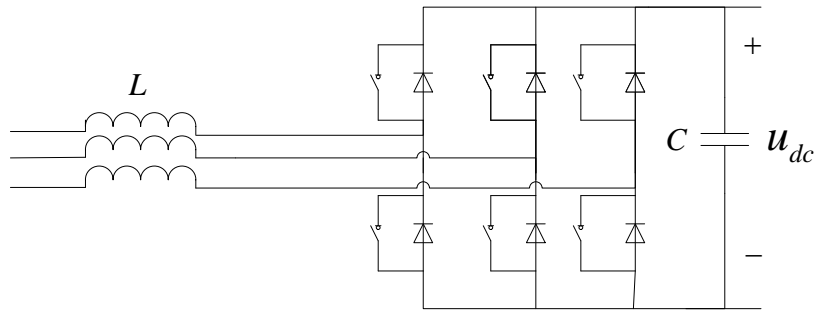
Figure 2.5: Two level three phase VSC converter [14]

The VSC can be operated both as a rectifier, i.e. ac voltage to dc voltage conversion, or an inverter, i.e. dc voltage to ac voltage conversion. By changing the direction of the current flow from source to converter or vice versa, it can switch the mode of operation. The generated voltage output in the ac side of the converter has two discrete voltage levels, i.e. positive and negative; therefore it is also recognized as two level converter. The VSC converter is connected to the ac side and dc side with an inductor (L) and a capacitor (C), which filter the harmonics to get smoother current and voltage wave forms.

Three phase three level and modular multilevel VSC converter are a modified converter strategy. In the three level converter each phase of the converter can switch to positive dc terminal voltage, negative dc terminal voltage and at zero, therefore the output voltage produced by the converter is closer to the reference voltage with less harmonic content [1].

The major concern about the conventional two level VSC converter with PWM technology is the high and steep voltage steps at the ac connected terminal [15]. Hence, a high level of electromagnetic interference is generated; as a result special filtering is required to remove this higher order harmonics [15]. The modular multilevel converter (MMC) topology has proposed significant improvements in the harmonic reduction and lowering of switching losses [1]. It consists of sub modules connected in series and the sub modules can be switched with lower frequencies which results low switching losses and a reduction in the steepness of the ac voltage. Hence the required filter size becomes much smaller. Individual switching of sub modules produces smooth and almost ideal sine waves in the output of the converter. The following figure shows a MMC topology.
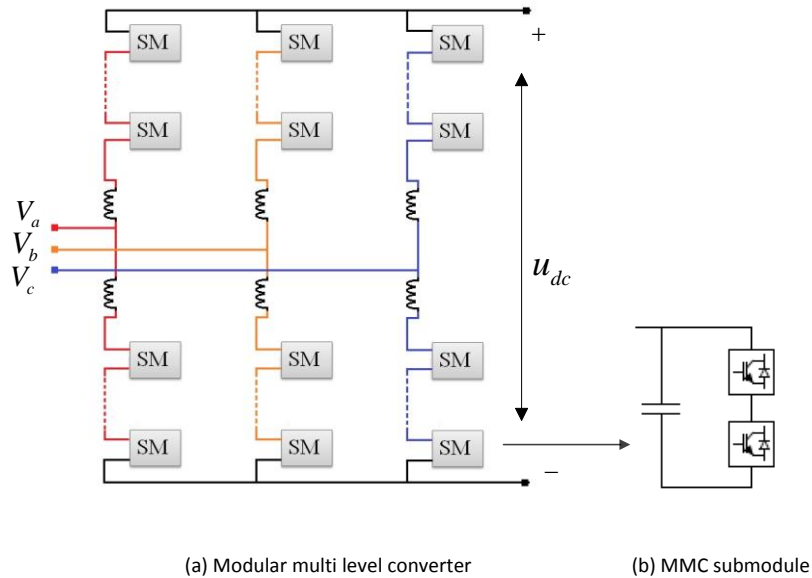
(a) Modular multi level converter   (b) MMC submodule

Figure 2.6: Modular multilevel VSC converter.

Each phase leg of the MMC consists of an upper and lower arm with sub-modules shown in Figure (b). Each sub-module has two valves which contain IGBTs and diodes connected across a capacitor. These valves can be switched in three different ways [10]

- When the upper valve of Figure 2.6 (b) turns off and the lower valve turns on, the sub-module is inserted and therefore the cell output voltage becomes same as the capacitor voltage. The capacitor charges when current flows from the capacitor side to the valve side and discharges if the direction is reversed.
- When the upper valve turns on and the lower valve turns off, then the capacitor is bypassed and the voltage of the capacitor remains constant.
- When both of the valves are turned off then the sub-module is blocked.

Therefore with a high number of sub-modules it can generate an output voltage wave form thus resembles to the desired voltage wave form [1].

2.3. VSC modeling

The VSC can be modeled both in detail and using an average value model (AVM). In the detailed model the IGBTs are used as switching components. Using the PWM technique, the gate pulses are given to the IGBT's to generate the desired wave form. Detail modeling is significant to analyze lower level controls of the VSC which include PWM and sub modules arm voltage control. However, in AVM, a controllable ac voltage source is connected to the ac circuit and a controllable current source is connected to the dc circuit [14]. The AC-side and DC-side representation of a VSC-AVM can be shown by using the following figures. The following AVM of a VSC has been implemented in the Simulink model which was used in this thesis,
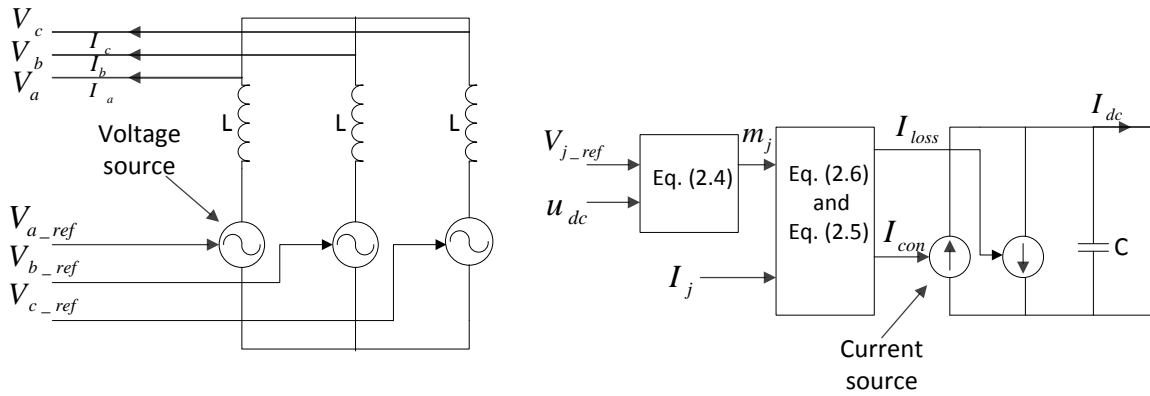

Figure 2.7: AC-side (left) and DC-side representation (right) of a VSC-AVM

The AC-side behavior of the VSC-AVM is described by

$$V_j = \frac{L}{2} \frac{dI_j}{dt} + V_{j\_ref} \qquad (2.1)$$

where, j characterizes each of the phase a, b, c ; V_j is three phase voltage; V_{j_ref} is the reference voltage generated from the inner current controller; L is inductor and I_j is three phase current.

The DC-side of the AVM is derived on the basis of both the ac and dc sides power conservation law,

$$P_{ac} = P_{dc} + P_{loss} \qquad (2.2)$$

$$\sum_{j=a,b,c} (V_{j\_ref} I_j) = u_{dc} I_{dc} + P_{loss} \qquad (2.3)$$

Modulation indexes (m_j) are responsible to control three phase reference voltage [14] are

$$m_j = \frac{2 V_{j\_ref}}{u_{dc}} \qquad (2.4)$$

$$I_{con} = \frac{1}{2} \sum_{j=a,b,c} m_j I_j \qquad (2.5)$$

and

$$I_{loss} = \frac{R\, I_{con}^2}{u_{dc}} \qquad (2.6)$$

Where R represents equivalent resistance of both switching and resistive losses of the converter.

The dc current provided by the converter can be derived by the following equation,

$$I_{dc} = I_{con} - I_{loss} \qquad (2.7)$$

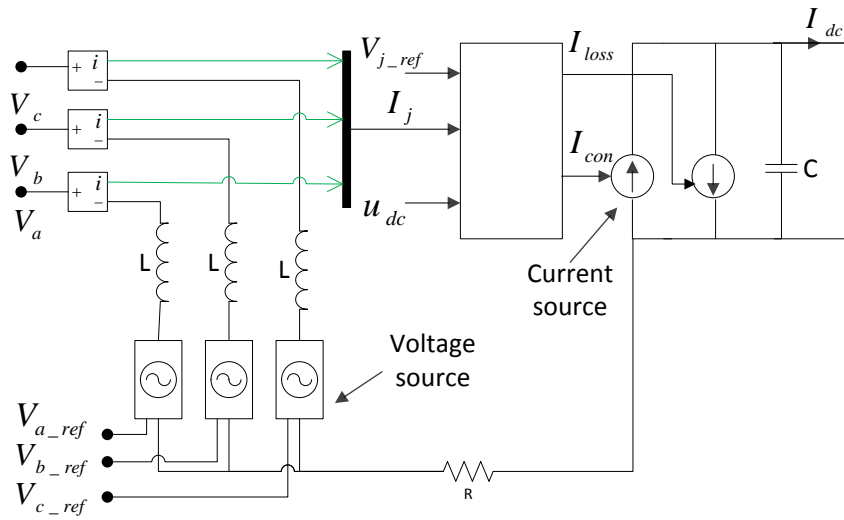The following figure shows the implementation of the average value model of the VSC [23].

Figure 2.8: AVM of a VSC

VSC-AVM works on the basis of conservation of power. Total power consumed by the three controllable voltage sources i.e. V_a, V_b, V_c equals to the injected power by the controllable current source I_{dc} in to the dc link.

2.4. Operating principle of VSC-HVDC systems

The voltage source converter with the switching device Insulated gate bipolar transistor (IGBT) can convert voltage either from ac/dc or dc/ac. Hence, the bidirectional power flow shown in Figure 2.9 is possible through the transmission line. Pulse width modulation (PWM) is widely used in IGBTs to generate the desired voltage wave form. It is also responsible for changing the phase angle and magnitude of the voltage waveform, so that the VSC acts in the system as a controllable voltage source which can independently control the active and reactive power of the system [6].

The operation of VSC-HVDC can be described by the following point to point VSC-HVDC system connected in between two ac sources with a dc line,
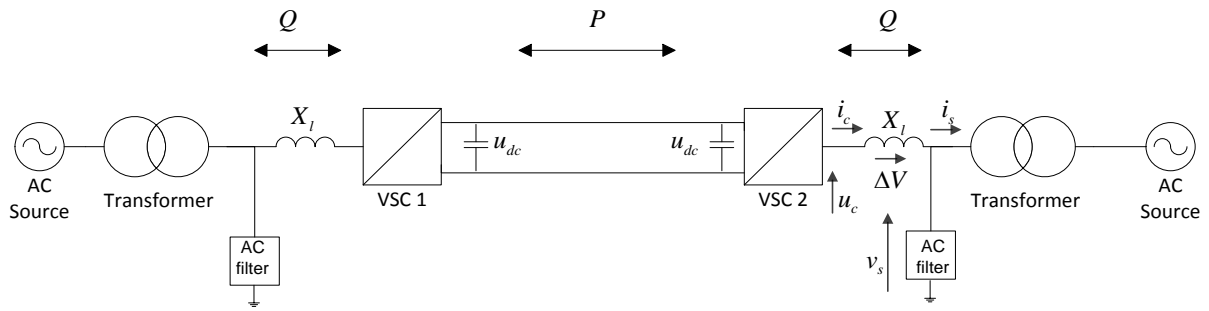

Figure 2.9: Point to point VSC-HVDC system.

In Figure 2.9 the converter voltage u_c is represented by [6]

$$u_c = \frac{u_{dc}}{2} m \, \sin(\omega t + \theta) + \text{harmonics} \tag{2.4}$$

The phase angle (θ) between the converter and the filter side voltage u_c and v_s respectively. The modulation index (m) are two variables, which can be set by the VSC controller to generate the desired voltage level. Hence the active and reactive power flows can be controlled by regulating the voltage drop ΔV over the phase reactor X_l.

Power transfer direction between the converter and source side is determined by the following two equations

$$P = \frac{u_c v_s \sin\theta}{X_l} \tag{2.5}$$

$$Q = \frac{u_c(u_c - v_s \cos\theta)}{X_l} \tag{2.6}$$

From equation (2.5), to control the active power flow direction, the phase angle θ has to be changed accordingly [6]. Reactive power flow direction can be controlled by the amplitude of the converter voltage u_c [6] and it is calculated from (2.6).

Chapter 3 : VSC-HVDC Control System

3.1. Introduction

The main purpose of controlling a VSC is to maintain the power balance between both sides of the converter, i.e. the dc link side and ac source side along with independent power flow control [16].

The control system of VSC-HVDC is classified into two levels, high level and low level controls. High level control system use a dq reference frame where d components of the current are responsible to operate dc voltage, active power and q components to operate ac voltage, reactive power. The control system hierarchy is depicted in the following figure.
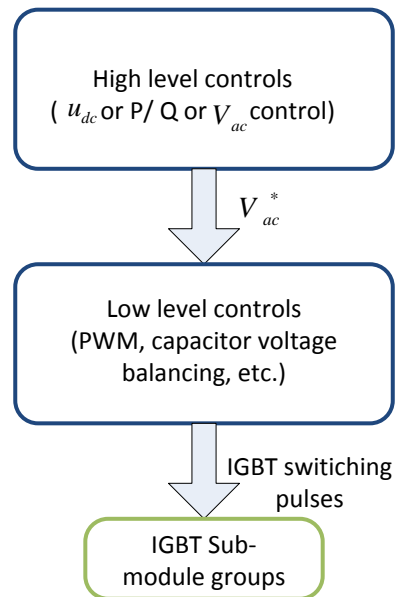

Figure 3.1: Hierarchy of the VSC-HVDC control system.

The voltage reference V_{ac}^* are fed to the low level control system which is generated from the high level control system, to perform PWM, capacitor voltage balancing tasks. At the end of the control system level, switching pulses for IGBT valves are generated as an output of the low level control system.

In this thesis, only the high level control system is the main concern of study, therefore low level control system is ignored.

In VSC-HVDC system the most investigated control methods are direct power control and vector control [17]. Besides a new control strategy for VSC-HVDC has been proposed in [17], which is named as power-synchronization control.

Direct power control system

Control strategy of direct power control is based on the active and reactive power equations (2.5) and (2.6) where the active power flow can be controlled by changing the phase angle θ and the reactive power flow is controlled by the converter voltage magnitude u_c. The following figure represents overall direct power control system.
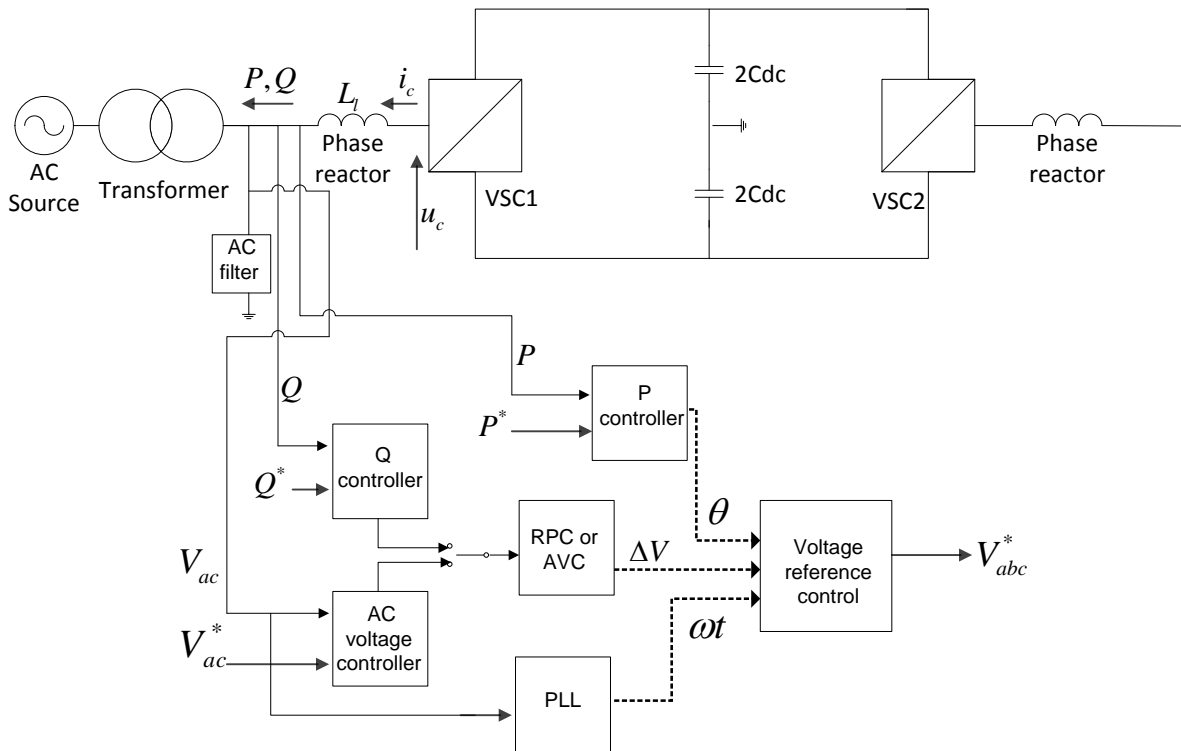

Figure 3.2: Direct power control diagram.

The VSC needs three variables to produce three phase ac voltage, i.e. voltage magnitude, phase angle and frequency [17]. In direct power control these variables are provided by the reactive power controller (RPC) or the ac voltage controller (AVC), active power controller and phase locked loop (PLL).

The active power controller takes the measured active power (P) from the grid side and controls it with a reference active power (P^*) using a PI controller. RPC and AVC controllers follow the same methodology where the PI controller is used to reduce the error between two input signals. The phase locked loop is used to synchronize the VSC to the ac system by comparing and reducing the error between the angular frequencies of ac system and VSC. All

of the controller's equations can be written in general form as $A = \left(K_p + \frac{K_i}{s} \right)(B^* - C)$. Where A represents $\Delta V, \theta$ and ωt ; B^* represents P^*, Q^* and V_{ac}^* ; C represents P, Q and V_{ac}.

With the controlled variables $\Delta V, \theta$ and ωt the voltage reference control block forms three phase reference voltage for the pulse width modulator.

The major drawback of this controlling system is the absence of an inner current controller, so that during a fault condition or other disturbances in the network over-current flows could damage the IGBTs of VSC. Furthermore, HVDC systems with this control method experiences this problem because of the variable switching frequency and slow response of the conversion [16].

Vector control system

The principle behind vector control, is ac voltages and currents occur as constant vectors in steady state and therefore an error that between the measured and reference vectors system can be removed from the signal by the PI controllers [16].Vector control consists of an inner and an outer control loop. This combination allows to control the real and reactive power independently through the fast inner current control loop [1] by separating the system currents in to *dq* components. The *d* components are used to control the active power or direct voltage and *q* components are used to control reactive power or ac voltage. The inner controller controls the converter current to a desired value. This current value is provided by the outer controller and generates three phase ac voltage references to feed to a controlled voltage source. The outer controller controls active power, reactive power, dc voltage and ac voltage of the system. All the measured three phase voltages and currents from the grid side are taken to control the power and voltage in the outer controller. Vector control schematic is shown in Figure 3.3.
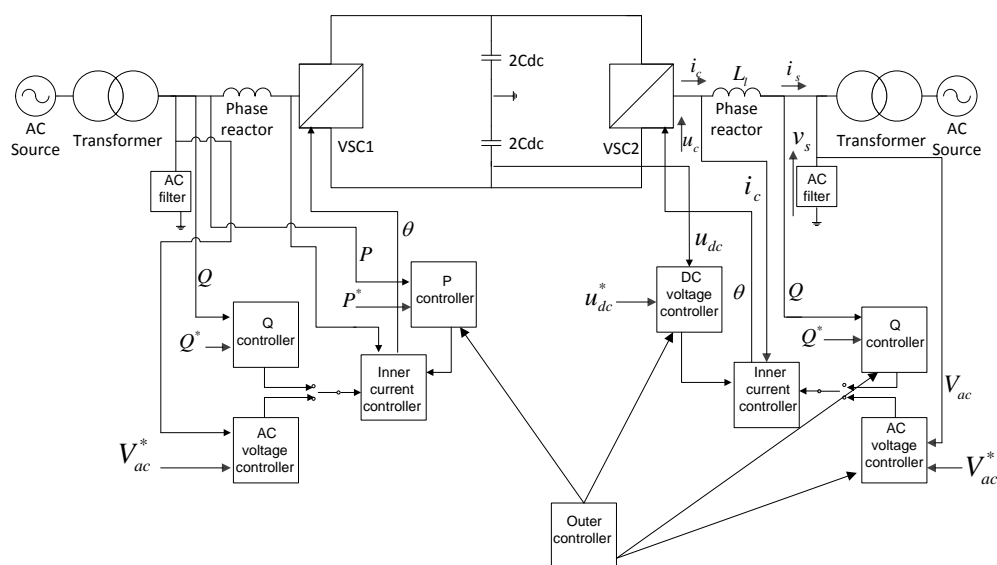

Figure 3.3: Vector control diagram of VSC-HVDC.

3.2. Inner current controller

In Figure 3.3, VSC2 side of the VSC-HVDC can be represented by

$$v_s = L_l \frac{di_s}{dt} + u_c \tag{3.1}$$

where, v_s and u_c are the filter side and converter side voltages, i_s is the current flowing towards ac side, i_c is the converter side current flowing through the inductive phase reactor L_l.

Converted to the s-domain (3.1) is

$$v_s = sL_l i_s + u_c \tag{3.2}$$

where, s represents Laplace operator of $\frac{d}{dt}$

Taking the dq transformation of (3.2), the dq components of the voltage

$$v_{sd} = sL_l i_{sd} + u_{cd} - \omega L_l i_{sq} \tag{3.3}$$

$$v_{sq} = sL_l i_{sq} + u_{cq} + \omega L_l i_{sd} \tag{3.4}$$

Cross coupling components $\omega L_l i_{sq}$, $\omega L_l i_{sd}$ in (3.3) and (3.4) are generated after the abc to dq transformation. Hence dq current components presented in the cross coupling term affects independent current control by the inner controller. With the intention (shown in Fig. 3.4) of removing cross coupling, the following decoupling scheme has been implemented
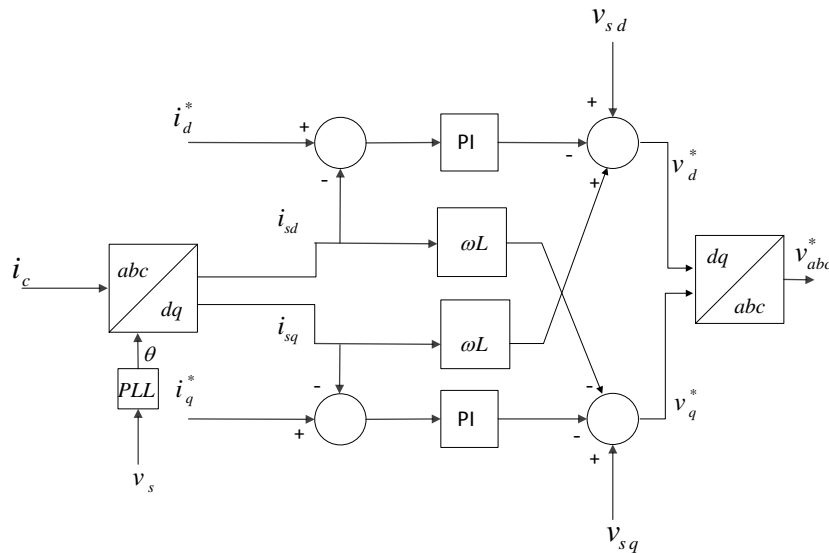

Figure 3.4 (a): Single line diagram of the inner current controller with decoupling.
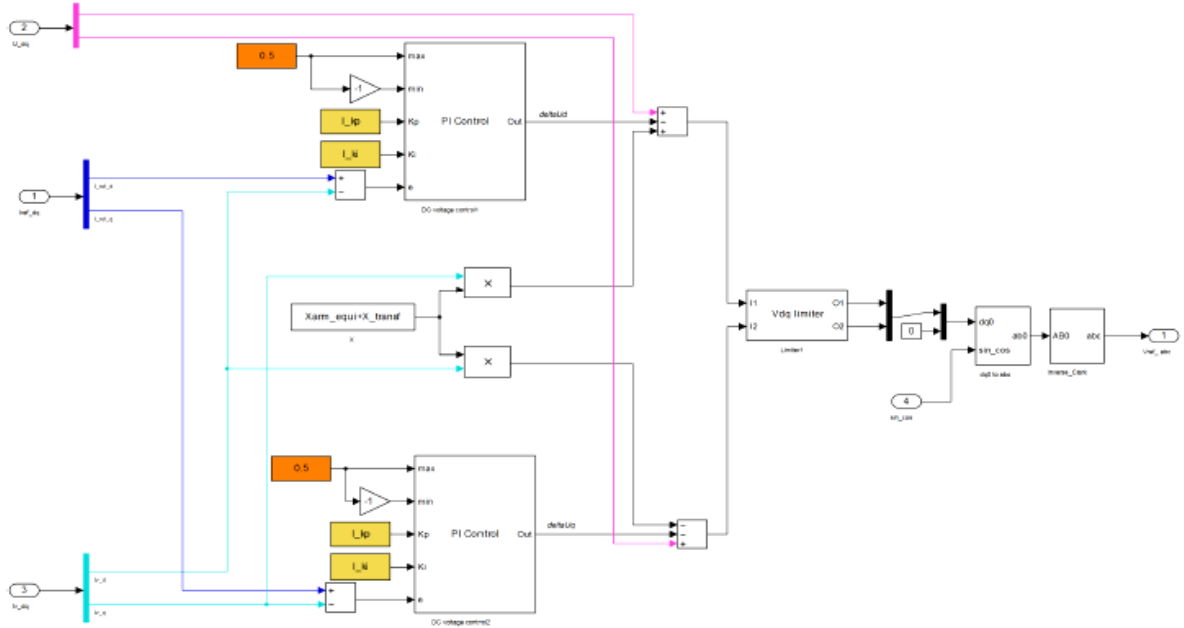
Figure 3.4 (b): Implementation of the inner current controller.

Output reference voltages form the inner controller leads to

$$v_d^* = v_{sd} + \omega L_l i_{sq} - \left(K_p + \frac{K_i}{s}\right)(i_d^* - i_{sd}) \tag{3.5}$$

$$v_q^* = v_{sq} - \omega L_l i_{sd} - \left(K_p + \frac{K_i}{s}\right)(i_q^* - i_{sq}) \tag{3.6}$$

where, K_p, K_i are the proportional and integral gain of PI controller, ω is the angular frequency, v_d^*, v_q^*, i_d^* and i_q^* are the dq components of voltage and current reference. Converter side three phase current i_c measured from the grid are transformed to dq components which are provided as input to the inner current controller.

In order to synchronize the converter with the grid, phase angle (θ) detection of the grid voltage is required. Phase locked loop (PLL) which uses phase tracking algorithm is used to make the synchronization, it can provide output signal synchronized with its reference input signal with the same phase angle and frequency [11]. It is implemented in dq synchronous reference frame, hence Park transformation is desired [11]. PLL provides synchronized phase angle with the gird to all of the controllers for the Park transformation [11]. From Figure 3.3 it can be seen that PLL synchronizes converter output current components i_{sd}, i_{sq} with the grid voltage v_s by providing phase angle (θ) to obtain the unity power factor [11].

3.3. Outer controller

Outer controller Responsible for controlling

> ➤ DC voltage (V_{dc}) (i_d^* is obtained)

> ➤ Active power (P) (i_d^* is obtained)

> ➤ Reactive power (Q) (i_q^* is obtained)

> ➤ AC voltage (V_{ac}) (i_q^* is obtained)
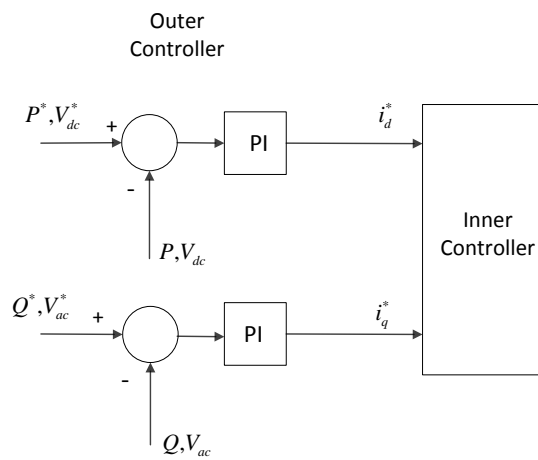

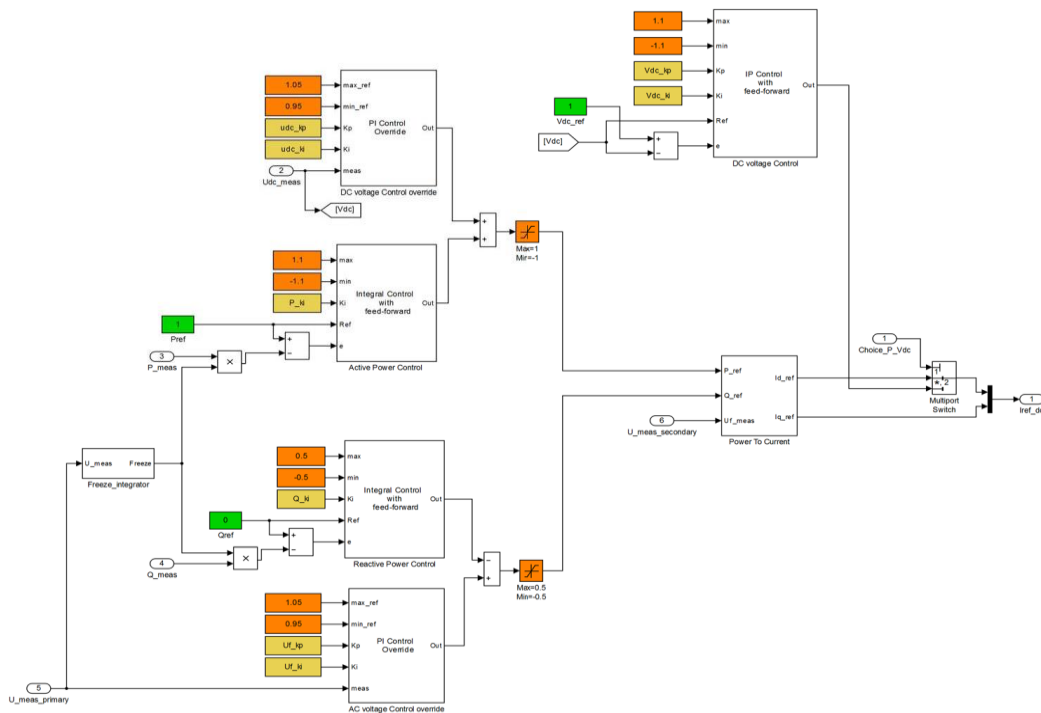**Figure 3.5 (a):** Outer controller block diagram.

Figure 3.5 (b): Implementation of the outer controller
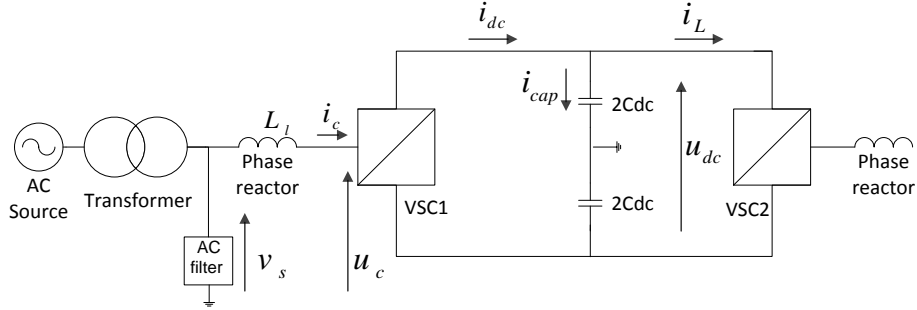
3.3.1. DC voltage control

Figure 3.6: Point to point VSC-HVDC system.

From Figure 3.6, dc link current i_{dc} flow from VSC1 side is divided in to capacitor current i_{cap} and VSC2 side current i_L

$$i_{dc} = i_{cap} + i_L \tag{3.7}$$

Therefore,

$$C_{dc}\frac{du_{dc}}{dt} = i_{dc} - i_L \tag{3.8}$$

Since in VSC-HVDC system, ac and dc side power should be balanced, so

$$P_{ac} = P_{dc} \tag{3.9}$$

After taking the Park transformation of the ac side voltage and current measurements, (3.9) will be

$$v_d\, i_d + v_q i_q = u_{dc}i_{dc} \tag{3.10}$$

The d axis of dq reference frame is aligned to the ac filter voltage v_s, therefore

$$v_q = 0 \tag{3.11}$$

with $v_q = 0$, (3.10) becomes

$$i_{dc} = \frac{v_d}{u_{dc}}i_d \tag{3.12}$$

From equation (3.8)

$$C_{dc}\frac{du_{dc}}{dt} = \frac{v_d}{u_{dc}}i_d - i_L \tag{3.13}$$

Here, u_{dc} is dc link capacitor voltage, v_d is d component of ac filter voltage and C_{dc} is dc capacitor.

Substituting Laplace operator s into (3.13)

$$u_{dc} = \frac{1}{s\,C_{dc}}\left(\frac{v_d}{u_{dc}}i_d - i_L\right) \tag{3.14}$$

Equation (3.14) shows that u_{dc} can be controlled by regulating i_d^*, since i_d is changed according to the set value of i_d^* using *PI* controller. Removing i_L as a disturbance signal mentioned in [18] from (3.14), then

$$u_{dc} = \frac{1}{s\,C_{dc}}\frac{v_d}{u_{dc}}i_d \tag{3.15}$$

Current controller loop response is assumed instantaneous with the outer controller [18], therefore

$$i_{dq} = i_{dq}^* \tag{3.16}$$

So from (3.12)

$$i_{dc} = \frac{v_d}{u_{dc}}i_d^* \tag{3.17}$$

During balanced condition in the system $i_{dc} = i_L$ and then (3.17) can be written as

$$i_d^* = \frac{u_{dc}}{v_d}i_L \tag{3.18}$$

The i_d^* of (3.18) is added to the dc voltage controller as a feed-forward term in case load is as added in the VSC2 side instead of a voltage source. This term facilitates load variation compensation in the system [18].
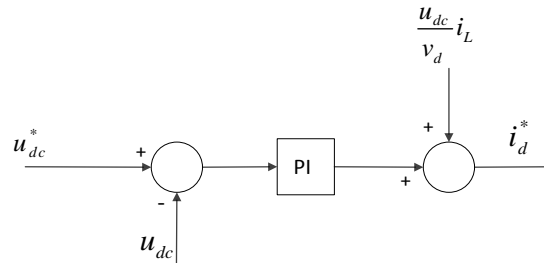

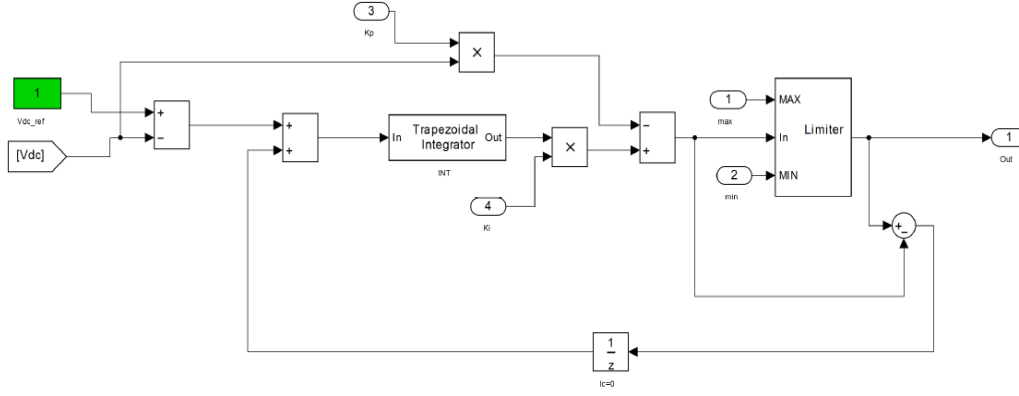**Figure 3.7 (a):** DC voltage control block.

Figure 3.7 (b): Implementation of the DC voltage controller.

Active current component reference equation according to the dc voltage control block can be written as,

$$i_d^* = \frac{u_{dc}}{v_d} i_L + \left(K_p + \frac{K_i}{s}\right)(u_{dc}^* - u_{dc}) \tag{3.19}$$

3.3.2. Active power and reactive power control

Instantaneous active power and reactive power in *dq* frame can be written as

$$P_{ac} = v_d\, i_d + v_q i_q \tag{3.20}$$

$$Q_{ac} = v_q\, i_d - v_d i_q \tag{3.21}$$

Substituting equation (3.11) and (3.16) into (3.20) and (3.21), we will get

$$P_{ac} = v_d\, i_d^* \tag{3.22}$$

and

$$Q_{ac} = -v_d i_q^* \tag{3.23}$$

Thus from (3.22) and (3.23), it can be seen that if v_d remains constant in the system then active and reactive power can be controlled with the simple open loop controller in the form of [18]

$$i_d^* = \frac{P^*}{v_d} \text{ and } i_q^* = -\frac{Q^*}{v_d} \tag{3.24}$$

where, P^* and Q^* represents reference active and reactive power.

With the feedback loop more precise control can be obtained [18]. Following figures depict active and reactive power controller with the combined open loop and feedback loop scheme,
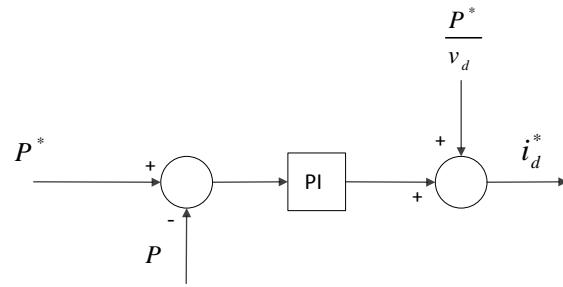
30

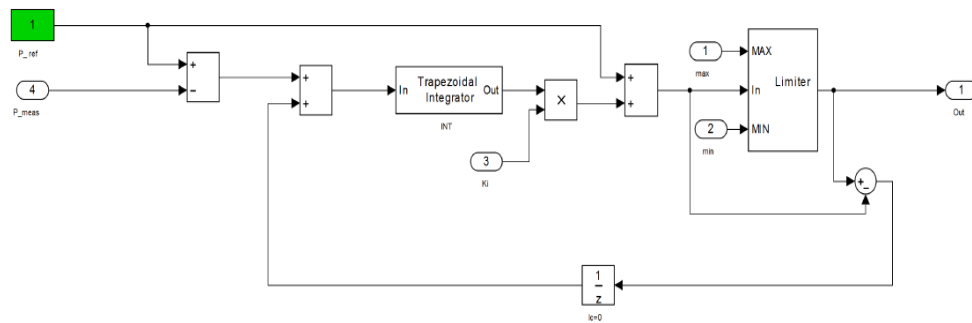**Figure 3.8 (a):** Active power controller block.

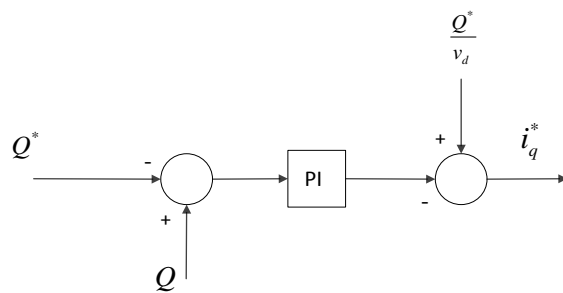**Figure 3.8 (b):** Implementation of the active power controller.

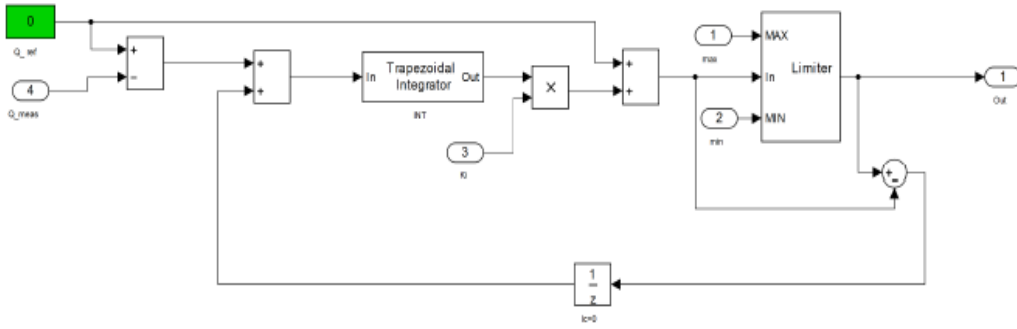**Figure 3.9 (a):** Reactive power controller block.

Figure 3.9 (b): Implementation of the reactive power controller.

Active and reactive current components i_d^*, i_q^* are delivered as an output from the active and reactive power controller as

$$i_d^* = \frac{P^*}{v_d} + \left(K_p + \frac{K_i}{s}\right)(P^* - P) \qquad (3.25)$$

$$i_q^* = \frac{Q^*}{v_d} + \left(K_p + \frac{K_i}{s}\right)(Q^* - Q) \qquad (3.26)$$

Here, P and Q are the measured active and reactive power from the ac filter of the grid.

3.3.3. AC voltage control

AC voltage controller can control the grid side voltage to a desired level by regulating the ac voltage reference. It also provides reactive current component i_q^* alike to the reactive power controller. This controller controls ac voltage by generating or absorbing exact amount of reactive power that is needed to match the measured ac voltage with the reference ac voltage.
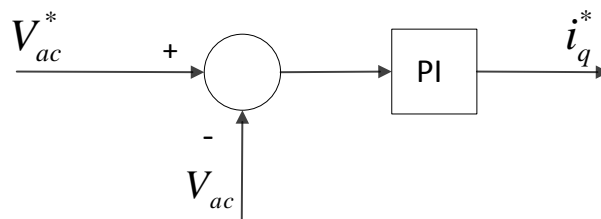

Figure 3.10: AC voltage controller block.

Power-synchronization control system

This strategy has been developed considering some difficulties during the vector controlled VSC-HVDC system connection with a weak ac system [17]. One of the difficulties is low frequency resonance, which can interfere inner current control loop therefore it affects the controller performance [17]. Moreover some investigations based on the phase locked loop (PLL) dynamics in the VSC-HVDC system connected with weak ac system has shown the negative impact of it to the system performance [17]. Therefore in this control method power synchronization strategy has been introduced to replace the PLL from the VSC-HVDC system [17]. Detail controlling method has discussed in this paper [17].

In this thesis vector control strategy has been used in the voltage source converter.

Chapter 4 : Improvement of the VSC controller

VSC controller improvement has been done considering the unbalanced fault condition occurrence during the operation and also to facilitate the power sharing in the multi-terminal dc systems.

4.1. Damping effect on dc voltage controller

From equation (3.15), it can be seen that dc link capacitor voltage u_{dc} has nonlinear correlation. Linearization of (3.15) will make the relation linear, which is

$$C_{dc} \frac{d\Delta u_{dc}}{dt} = \frac{v_d}{u_{dc}} \Delta i_d + \frac{i_d}{u_{dc}} \Delta v_d - \frac{v_d i_d}{u_{dc}^2} \Delta v_{dc} \tag{4.1}$$

So the transfer function of (4.1) from u_{dc} to i_d as defined in [18]

$$T.F = \frac{v_d}{u_{dc}} \frac{1}{s\, C_{dc}} \tag{4.2}$$

Transfer function of (4.2) has a pole at origin, therefore controlling of dc voltage is difficult with the proportional and integral gain. During unbalanced fault condition to provide the active damping on the dc voltage an additional inner feedback loop is introduced with a damping conductance (G_a) [18].
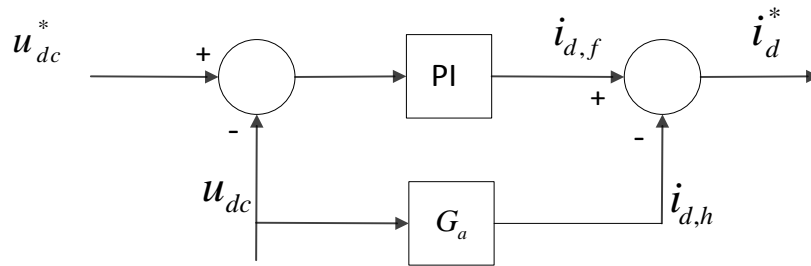

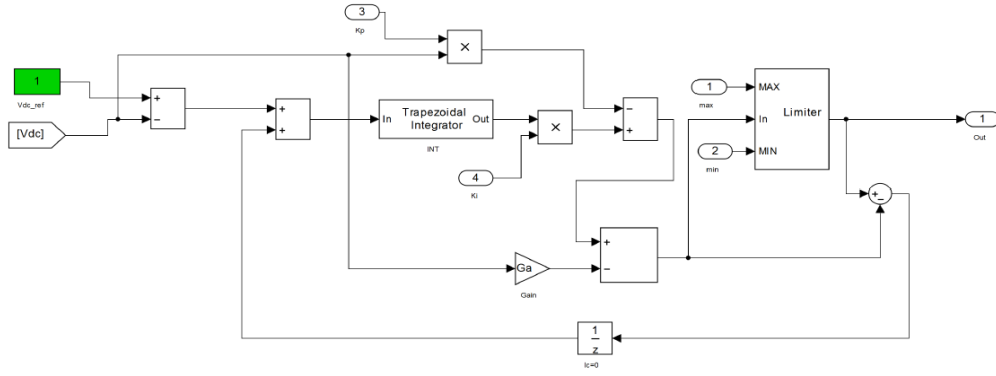**Figure 4.1:** DC voltage controller with active damping.

Figure 4.1 (b): Implementation of the dc voltage controller with active damping.

During unbalanced fault in the ac side of the system, harmonic current components appear with the fundamental current components. Resistive behavior for the harmonic components can be obtained by injecting a harmonic current in to the grid which is 180 degree out of phase with the grid voltage [19]. Therefore, the output current of converter with the damping effect will be [19]

$$i_d^* = i_{d,f} + i_{d,h}$$

$$= i_{d,f} - G_a u_{dc} \tag{4.3}$$

where, $i_{d,f}$ is fundamental current component, $i_{d,h}$ is harmonic current component and G_a acts as a resistance and provides resistive behavior to the harmonics and oscillations.

Implementation of the damping effect on the dc voltage controller is one of the contributed part of this thesis. The impact of using damping controller has been observed by applying it in the point to point VSC-HVDC system under unbalanced fault condition. Damping conductance calibration has been performed in order to get the damped dc voltage behavior during fault condition which will be shown in section 5 at figure 5.11.

4.2. Negative sequence current control

During normal operating condition, i.e. without any disturbance in the system, the summation of negative, positive and zero sequence component of voltages and currents is zero. Asymmetrical ac side fault affects three phase voltages and currents which decline the performance of the VSC. In this thesis the constant voltage source is connected with converter through a Y/Δ configured transformer, therefore zero sequence current from the converter can be excluded [20]. The negative sequence current appears with second order harmonics which causes dc link voltage dip and ac side line current larger to make the system unbalanced.

Consequently the adverse effect of the negative sequence current in the converter may disconnect the converter from the system. This situation can be prevented by providing more robust current control scheme, which is separately controlling of negative and positive sequence current components in the inner current controller [21].

In order to control the negative and positive sequence current separately, it is necessary to separate the components first. Delayed signal cancellation (DSC) method proposed in [21], has been used in this thesis for the sequence separation. Following block diagram represents the DSC scheme of the current sequence separation,
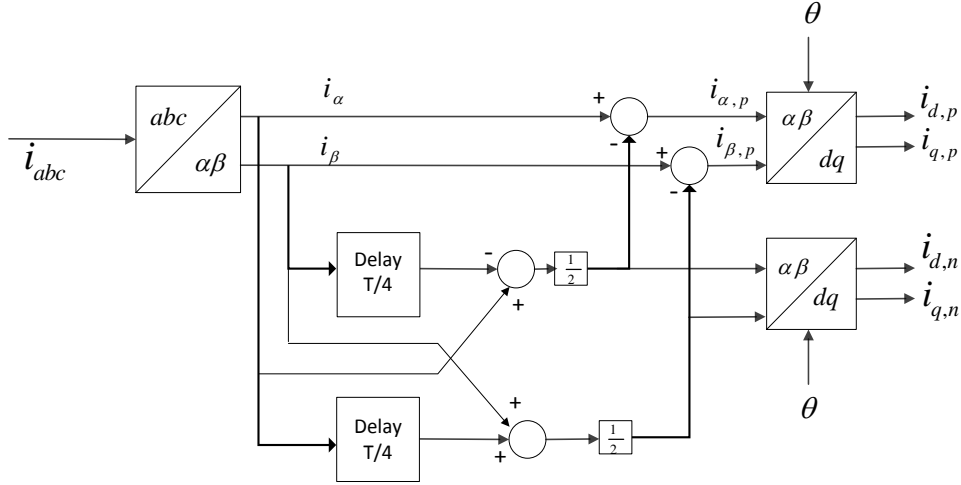

Figure 4.2: Positive and negative sequence current components separation block.

Applying DSC method, the expression of the sequences in the $\alpha\beta$ frame will be [6]

For negative components,

$$i_{\alpha,n}(t) = \frac{1}{2}\left\{i_\alpha(t) - i_\beta(t - \frac{T}{4})\right\} \tag{4.4}$$

$$i_{\beta,n}(t) = \frac{1}{2}\left\{i_\beta(t) + i_\alpha(t - \frac{T}{4})\right\} \tag{4.5}$$

For positive components,

$$i_{\alpha,p}(t) = i_\alpha(t) - i_{\alpha,n}(t) = \frac{1}{2}\left\{i_\alpha(t) + i_\beta(t - \frac{T}{4})\right\} \tag{4.6}$$

$$i_{\beta,p}(t) = i_\beta(t) - i_{\beta,n}(t) = \frac{1}{2}\left\{i_\beta(t) - i_\alpha(t - \frac{T}{4})\right\} \tag{4.7}$$

where, $i_{\alpha,n}, i_{\beta,n}, i_{\alpha,p}, i_{\beta,p}$ are the negative and positive current components in the $\alpha\beta$ frame and $T = 1/f$, here f is the fundamental frequency. Time delay of one quarter of a period is used in the DSC technique as outlined in [21].

Separated current components are now controlled in two inner current controller loops. Positive sequence current components are controlled in one loop and the negative sequence current components in another loop. Negative sequence current components are controlled in such a way that it becomes close to zero during unbalanced fault condition by setting the reference current at zero. The block diagram of the negative sequence inner current controller is shown below
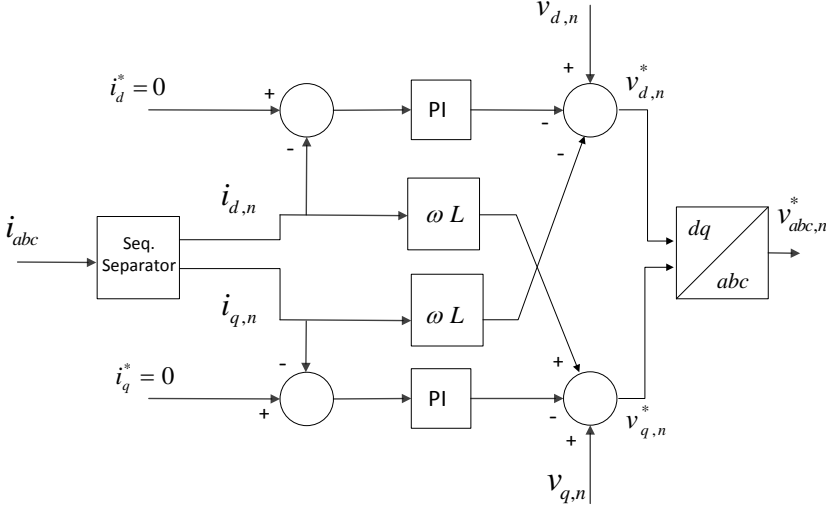

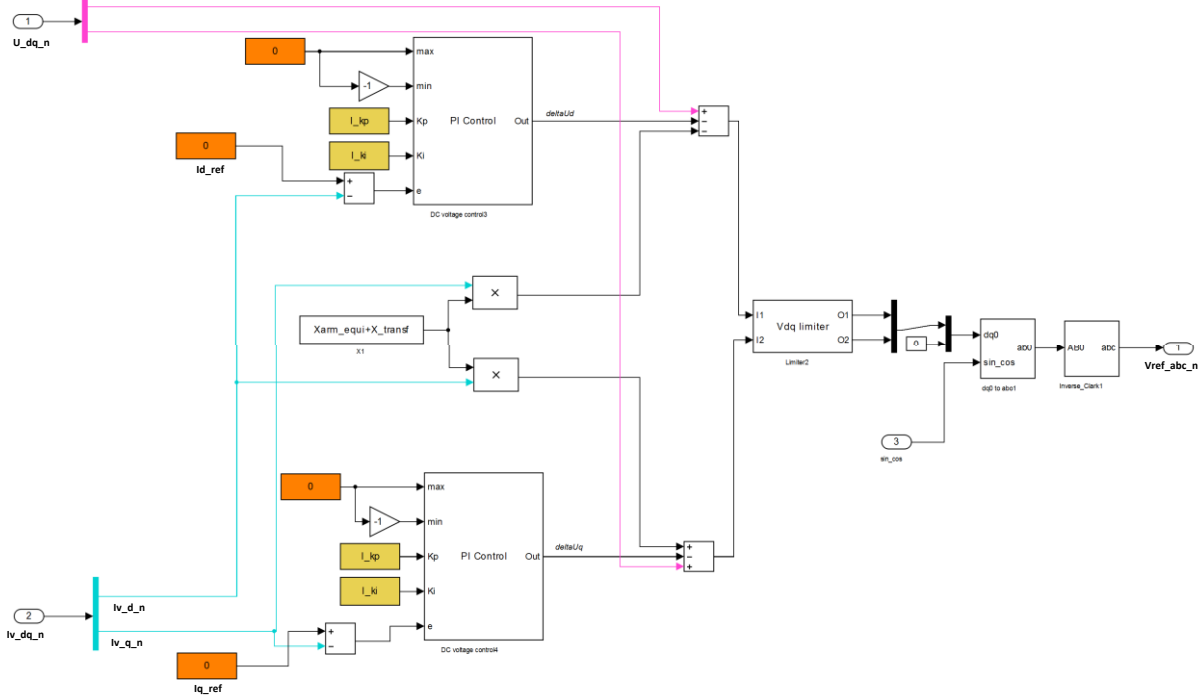**Figure 4.3 (a):** Negative sequence current controller block.

Figure 4.3 (b): Implementation of the negative sequence current controller.

Measured three phase currents i_{abc} from the grid are separated in the sequence separator block which is depicted in Figure 4.2. The negative sequence currents are then controlled in Figure 4.3. block and provides $v^*_{abc,n}$, three phase negative sequence reference voltages. Similarly three phase positive sequence reference voltages $v^*_{abc,p}$ are provided by positive sequence inner current control block. These two voltage references are added to get one voltage reference, i.e. $v^*_{abc} = v^*_{abc,p} + v^*_{abc,n}$ to provide in to the PWM.

In this thesis the negative sequence current controller has been developed and implemented in the point to point VSC-HVDC system. The outcome of the controller has also been observed and analyzed during unbalanced fault condition. The results are shown in section 5 at Figure 5.12.

4.3. DC voltage droop control

DC voltage droop control is mainly used in multi terminal dc grid. This controlling concept is based on the commonly applied voltage, frequency droop control in the parallelly connected generators to facilitate the load sharing.

Conventional active power and dc voltage controller shows following characteristics between active power (P) and dc voltage (u_{dc}) presented in Figure 4.4 (a) and 4.4 (b)
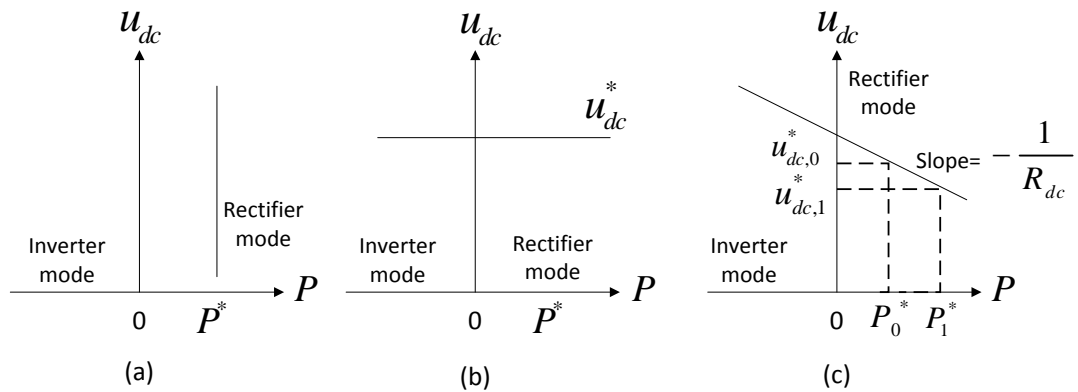

Figure 4.4: Active power and dc voltage characteristics of (a) active power controller, (b) dc voltage controller, (c) dc voltage droop controller.

Active power controller keeps the active power constant in spite of the dc voltage reference changes; similarly for dc voltage controller dc voltage is kept at its set value, regardless of the active power reference changes. Negative power flow represents inverter mode and positive power flow represents rectifier mode of operation.

DC voltage droop controller is the combination of active power and dc voltage controller with a pre-defined slope. The slope is given according to the dc voltage response (R_{dc}) [14], which provide linear change to the dc voltage in terms of active power reference change.

From Figure 4.4(c), it can be seen that when active power reference increases in the rectifier mode from P_0^* to P_1^*, it will decrease the initial dc voltage level $u_{dc,0}^*$ to $u_{dc,1}^*$ based on the slope.
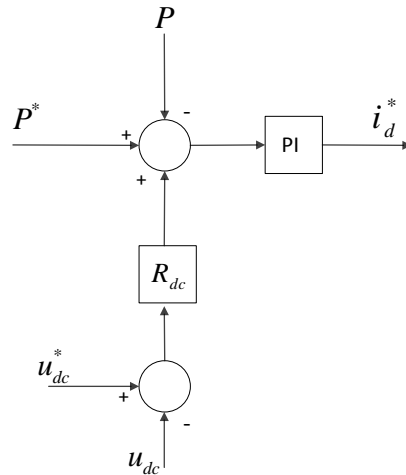

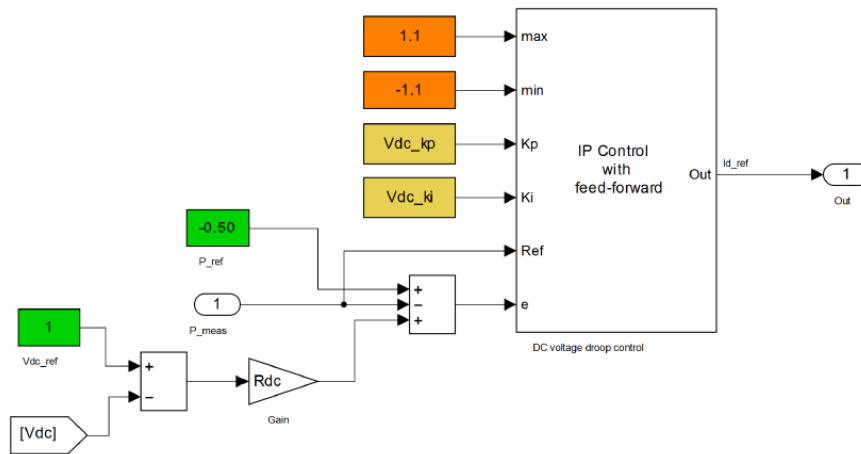**Figure 4.5 (a):** DC voltage droop controller.

Figure 4.5 (b): Implementation of the dc voltage droop controller.

Active current reference i_d^* is provided from the dc droop controller likely to the active or dc voltage controller. Assuming steady state error signal of the dc droop controller equals to zero then the equation leads to [14]

$$P^* - P + R_{dc}(u_{dc}^* - u_{dc}) = 0 \tag{4.8}$$

The dc voltage droop controller is implemented and simulated for different topologies of four terminal VSC-HVDC system, in this thesis. Besides the simulation results of with and without dc voltage droop controller has been observed and studied the impact of this controller benefit in the multi-terminal VSC-HVDC system. Simulation results are shown in section 5 at Figure 5.15 to 5.18.

Chapter 5: Test systems and off-line simulation results

5.1. Point to point VSC-HVDC test system
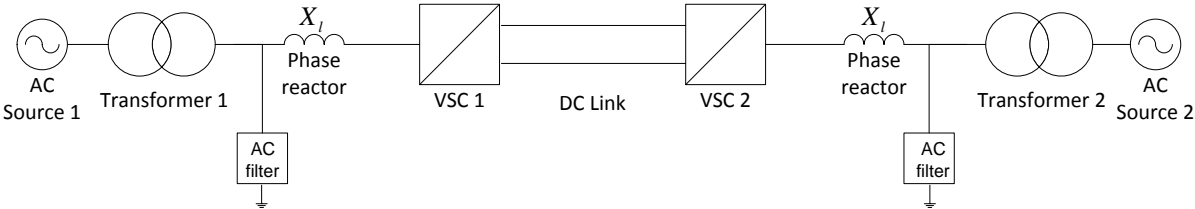
Figure 5.1: Point to point VSC-HVDC test system.

The test system shown in Figure 5.1 represents a point to point VSC-HVDC system. Two ac sources are connected through two converters with 750 km long dc links. This model has been built in Simulink with the help of SimPowerSystems library for the controller validation. Modular multilevel VSC converter topology has been used in this thesis.

System parameters of the modular multilevel converter are listed in the Table 5.1.

Table 5.1: Converter parameters.

Converter rating	305 MVA
AC voltage	380 KV RMS line to line
DC voltage	320 KV
Reactance of converter transformer	0.18%
Arm inductance	0.075%
Capacitor energy in each sub module	40 KJ/MVA
Number of sub module in each arm	20

Controller settings for the point to point topology are given below :

Table 5.2: Control strategy of the converters.

Converter	Controlling type	Parameter
VSC1 (rectifier)	Active power (P) and Reactive power (Q)	$P^* = 1\ p.u$, $Q^* = 0\ p.u$
VSC2 (inverter)	DC voltage (u_{dc}) and Reactive power (Q)	$u_{dc}^* = 1\ p.u$, $Q^* = 0\ p.u$

5.1.1. Tuning of the controller

Controller tuning requirement and methodology

The controllers are tuned based on the requirement of less overshoot, undershoot and settling time of the controller response. Firstly, active power controller is tuned to satisfy the active power flow with the set active power reference value. Secondly, dc voltage controller is tuned to assure the constant dc power through the overall system. Finally, reactive power controller is tuned to keep the ac voltage of the system at the desired set value.

Active power controller tuning

Implementing a step changes in VSC1 side active power reference P^*, from 1 p.u to 0.5 p.u at 2 sec. Active power controller has been tuned with the trial and error method.

Start changing the integral gain of active power controller K_i from zero and observe the steady state response of the controller. Following figure shows active power flow of VSC1 for different K_i values.
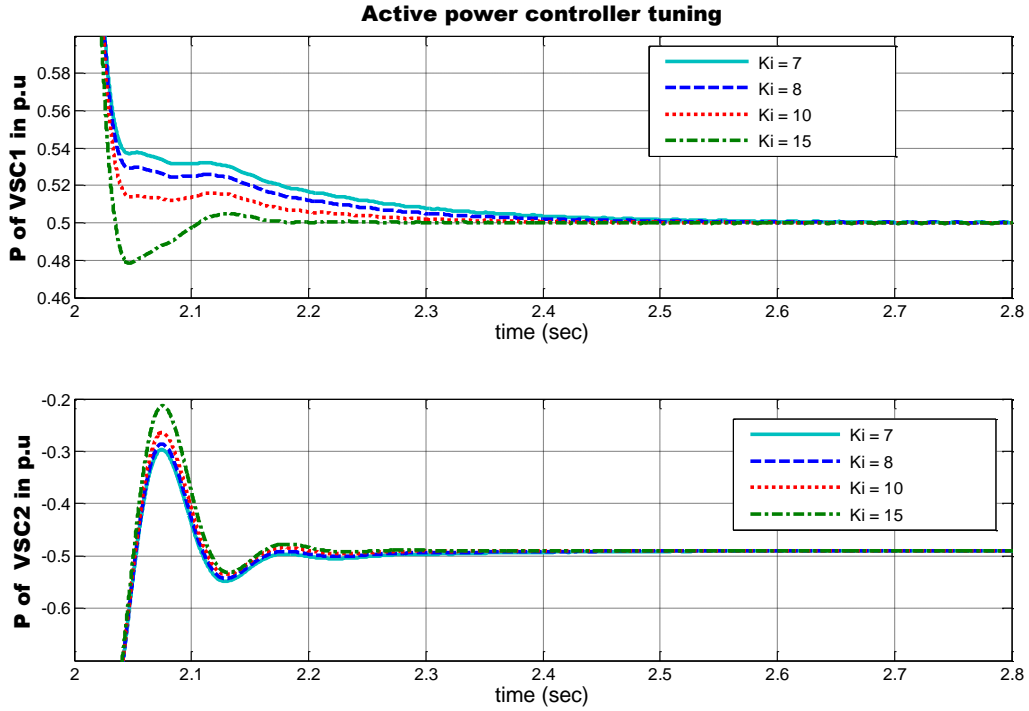
Figure 5.1: Active power flow of the converters for different K_i values.

Main concern of the tuning was to make the peak level during step changes low in terms of the steady state level, i.e. 0.5 p.u and decrease the converging time of the controller to steady state, which is also known as settling time.

Undershoot and settling time for different active power controller K_i values are listed bellow

Table 5.3: Active power controller response for different Ki values.

K_i	P-VSC1 (Undershoot in p.u)	Settling time in sec
7	No	0.70
8	No	0.60
10	No	0.38
15	0.478(4.4%)	0.30

From Table 5.3 it can be seen that, with the increasing K_i value settling time of active power flow in VSC1 side decreases. However from Figure 5.1, it also can be observed that for the active power flow in VSC2 side, overshoot during step change increases with the increasing K_i value. Therefore in spite of the set time decrement for VSC1 side, it is also important to take in account the overshoot of VSC2 side. Hence $K_i = 10$ has been chosen as the active power controller integral gain considering both side power flow condition based on the overshoot and response time.

DC voltage controller tuning

Similarly dc voltage controller has been tuned with trial and error method by implementing step changes in VSC2 side dc voltage reference V_{dc}^*, from 1 p.u to 0.8 p.u at 2 sec.
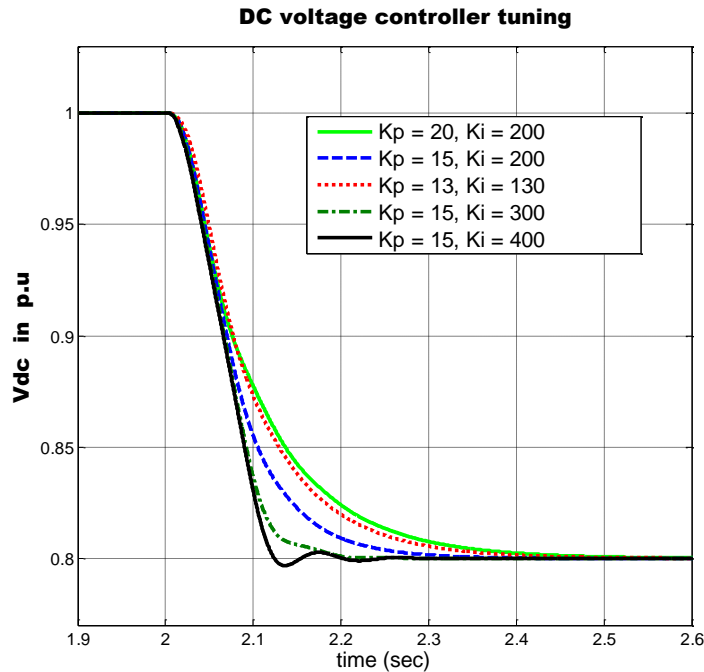

Figure 5.2: DC voltage for different $\boldsymbol{K_p}, \boldsymbol{K_i}$ values.

Undershoot and settling time for different dc voltage controller K_p, K_i values are listed bellow:

Table 5.4: DC voltage controller response for different Kp, Ki values.

K_p	K_i	V_{dc}(Undershoot in p.u)	Settling time in sec
20	200	No	0.52
15	200	No	0.40
13	130	No	0.50
15	300	No	0.20
15	400	0.796 (0.5%)	0.33

Observing dc voltage controller response for different gain values, K_p= 15 and K_i= 300 has been chosen in terms of no undershoot and less settling time.

Reactive power controller tuning

Step changes in VSC1 side reactive power reference Q^* from 0 p.u to 0.3 p.u at 2 sec has been applied for tuning.
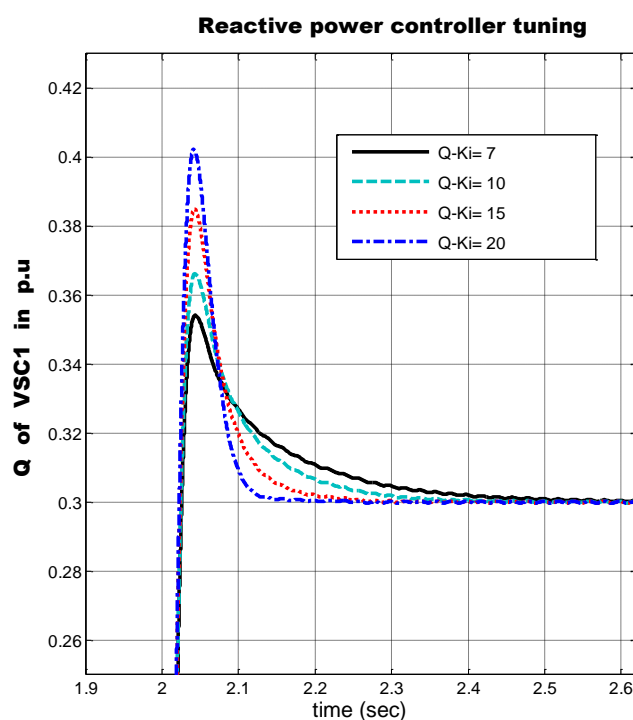

Figure 5.3: Reactive power flow for different K_i values.

Undershoot and settling time for different reactive power controller K_i values are listed bellow :

Table 5.5: Reactive power controller response for different Ki values.

K_i	Q-VSC1 (Overshoot in p.u)	Settling time in sec
7	0.35 (18%)	0.60
10	0.36 (22%)	0.42
15	0.38 (28.3%)	0.28
20	0.40 (33.3%)	0.25

According to the changing integral gain values, it can be seen from the Table 5.4 that, with the increasing K_i reactive power overshoot increases and the settling time decreases during step changes. However considering 33% overshoot as a maximum rate, K_i= 15 has been chosen in spite of having less set time for K_i= 20.

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AC voltage override controller tuning

Unbalanced fault in ac side of the system disturbs ac voltage therefore it will also affect reactive power of the corresponding fault occurring side. An ac voltage override controller has been used to control the reactive power during fault condition. To tune the ac voltage override controller a single phase to ground fault has been applied in between transformer and phase reactor in Figure 5.1 of VSC1 side. The fault occurred at 2 sec and cleared at 2.5 sec, while the reactive power references Q^* of both side converters were set to 0 p.u.
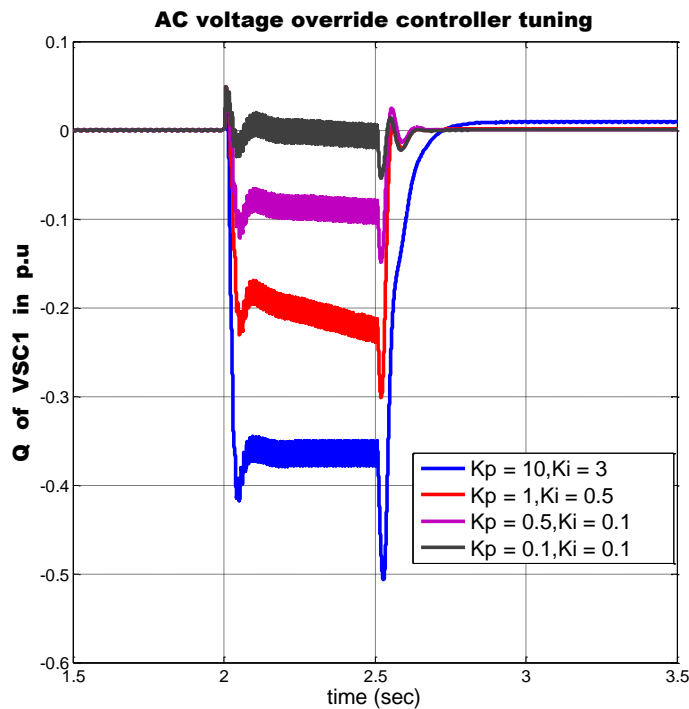

Figure 5.4: Reactive power flow for different K_p, K_i values.

From Figure 5.4, $K_p = 0.1 \; and \; K_i = 0.1$ shows the best response for reactive power flow during unbalanced fault as it follows the set reference 0 p.u more closely.

5.1.2. Test cases

In this chapter, all the simulation results for different test cases acquired from point to point test system depicted in Figure 5.1. Control strategy of two side converters VSC1 and VSC2 has already been mentioned in Table 5.2.

Active power controller

Active power reference of VSC1 side changes from 1 to 0.5 p.u at 1.5 sec and set back to 1 p.u at 2 sec.

To test active power controller, set the active power reference P^* at 1 p.u, reactive power reference Q^* at 0 p.u and dc voltage reference u_{dc}^* at 1 p.u. Changing the VSC1 side active power controller reference P^* from 1 to 0.5 p.u at 1.5 sec and setting back the active power reference P^* value to 1 p.u at 2 sec, the following simulation results are obtained.
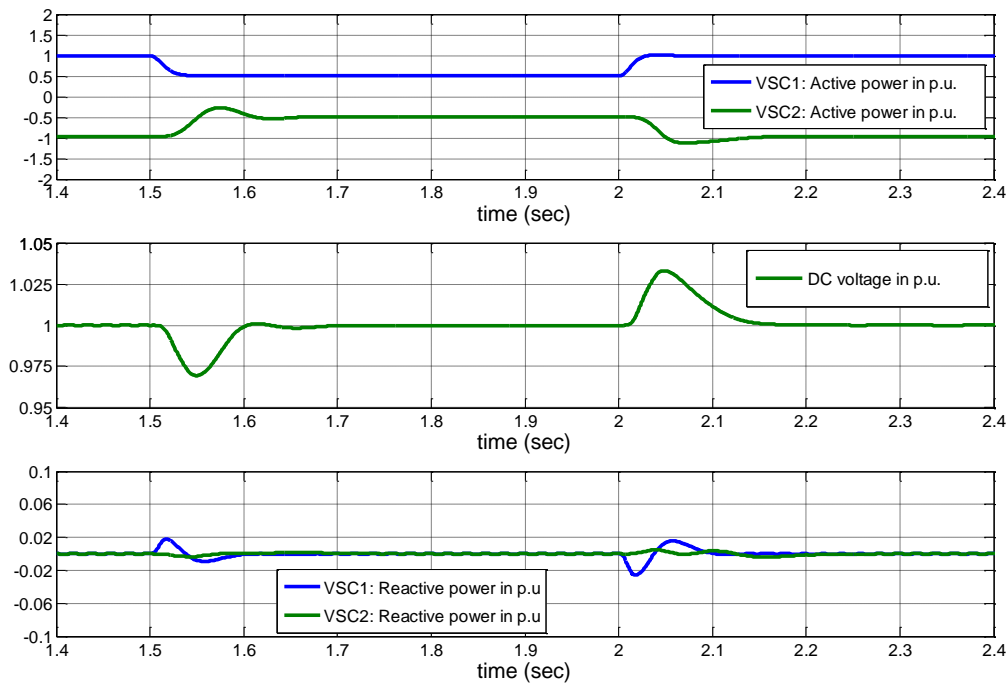

Figure 5.5: System responses for a step change in active power.

From the simulations it can be observed that active power flow in both of the directions of VSC-HVDC system responses stably with the power reference changes by the active power controller. This change affects the active current components therefore it also reflects to dc voltage at the beginning of step changes. Moreover because of the decoupling control effect,

active power change has very minor impact on the reactive current components so on the reactive power.

Reactive power controller

Reactive power reference of VSC2 changes from 0 to 0.3 p.u at 1.5 sec and set back to 0 p.u at 2 sec.

With active power reference P^* at 1 p.u, reactive power reference Q^* at 0 p.u and dc voltage reference u_{dc}^* at 1 p.u, reactive power reference of VSC2 is changed from 0 p.u to 0.3 p.u at 1.5 sec and again set back to 0 p.u at 2 sec.
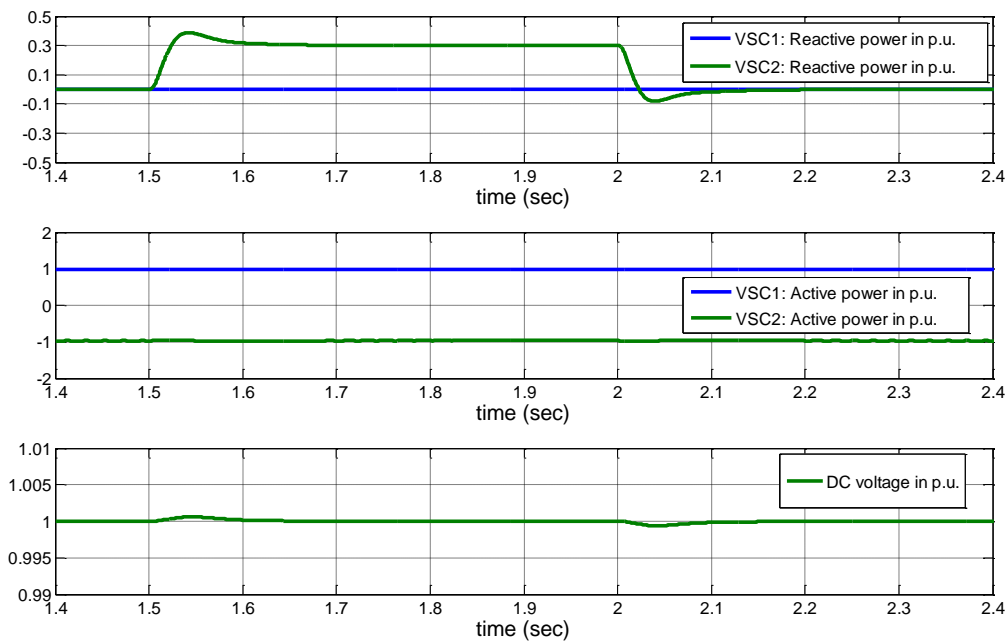

Figure 5.6: System responses for a step change in reactive power in VSC2 side.

From the simulation results, reactive power flow in the VSC2 side follows accordingly to the implemented reactive power step changes. Active power flow remains same at the set value 1 p.u and it is not affected by reactive power change in the system since the controller has decoupling effect. Reactive power in VSC1 side does not change with the reactive power change in VSC2 side, which represents that two converters can control reactive power independently from both sides. As reactive power change has major impact on the reactive current components and less on active current components, dc voltage is not affected much

DC voltage controller

DC voltage refernce changes from 1 to 0.9 p.u at 1.5 sec and set back to 1 p.u at 2 sec.

In order to test dc voltage controller, keep all the intial operating parameters of the sytem i.e. active power reference P^* at 1 p.u, reactive power reference Q^* at 0 p.u and dc voltage reference u_{dc}^* at 1 p.u. Then change the dc voltage reference u_{dc}^* from the initial value 1 p.u to 0.9 p.u at 1.5 sec and set the reference back to 1 p.u at 2 sec.
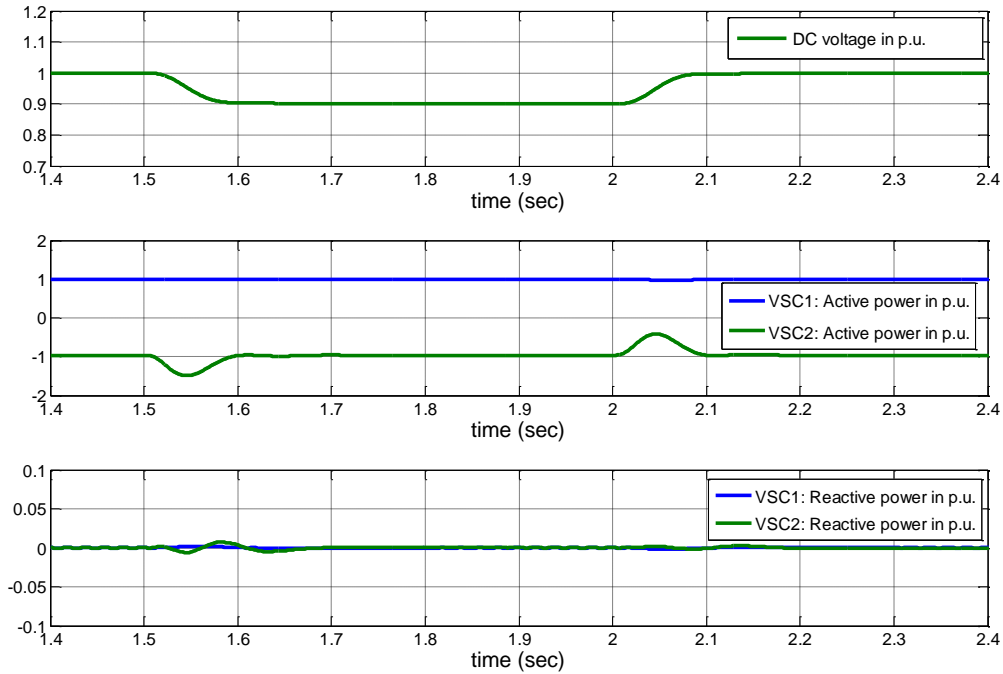

Figure 5.7: System responses for a step change in dc voltage.

Impact of dc voltage step change is similar to the active power change in the system. Active current components are affected therefore transient change in the active power flow occurs during the step change. Moreover dc voltage of the system maintains the reference change accordingly. Decoupling effect makes the reactive power flow less responsive.

Three phase to ground fault at VSC1 side

The fault occurs at 1.5 sec and clears at 2 sec of VSC1 side.

Three phase fault is the severe fault condition in the power system. Therefore to investigate the performance of the controller in VSC-HVDC system, a three phase to ground is implemented in the VSC1 side in between transformer and ac filter in Figure 5.1. The fault is applied at 1.5 sec and cleared at 2 sec with the similar initial operating parameters i.e. active power reference P^* at 1 p.u, reactive power reference Q^* at 0 p.u and dc voltage reference u_{dc}^* at 1 p.u.
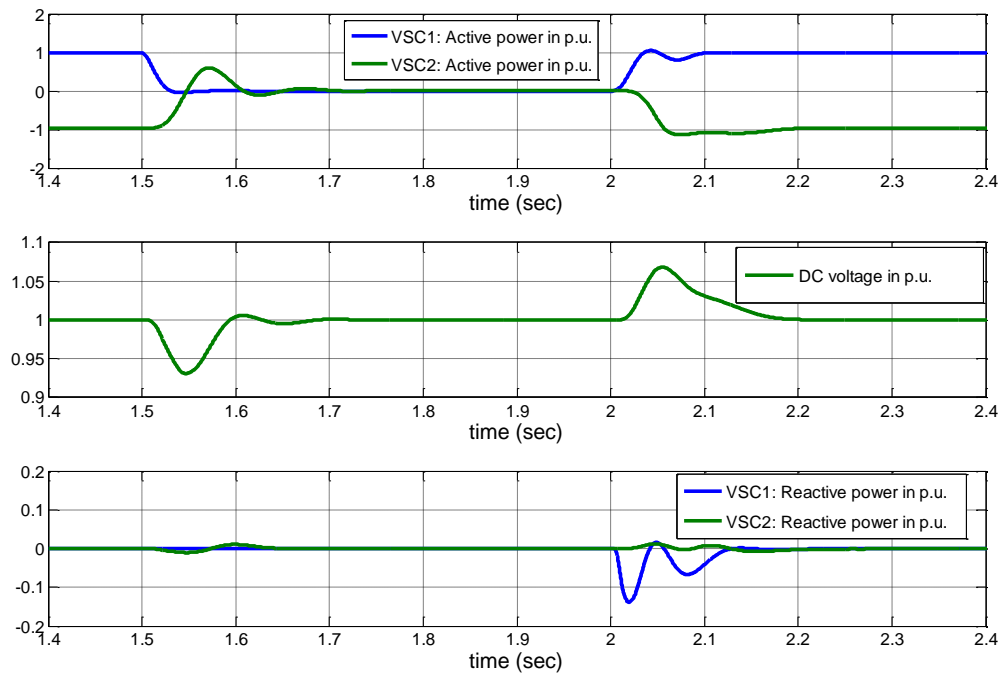
Figure 5.8: System responses for three phase to ground fault at VSC1 side.

From the simulation results, during fault condition active power flow from the VSC1 side decreases to zero, therefore the inverter side which is VSC2 does not get any power to receive. After the fault clearing active power retains to the steady sate value 1 p.u quickly. DC voltage decreases at the beginning of fault occurring and then dc voltage controller detects the voltage drop and increases it by charging the dc link capacitor hence dc voltage recovers at its set value 1 p.u. The opposite phenomena occurs during the fault clearing time, dc voltage controller detects over voltage therefore discharge the capacitor to reduce the voltage level at 1 p.u. Impact on reactive power is very less comparative to the active power flow.

Three phase to ground fault at VSC2 side

The fault occurs at 1.5 sec and clears at 2 sec of VSC2 side.

Three phase to ground fault is implemented in VSC2 side in between transformer and ac filter in Figure 5.1. Fault is implemented at 1.5 sec and cleared at 2 sec with the similar initial operating parameters.
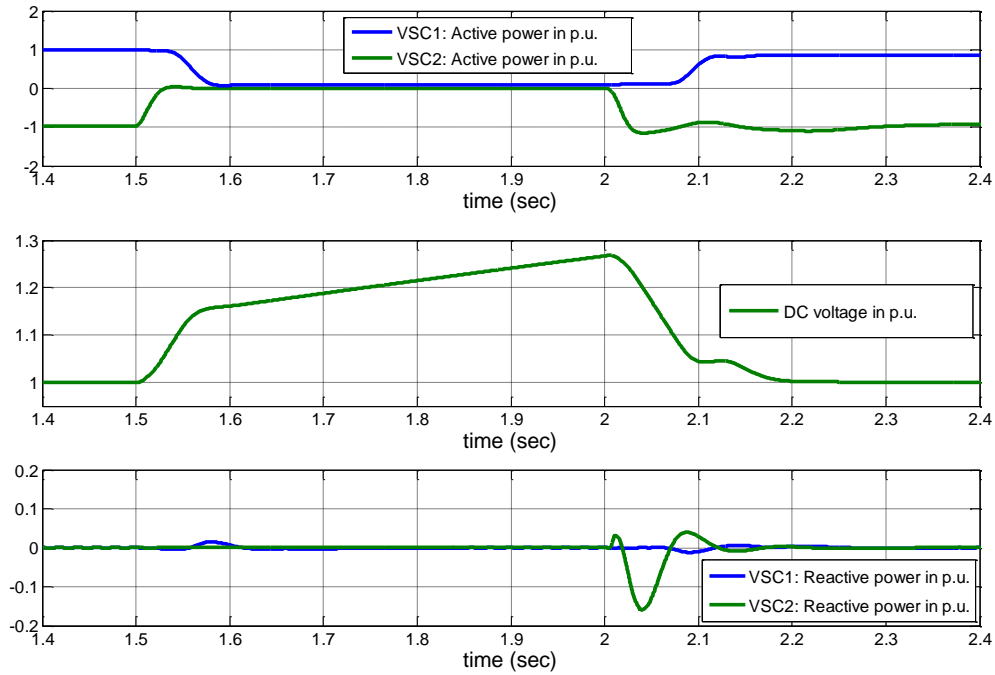
Figure 5.9: System responses for three phase to ground fault at VSC2 side.

Fault in VSC2 side makes the converter unable to exchange active power from dc to ac side, therefore dc voltage level increases as the active power flowing from VSC1 to VSC2 side. DC voltage controller limits this dc voltage increment within acceptable range. When the fault is cleared dc voltage controller starts healing the dc voltage level to the steady state value 1 p.u. Similarly it shows minor impact on the reactive power flow.

Single phase to ground fault at VSC1 side

The fault occurs at 2 sec and clears at 2.5 sec of VSC1 side.

During unbalanced fault in the system, second order harmonics appear in the system voltages and currents which disturb steady state operating condition of the system. Therefore in section 4.1 and 4.2 two improvements in the control scheme have been discussed based on the unbalanced fault condition.

In this case, VSC-HVDC system behavior during unbalanced fault, i.e. single phase to ground fault is investigated with and without implementing the modified controlling scheme of section 4.1 and 4.2.

To observe the impact of active damping on dc voltage controller, a single phase to ground fault is applied in VSC1 side at 2 sec and cleared at 2.5 sec with the initial operating condition of the system, active power reference P^* at 1 p.u, reactive power reference Q^* at 0 p.u and dc voltage reference u_{dc}^* at 1 p.u.
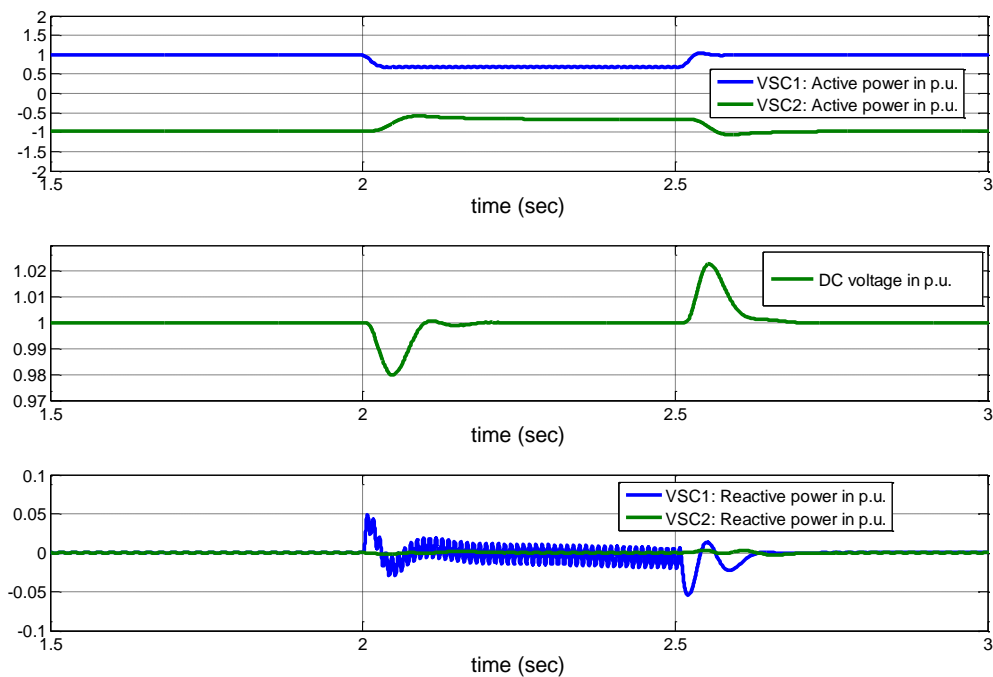
Figure 5.10: System responses for single phase to ground fault at VSC1 side without implementing damping on dc voltage controller.

It is seen from the simulation results that ripple appears in the VSC1 side therefore reactive power oscillates with high frequency. Moreover dc voltage dip appears as the fault affects active power flow of the system.

Main objective of active damping implementation on the dc voltage controller is to attenuate this voltage dip. It doesn't have impact on the active power flow; therefore only dc voltage simulation results are shown in figure 5.11 for different damping conductance G_a which has already discussed in section 4.1.
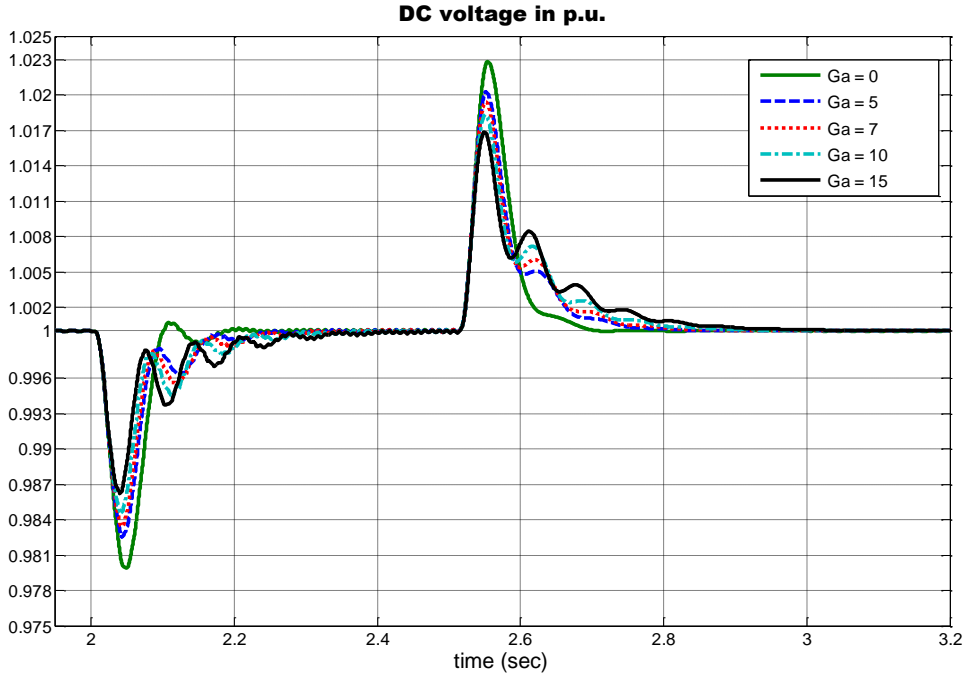
Figure 5.11: DC voltage for single phase to ground fault at VSC1 side with the implementation of damping effect on dc voltage controller.

From Figure 5.11, damping conductance $G_a = 0$ denotes there is no damping effect on the dc voltage controller also it can be seen that, with increasing damping conductance value, dc voltage dip decreases but the response time to the steady state increases. Following table represents attenuation and response time of dc voltage for the different conductance values.

Table 5.6: DC voltage for different conductance values.

G_a	1st peak of dc voltage in p.u.	2nd peak of dc voltage in p.u.	Response time (sec)
0	0.980	1.023	0.71
5	0.983	1.020	0.76
7	0.984	1.019	0.80
10	0.985	1.018	0.87
15	0.986	1.016	1.08

Though voltage dip decreases with the increasing conductance value, with higher value it starts to oscillate, hence $G_a = 10$ is chosen as the amplitude decrease and response time is less among other conductance values.

In order to test the negative sequence current controller described in section 4.2, again a single phase to ground fault is applied in VSC1 side at 2 sec and cleared at 2.5 sec with the same initial system operating condition.
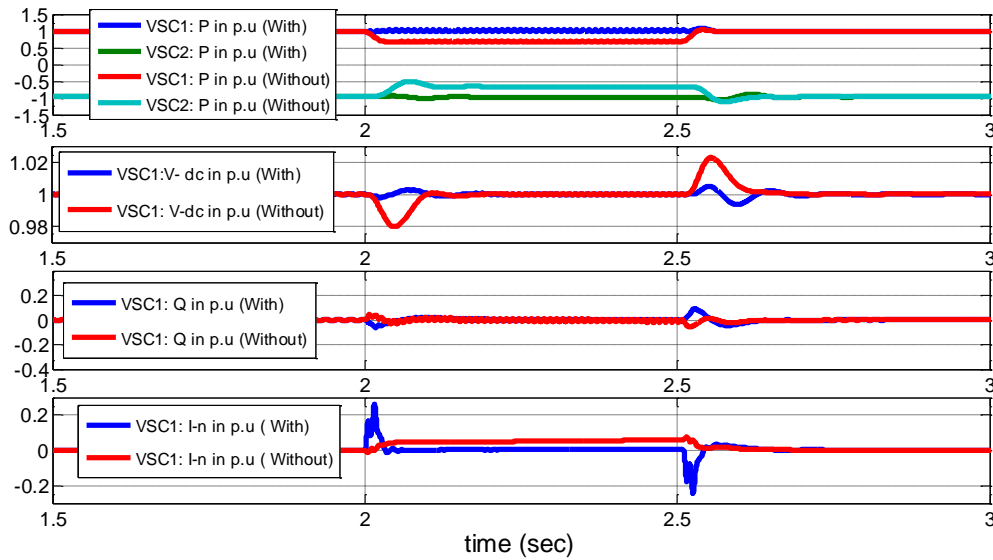

Figure 5.12: System responses for single phase to ground fault at VSC1 side with and without implementing negative sequence current control.

From Figure 5.12, it can be observed that after implementing negative sequence current controller system response improves significantly. As the negative sequence current controller suppresses the harmonics containing negative sequence current from the system as shown in last simulation, it reduces the active power drop and maintains the active power flow almost at 1 p.u. In the figure with and without denotes with negative sequence current controller and without negative sequence current controller respectively. DC voltage of the system also improves considerably than without using negative sequence current controller.

5.2. Four terminals VSC-HVDC test system
5.2.1. Introduction

Multi-terminal VSC-HVDC is one of the main types of the dc grid topologies [12], where more than two VSC connected with the dc grids.

In this chapter all the simulations are carried out based on four points VSC-HVDC system. Four ac voltage sources are connected together with the four converters by 750 km long dc links. Two different multi-terminal dc grid topologies were considered, (1) two converters act as rectifier and two as inverter, (2) one converter acts as rectifier and rest of the three as inverter.

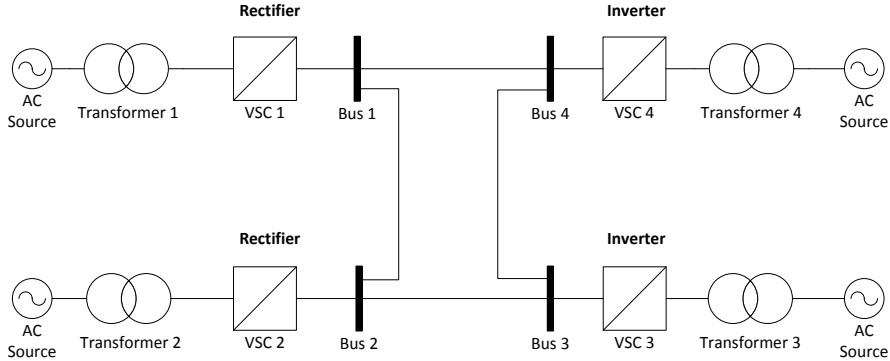Following test system depicts topology - 1

Figure 5.13: Four terminals VSC-HVDC test system, topology - 1.

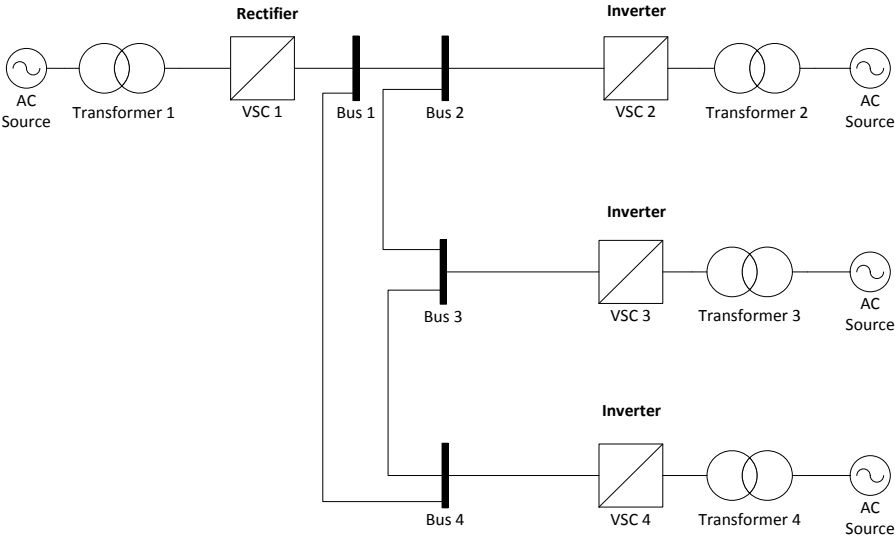VSC-HVDC test system with topology − 2 has shown below:

Figure 5.14: Four terminals VSC-HVDC test system, topology - 2.

Same converter parameters have been used in both of the topologies mentioned in Table 5.1.

5.2.2. Test cases

In order to observe the behavior of dc voltage droop controller discussed in section 4.3 in four-point dc grid system, several test simulations were carried out with and without

implementation of dc voltage droop controller in the system. Therefore two control strategies have been set for the converter (a) with dc voltage droop controller, (b) without dc voltage droop controller.

Following controller settings were applied for topology – 1

Table 5.7: Converters controller settings for topology - 1.

Control strategy	Converter	Controlling type	Parameter
(a) With DC voltage droop controller	VSC1 (rectifier)	Active power (P) and Reactive power (Q)	$P^* = 0.5\ p.u,$ $Q^* = 0\ p.u$
	VSC2 (rectifier)	Active power (P) and Reactive power (Q)	$P^* = 0.5\ p.u,$ $Q^* = 0\ p.u$
	VSC3 (inverter)	DC voltage droop ($u_{dc} - droop$) and Reactive power (Q)	$P^* = -0.5\ p.u,$ $u_{dc}^* = 1\ p.u,$ $Q^* = 0\ p.u,$ $R_{dc} = \frac{1}{0.04}$
	VSC4 (inverter)	DC voltage droop ($u_{dc} - droop$) and Reactive power (Q)	$P^* = -0.5\ p.u,$ $u_{dc}^* = 1\ p.u,$ $Q^* = 0\ p.u,$ $R_{dc} = \frac{1}{0.04}$
(b) Without DC voltage droop controller	VSC1 (rectifier)	Active power (P) and Reactive power (Q)	$P^* = 0.5\ p.u,$ $Q^* = 0\ p.u$
	VSC2 (rectifier)	Active power (P) and Reactive power (Q)	$P^* = 0.5\ p.u,$ $Q^* = 0\ p.u$
	VSC3 (inverter)	DC voltage (u_{dc}) and Reactive power (Q)	$u_{dc}^* = 1\ p.u,$ $Q^* = 0\ p.u$
	VSC4 (inverter)	Active power (P) and Reactive power (Q)	$P^* = -0.5\ p.u,$ $Q^* = 0\ p.u$

Controller settings for topology – 2 are listed below

Table 5.8: Converters controller settings for topology - 2.

Control strategy	Converter	Controlling type	Parameter
(a) With DC voltage droop controller	VSC1 (rectifier)	Active power (P) and Reactive power (Q)	$P^* = 1\, p.u,$ $Q^* = 0\, p.u$
	VSC2 (inverter)	DC voltage (u_{dc}) and Reactive power (Q)	$u_{dc}^* = 1\, p.u,$ $Q^* = 0\, p.u$
	VSC3 (inverter)	DC voltage droop ($u_{dc} - droop$) and Reactive power (Q)	$P^* = -0.33\, p.u,$ $u_{dc}^* = 1\, p.u,$ $Q^* = 0\, p.u,$ $R_{dc} = \frac{1}{0.1}$
	VSC4 (inverter)	DC voltage droop ($u_{dc} - droop$) and Reactive power (Q)	$P^* = -0.33\, p.u,$ $u_{dc}^* = 1\, p.u,$ $Q^* = 0\, p.u,$ $R_{dc} = \frac{1}{0.1}$
(b) Without DC voltage droop controller	VSC1 (rectifier)	Active power (P) and Reactive power (Q)	$P^* = 1\, p.u,$ $Q^* = 0\, p.u$
	VSC2 (inverter)	DC voltage (u_{dc}) and Reactive power (Q)	$u_{dc}^* = 1\, p.u,$ $Q^* = 0\, p.u$
	VSC3 (inverter)	Active power (P) and Reactive power (Q)	$P^* = -0.33\, p.u,$ $Q^* = 0\, p.u$
	VSC4 (inverter)	Active power (P) and Reactive power (Q)	$P^* = -0.33\, p.u,$ $Q^* = 0\, p.u$

To test the dc voltage droop controller in to the multi-terminal dc grid, following test cases were considered:

Test 1(Implemented in topology-1)

The VSC2 converter losses at 2 sec.

In topology 1, considering the loss of VSC2 converter at 2 sec with the system parameter settings listed in Table 5.7. Therefore the impact of the converter loss with and without dc voltage droop controller can be observed in the following simulation results
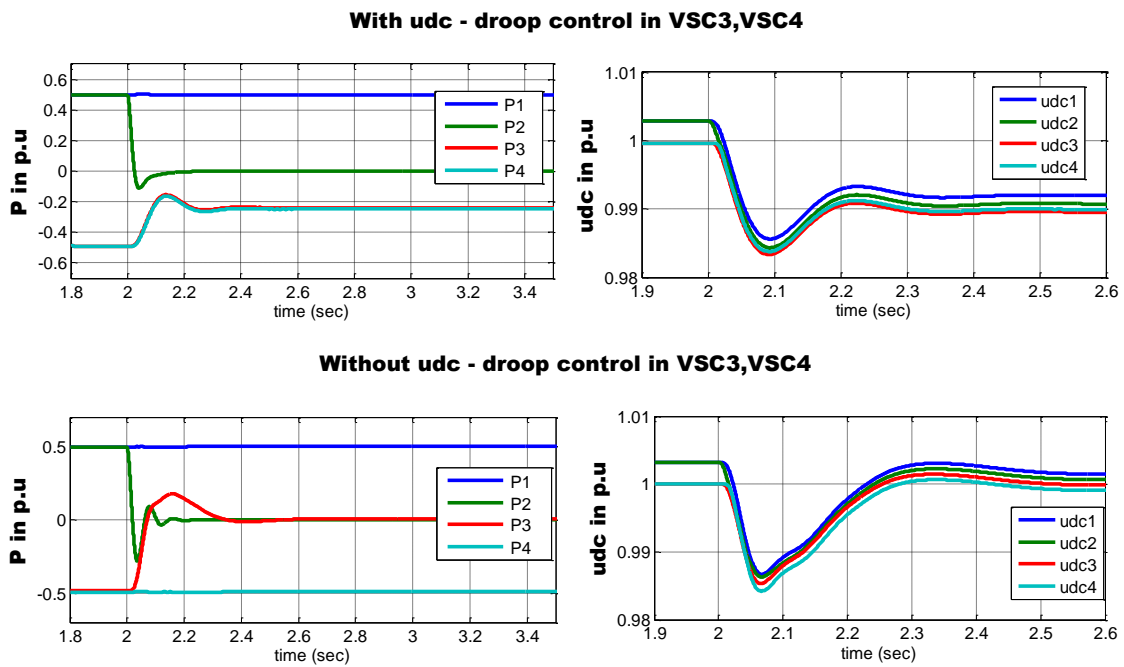

Figure 5.15: System responses with and without DC voltage droop controller for VSC2 loss at 2 sec

From Figure 5.15, it can be seen that initially two rectifiers VSC1, VSC2 provides 1 p.u active power in total and rest of the inverter VSC3, VSC4 receives that power equally in both cases. After the loss of converter VSC2, power flow reduces to 0.5 p.u from the rectifier side. During this time dc voltage droop controller facilitates equal power sharing between the converters VSC3 and VSC4. On the other hand without dc voltage droop control, VSC4 was set to control the active power hence when power reduces to half of it VSC4 keeps the active power consumption to the set value, i.e. -0.5 p.u. As all of the power is consumed by the VSC4 terminal, VSC3 which was set to dc voltage control reduces to zero power absorption.

According to the dc voltage droop controller equation (4.8) we can evaluate the dc voltage because of active power change after losing converter VSC2 in the following way,

$$(P^*\text{-}P) + R_{dc}(u_{dc}^* - u_{dc}) = 0$$

$$(\text{-}0.5+0.25)+(\frac{1}{0.04})\,(1\text{-}u_{dc}\,) = 0, \text{ where } [R_{dc}=\frac{1}{0.04}]$$

$$\text{So, } u_{dc} = 0.99 \text{ p.u}$$

Test 2(Implemented in topology-1)

Active power flow of VSC1 changes from 0.5 p.u to 0.3 p.u at 2 sec.

In topology 1, active power flow of VSC1 changes from 0.5 p.u to 0.3 p.u at 2 sec, where VSC2 continuously provides 0.5 p.u active power. All the initial system parameters are kept same as the previous test case.
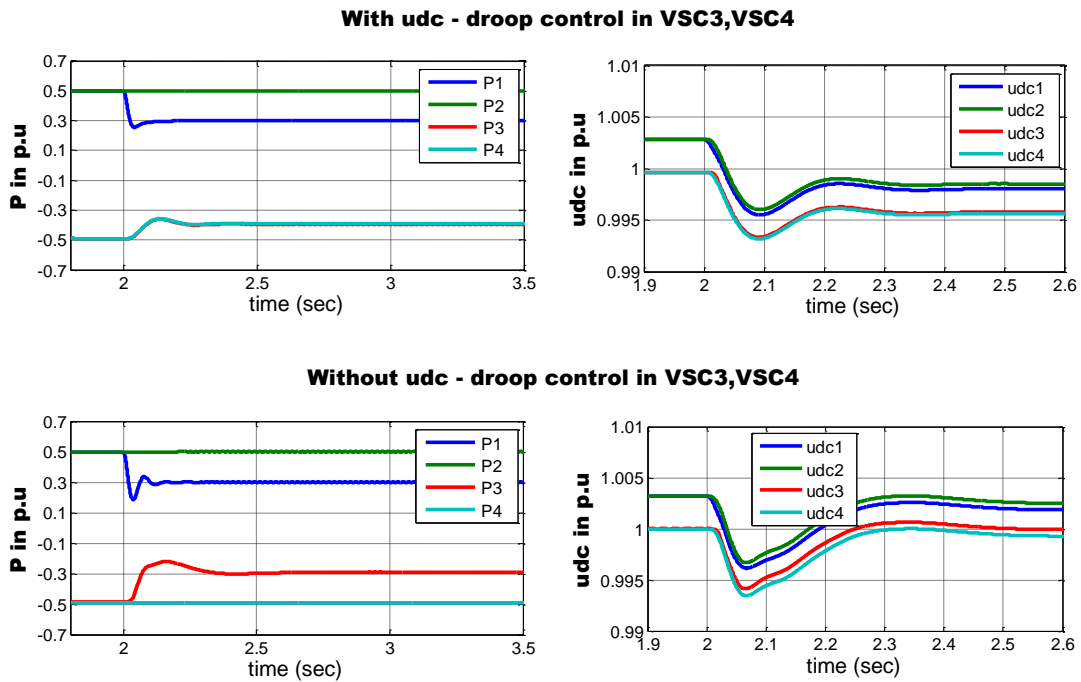

Figure 5.16: System responses with and without DC voltage droop controller for active power change in VSC1 side at 2 sec.

After reducing active power at 2 sec, net power flow from the rectifier side will be 0.8 p.u. From Figure 5.16 we can observe the impact of the reduced power flow for both cases. With the dc voltage droop controller the rest of the power is consumed equally by the two inverters VSC3 and VSC4, but without droop control VSC4 keeps the consumption at -0.5 p.u as it is active power controlled. Therefore dc voltage controlled inverter receives rest of the power -

0.3 p.u. Here negative sign indicates consumption of power. Similarly dc voltage changes linearly according to the predefined slope with the active power change in the dc voltage droop controller.

Test 3(Implemented in topology-2)

The converter VSC3 changes power from -0.33 p.u to -0.38 pu at 3 sec and VSC4 changes the power from -0.33 p.u to -0.48 p.u at the same time.

This test case is implemented in topology 2 only for dc voltage droop control strategy (a) from Table 5.8, where one converter acts as converter and rest of the three as inverter. 1 p.u active power is provided by the VSC1 rectifier, and VSC2, VSC3 and VSC4 shares equal amount of power initially, i.e. 33.3%.
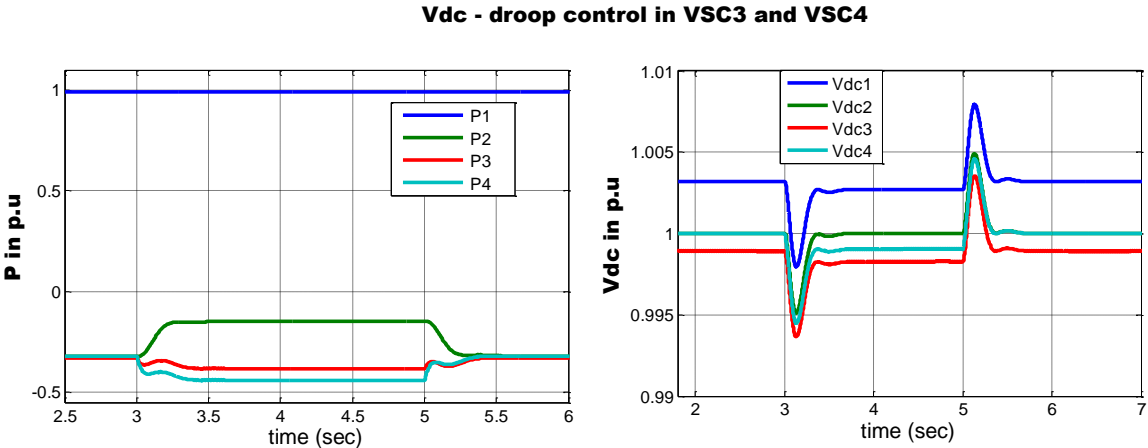

Figure 5.17: Active power share change of VSC3 (-33% to -38%) and VSC4 (-33% to -48%) from 3 to 5 sec

Active power sharing capability of the dc voltage droop controlled converter is depicted in this test. VSC3, VSC4 converters are set to the dc voltage droop controller and VSC2 converter is fixed to dc voltage control. VSC3 starts changing power from -0.33 p.u to -0.38 pu at 3 sec and VSC4 changes the power from -0.33 p.u to -0.48 p.u at the same time; here negative sign represents power consumption. Therefore power sharing by the dc voltage controlled converter VSC2 during 3 to 5 sec reduces to -0.14 p.u from -0.33 p.u.

DC voltage level has been slightly affected during the transition of the active power, and retains to the steady state level shortly.

Test 4(Implemented in topology-2)

The converter VSC3 is lost from 2 to 4 sec during the system operation.

In topology 2, the loss of VSC3 converter is considered from 2 to 4 sec during the system operation. The impact of losing one of the inverter is observed in this test for droop and without droop controller in the system.
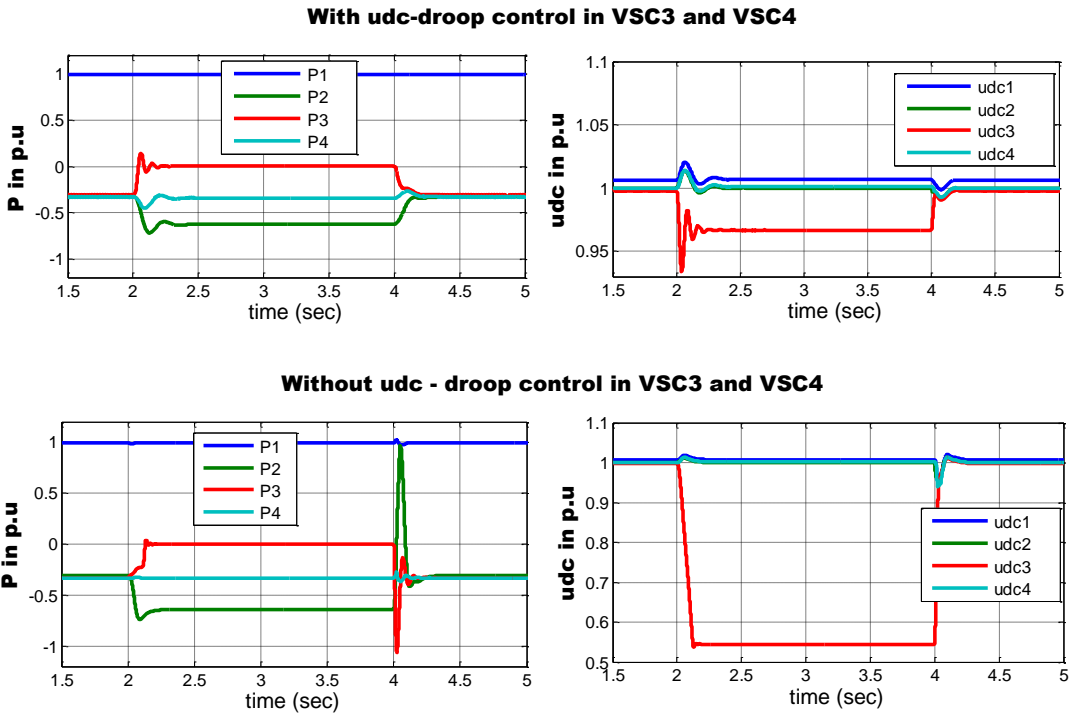

Figure 5.18: System responses with and without DC voltage droop controller for loss of VSC3 at 2 sec and recovered at 4 sec.

During the loss of VSC3 , with dc voltage droop control power sharing between droop controlled converter VSC4 and dc voltage controlled converter VSC2 is smooth. VSC4 keeps the consumption level at the set value -0.33 p.u and rest of the power is consumed this time by VSC2.DC voltage level of the VSC3 side does not go below to 0.967 p.u from 1 p.u because of the predefined dc voltage response R_{dc}.

Without dc voltage droop control, as the VSC4 converter is active power controlled, so the power consumption by this converter will be same all the time. Therefore VSC2 converter

which is dc voltage controlled becomes responsible for the power flow adjustment in the system. During the recovery time of the VSC3 converter, robustness of the VSC4 converter creates high level of power peak and oscillation in both VSC2 and VSC3 converters. Moreover VSC3 side dc voltage reduces to its minimum voltage level as the capacitor discharges.

Chapter 6 : Real time simulation results

6.1.   Introduction

In this section, real time simulations are carried out for previously discussed point to point and 4 points VSC-HVDC Simulink models. To make the Simulink models compatible for the real time simulator, some modification has been done.

In order to simulate point to point VSC-HVDC model in real time with the Opal-RT software, first of all the entire model has to be rearranged mainly into three subsystems, which are master, slave and console subsystems. Both of the master and slave subsystems can contain computational elements of the model, mathematical operation blocks, input-output blocks, signal generator etc. [22]. However one model must have one master subsystem and might have several slave subsystems. Therefore, the rectifier side of the point to point VSC-HVDC model i.e. rectifier, controller, three phase voltage source and transformer are included to the master subsystem. On the other hand inverter side elements are included to the slave subsystem. In the console subsystem all the user interface blocks which are scopes to observe the different parameters of the system, switches to implement different step changes, faults during the execution of the model, control mode selectors etc. In RT-LAB OpComm block has been used to enable and save communication setup information between console and computational nodes [22].Therefore, all subsystems inputs are connected via OpComm blocks.

Following figures are showing the model of three subsystems for the real time simulator. In Figure 6.2 only master subsystem is presented, which is exactly identical with the slave subsystem. All of the monitoring signals of the system are directed to the console block of Figure 6.3.

Four terminals VSC-HVDC model has similar configuration to the point to point model with one master subsystem, three slave subsystems and one console subsystem.
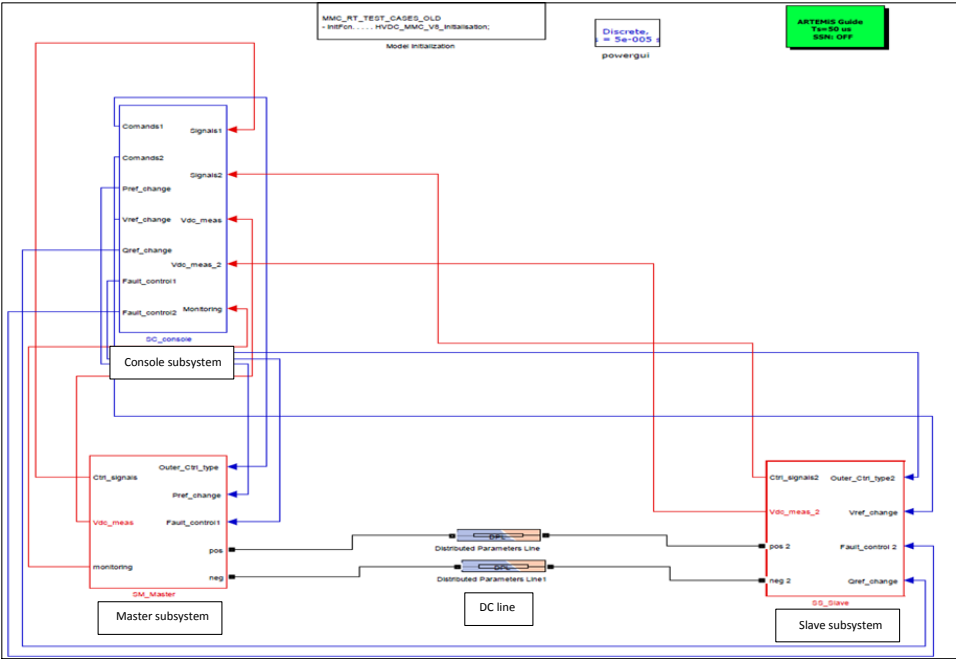

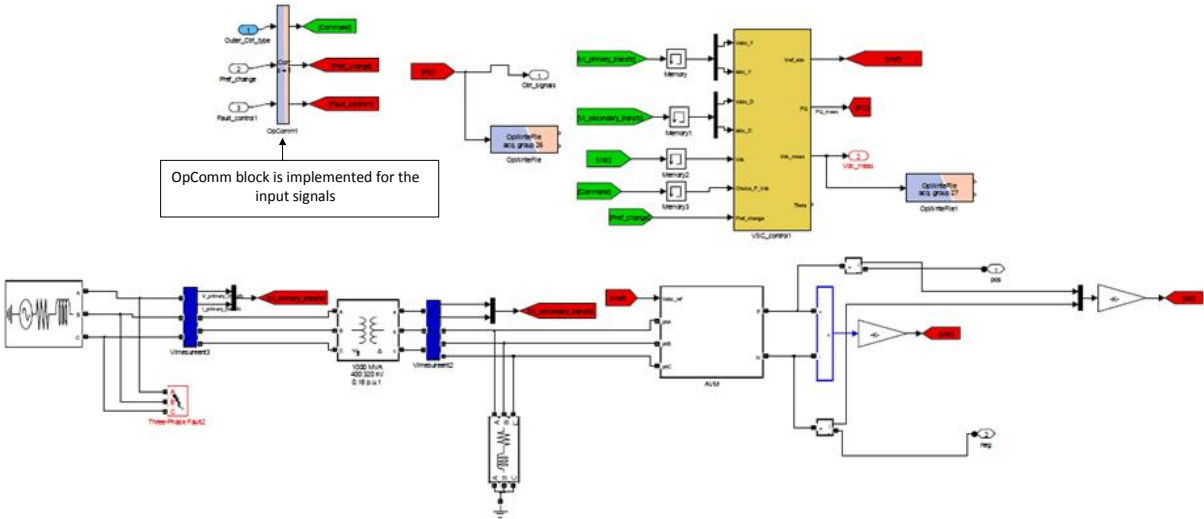**Figure 6.1:** Modified point to point VSC-HVDC model for the Opal-RT software.

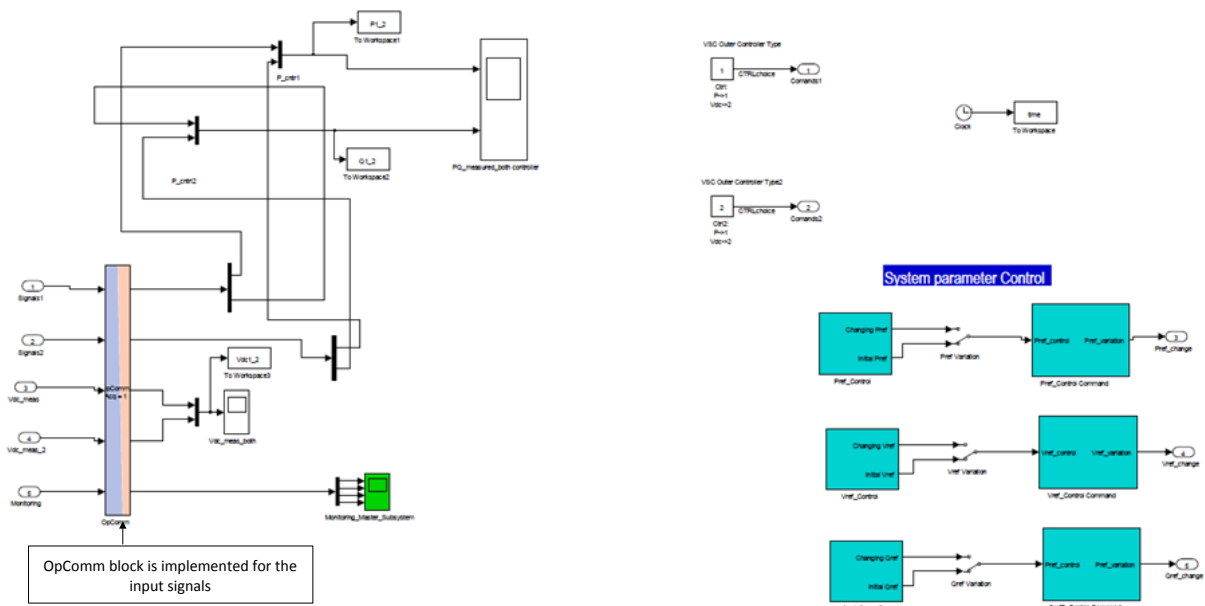**Figure 6.2:** Master subsystem with the OpComm block.

Figure 6.3: Console subsystem block diagram.

6.2. Simulation results

Point to point VSC-HVDC test system depicted in Figure 5.1 has been used to simulate the test cases in real time simulator with the same converter parameters, control strategies and initial operating conditions listed in Table 5.1 and 5.2 respectively.

In order to observe the dynamic performances of the VSC-HVDC model in real time following test cases has been carried out.

Figure 6.4 represents the system responses in real time for a step change in active power reference of VSC1 side from 1 p.u to 0.5p.u is applied at 5 sec and set back to the initial value 1 p.u at 7 sec.
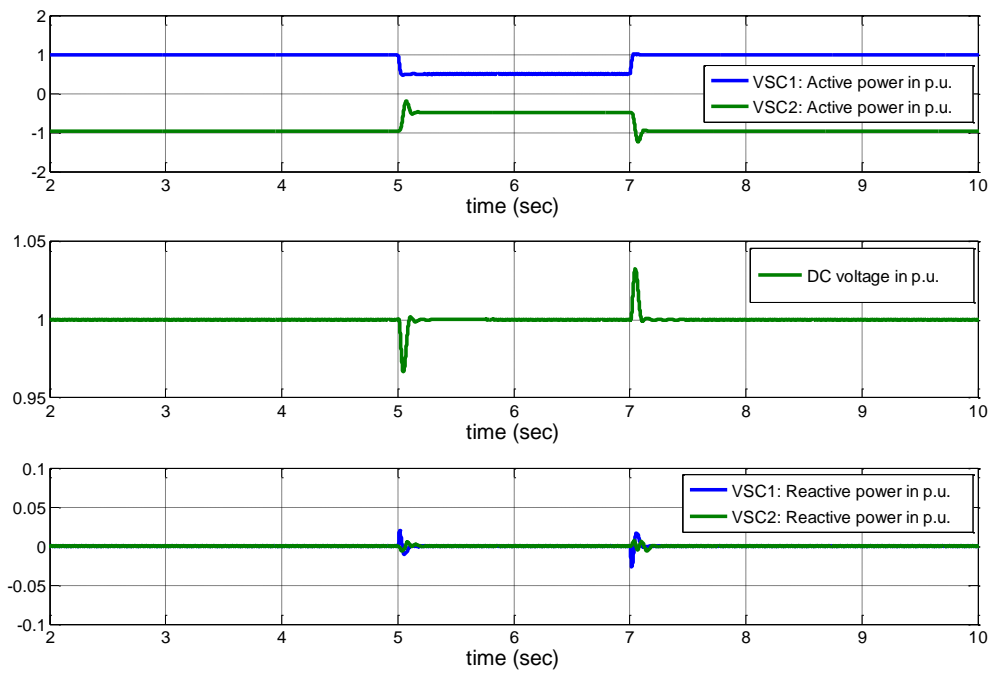
Figure 6.4: Point to point VSC-HVDC system responses in real time simulator for a step change in active power.

Figure 6.5 represents the system responses in real time for a step change in reactive power reference of VSC2 side from 0 p.u to 0.3 p.u is applied at 25 sec and set back to the initial value 0 pu at 27 sec.
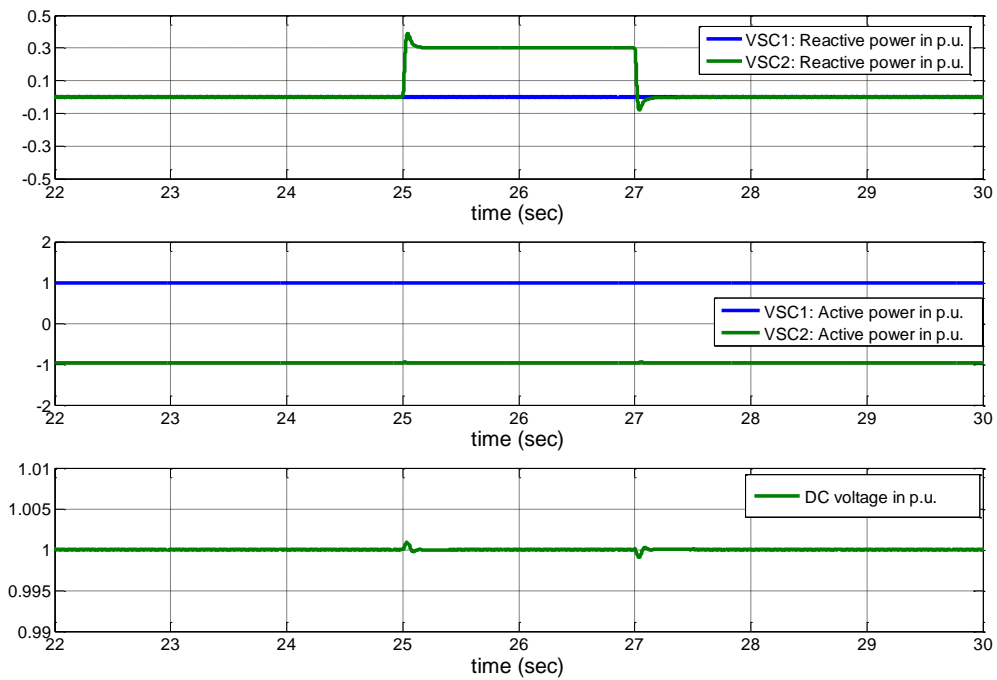
Figure 6.5: Point to point VSC-HVDC system responses in real time simulator for a step change in reactive power.

Figure 6.6 represents the system responses in real time for a step change dc voltage reference of VSC2 side from 1 p.u to 0.9 p.u is applied at 15 sec and set back to the initial value 0 p.u at 17 sec.
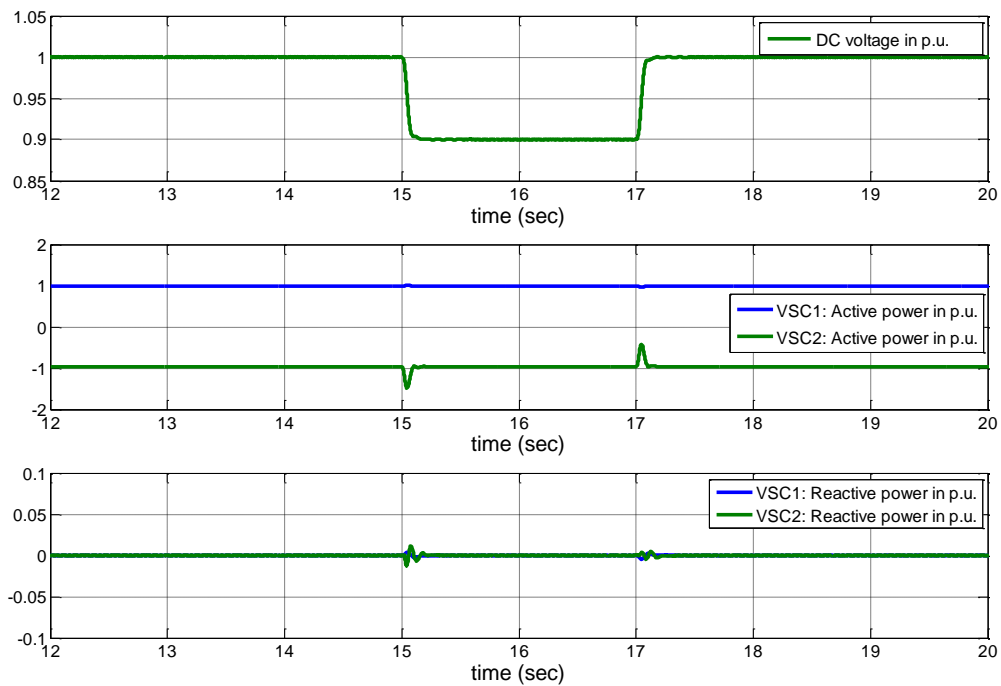
Figure 6.6: Point to point VSC-HVDC system responses for a step change in dc voltage in real time simulator.

Figure 6.7 represents the system responses in real time for three phase to ground fault in VSC1 side occurs at 45 sec and clears at 45.20 sec.
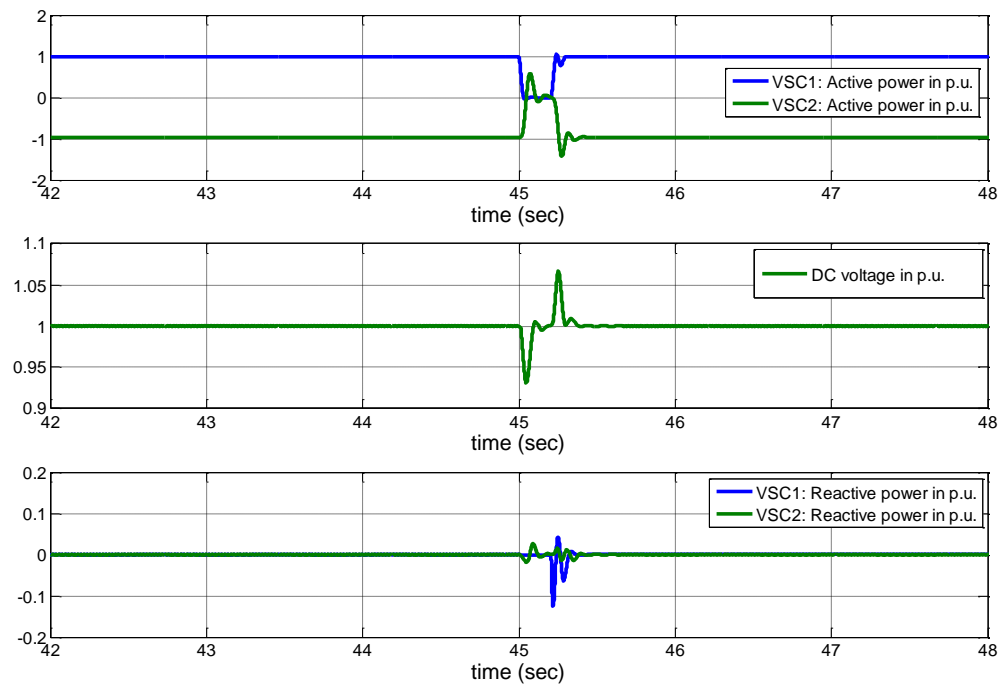

Figure 6.7: Point to point VSC-HVDC system responses in real time simulator for three phase to ground fault at VSC1 side.

Figure 6.8 represents the system responses in real time for three phase to ground fault in VSC2 side occurs at 35 sec and clears at 35.20 sec.
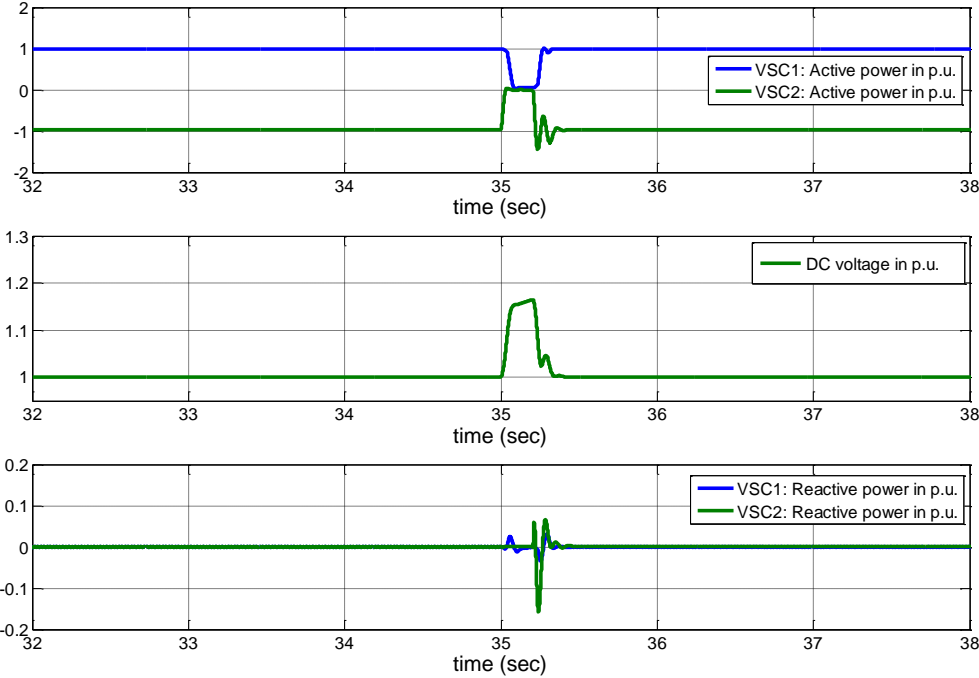

Figure 6.8: Point to point VSC-HVDC system responses in real time simulator for three phase to ground fault at VSC2 side.

Figure 6.9 represents the system responses in real time for single phase to ground fault in VSC1 side occurs at 45 sec and clears at 45.20 sec.
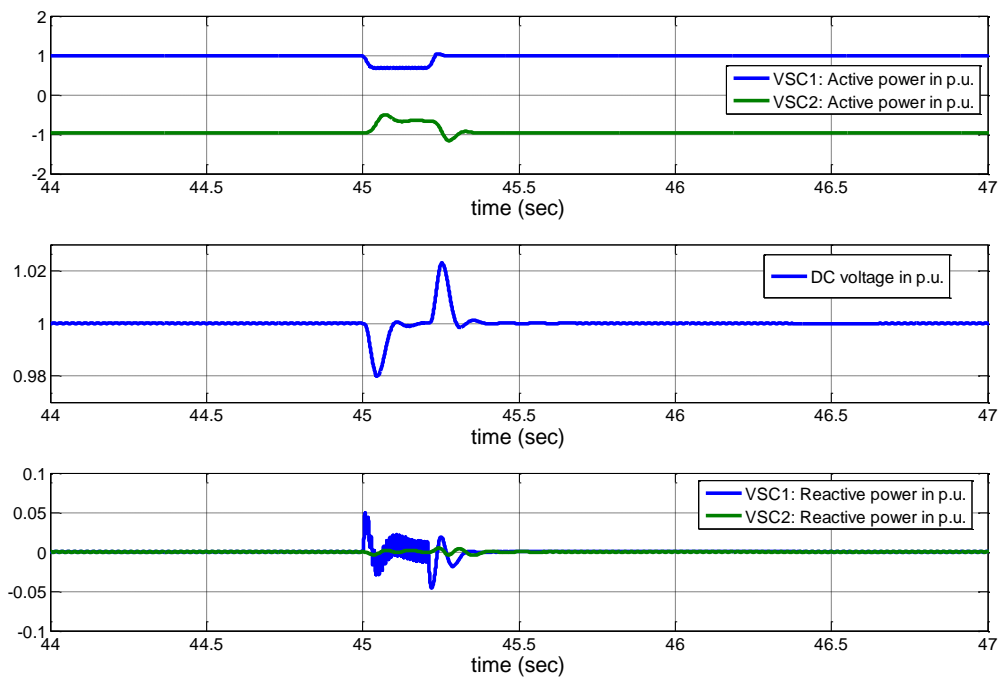
Figure 6.9: Point to point VSC-HVDC system responses in real time simulator for single phase to ground fault at VSC1 side.

Figure 6.10 represents the system responses with the negative sequence current controller in real time for single phase to ground fault in VSC1 side occurs at 45 sec and clears at 45.20 sec.
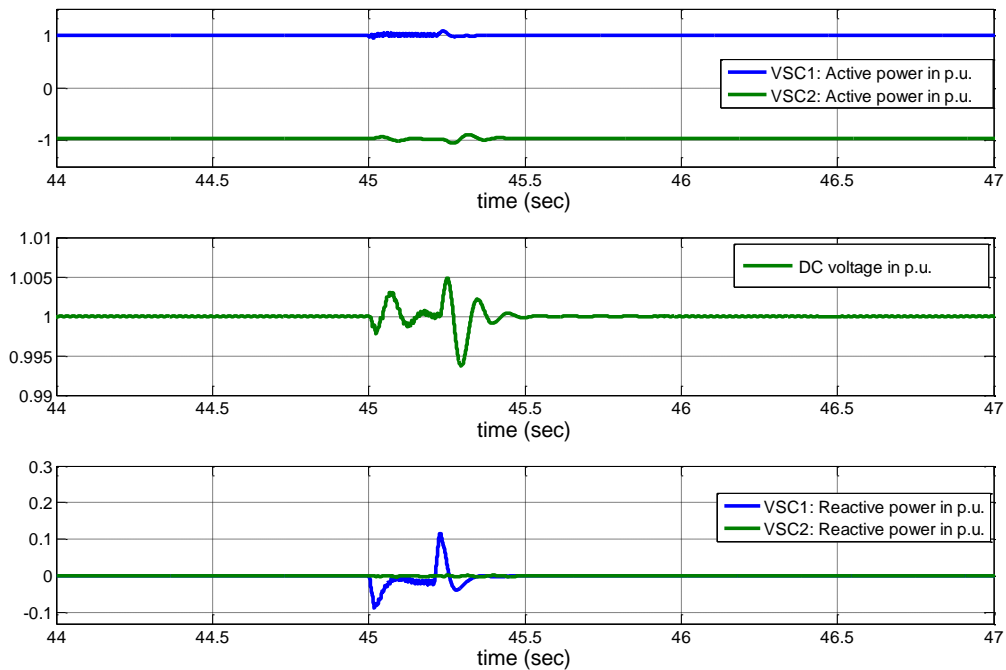
Figure 6.10: Point to point VSC-HVDC system responses in real time simulator with negative sequence current controller for single phase to ground fault at VSC1 side.

Four points VSC-HVDC test systems shown in Figure 5.13 and 5.14 have been used to simulate the test cases in real time simulator with the same converter parameters listed in table 5.1. Notice that, from Table 5.7 and 5.8 only control strategy (a) which is, with dc voltage droop controller has been considered for the real time simulation of four points VSC-HVDC system. Moreover the initial operating conditions remain same as the Table 5.7 and 5.8.

In topology-1, of Figure 5.13 with the dc voltage droop controller, an step change of active power reference from 0.5 p.u to 0.3 p.u is applied at 5 sec and set back to the previous value 0.5 p.u at 7 sec and keep all other parameters same. With this step change following figure represents the four points VSC-HVDC system responses in real time simulator.

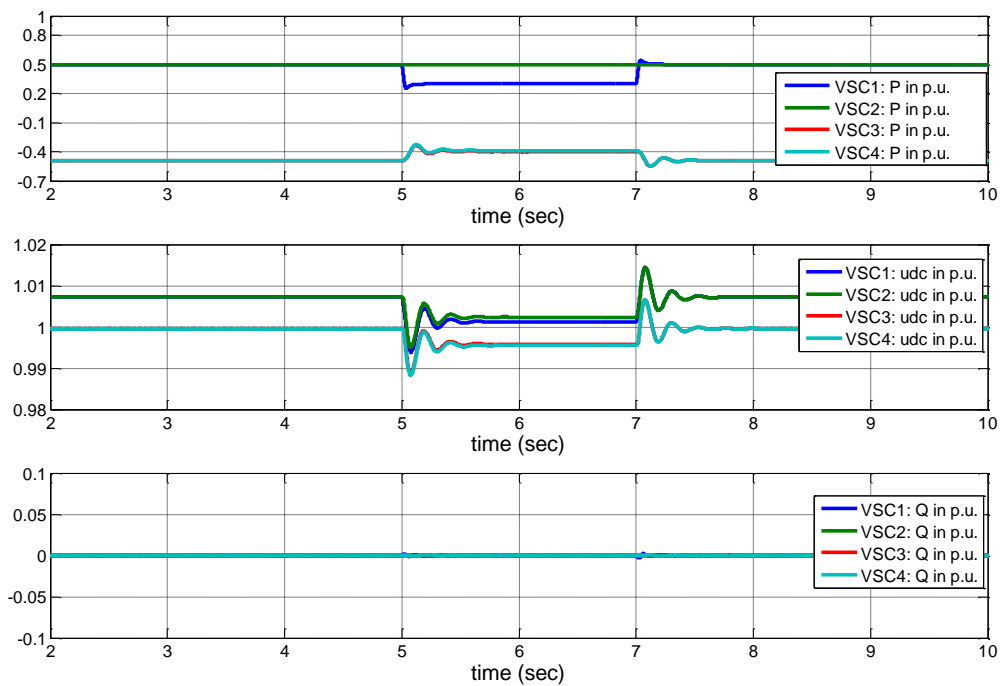**Figure 6.11**: Four terminals VSC-HVDC system responses with DC voltage droop controller in real time simulator for active power change in VSC1 side.

In topology-2, shown in Figure 5.14 with the dc voltage droop controller, VSC3 inverter is lost at 25 sec and come back to the operation at 30 sec, where all other parameters remain same. Following figure represents the system responses for the loss of VSC3 inverter.
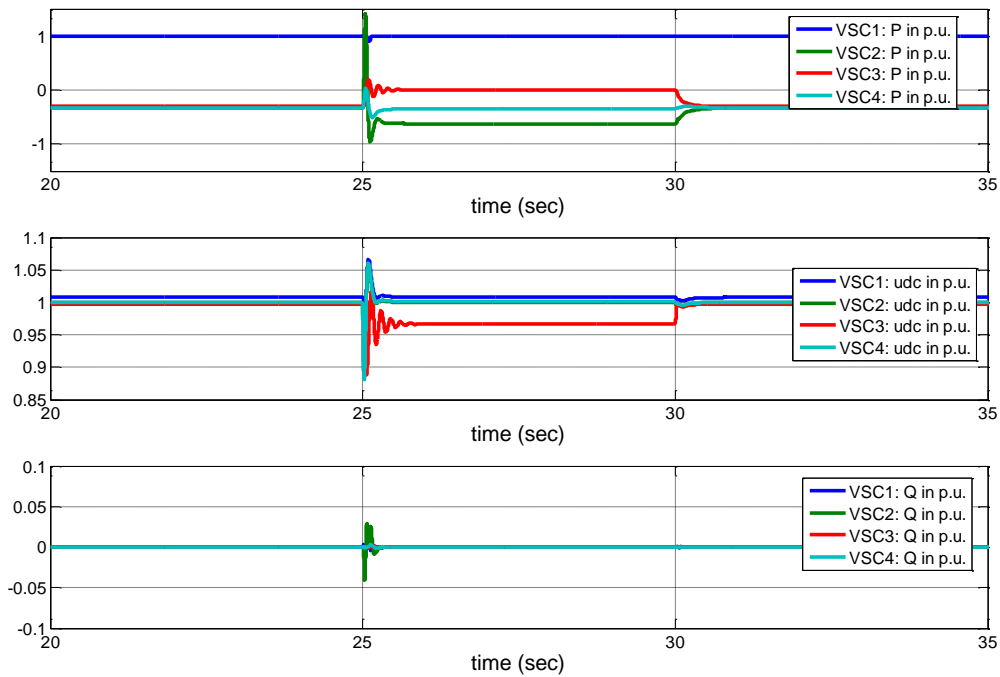
Figure 6.12: Four terminals VSC-HVDC system responses in real time simulator with DC voltage droop controller for loss of VSC3.

Controller responses in the real time simulator shown in the above figures are fast and stable; it shows similar behavior as the off-line simulation results. Therefore, it can be said that all of the developed point to point and four terminals VSC-HVDC models will be able to withstand in the real time steady state and fault conditions.

Performance analysis:

Timing information of the real time simulation can be obtained by using OpMonitor block, which is a monitoring block consists in the Opal-RT library. The OpMonitor block provides "Computation time", "Real step size", "Idle time" and "Number of overruns" which is important to analyze whether the used current step in the real time simulation is appropriate or there is a possibility to reduce the step size.

Following figures have shown the point to point VSC-HVDC (without negative sequence controller)
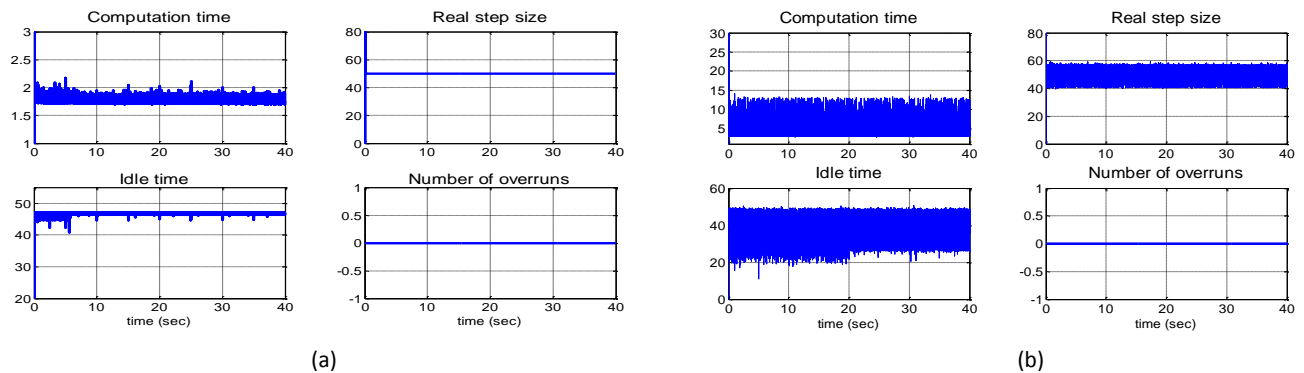
Figure 6.13: OpComm block output (a) for point to point (without neg. seq. controller)   (b) for point to point (with neg. seq. current controller) VSC-HVDC system.

From Figure (6.13) it has been shown that the computation time is very small for case (a) and increases up to around 13 micro seconds for case (b), however computation time for both cases are small from the real step size, therefor no overruns occurs during the real time simulation.

Figure 6.14: OpComm block output (a) for four point (topology-1) (b) for four point (topology-2) VSC-HVDC system.

The computation time for both topologies are almost same shown in Figure (6.14), which are also smaller than the step size as a result no overrun occurs during the real time simulation.

Chapter 7: Conclusion and future work

7.1. Conclusion

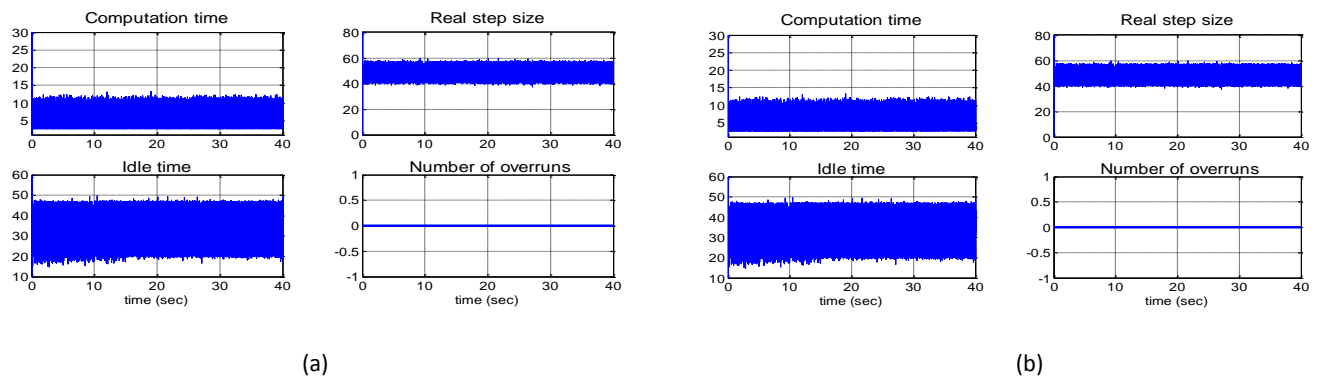The main objective of this thesis was to develop higher level generic control model for the VSC-HVDC system. Furthermore the point to point and four points test systems have been built in the Simulink and transfer all the Simulink models in to the real time simulator. Both offline i.e. simulation in Simulink and real time simulations were accomplished with several test cases.

This report was organized into seven chapters; an overview of all of the chapters will be described in the following part of this section.

In the first chapter the motivation behind the thesis work is defined based on the benefits of using voltage source converter in the dc grid system comparison to the conventional line commuted converter and the importance of the available generic control model for the research works to improve the HVDC technology. Besides, the contribution and outline of the thesis are also described in this chapter.

Different arrangements, basic elements and operating principle of VSC-HVDC system are discussed in the second chapter. The control systems are elaborately discussed with the mathematical models and block diagram in third chapter. Fourth chapter represents the improvement of the controller model. One of the improvements is active damping of dc voltage during unbalanced fault condition by implementing damping conductance as a feed forward term to the dc voltage controller. The other one is negative sequence current control, as it appears during unbalanced fault in the ac side of the system. In order to control the negative sequence currents, the separation of positive and negative sequence current components is required. Therefore two current components are controlled in the two different inner current control blocks, and by setting the negative sequence current references at zero value negative sequence current components can be suppressed. Finally dc voltage droop controller is developed for the four terminals VSC-HVDC system to facilitate the active power sharing between the terminals. It also improves the system responses during the loss of any converter station during operation.

In chapter five all of the controllers are tuned with the trial and error method. To tune the controllers, step changes are implemented and the gain values of PI controllers are selected based on the minimum overshoot and settling time of the steady state response. Offline simulation results for both point to point and four terminals VSC-HVDC system which are

carried out in the Simulink are shown in this chapter. In addition the real simulation results for both point to point and four terminals VSC-HVDC system are depicted in chapter six.

Based on the offline simulation results, following conclusions can be drawn;

- The response of the active power, reactive power and dc voltage controller are fast and accurate i.e. they follow the step changes accordingly.
- Active power and dc voltage are controlled independently.
- Controller recovers the system parameters to the steady sate quickly after clearing the faults.
- With the implementation of damping effect on dc voltage controller, the improvement of the dc voltage during fault is less.
- With the negative sequence current controller the improvement of the active power and dc voltage during unbalanced fault is significant.
- With the dc voltage droop controller, equal active power consumption is observed between the inverter sides in case of the reduction of power flow provides from the rectifier sides.
- With the dc voltage droop controller, multi-terminal VSC-HVDC system performance improves in case of the converter loss.
- In the real time simulation all of the controller performances are fast and accurate.
- The controller responses in real time simulation are similar to the offline simulation.

7.2. Future work

- Implementation of ac voltage controller to the voltage source converter station, this is preferable in case of the VSC-HVDC connection with very weak ac system [1].
- Connect VSC-HVDC link in to large ac system and analyze the improvement of the voltage stability of the ac system.
- Improve the control system by implementing power synchronization control for connecting VSC-HVDC with weak ac system.

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A.1. DQ Transformation

Three phase voltage or current space vectors transformation to *dq* synchronous rotating frame simplify the decoupled control of active and reactive power flows [14].

Considering balanced three phase system, voltage or current equation can be written as [14]

$$X_a + X_b + X_c = 0 \tag{A.1}$$

Where, X is phase voltage or current space vector quantity.

Transformation of stationary *abc* to stationary *αβ* frame is known as Clark transformation. Therefore the equation will be, [14]

$$X_{\alpha\beta} = X_\alpha + jX_\beta = K[X_a + X_b e^{\frac{2\pi}{3}} + X_c e^{\frac{4\pi}{3}}] \tag{A.2}$$

Where, *K* is a constant value

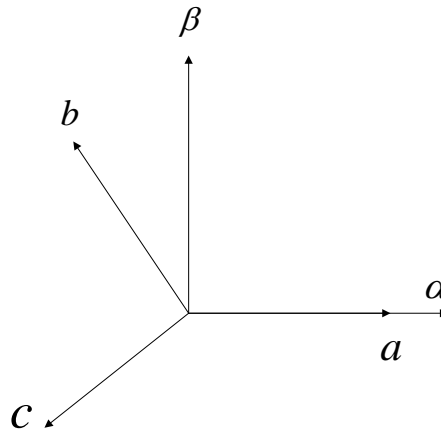Following figure represents *abc* and *dq* reference frames

Figure A.1: *abc* and *dq* reference frames.

Matrix form of the Clark transformation can be stated as [14]

$$\begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = K \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{A.3}$$

Now, stationary $\alpha\beta$ frame to rotating dq frame transformation can be obtained by the Park transformation, i.e. [14]

$$X_{dq} = X_{\alpha\beta}e^{-j\theta} \qquad\qquad (A.4)$$

Matrix form of the Park transformation can be written as [14]

$$\begin{bmatrix} X_d \\ X_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} \qquad\qquad (A.5)$$
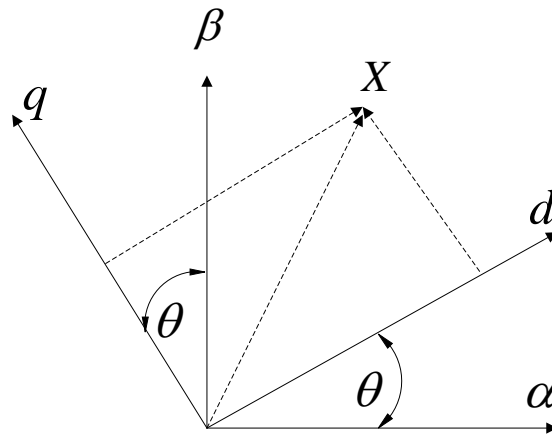

Figure A.2: dq and αβ reference frames.

Where, θ is the transformation angle also can be written as , and ω is the angular frequency of the AC system [14].

Inverse transformation is also required to transform dq to $\alpha\beta$ and $\alpha\beta$ to abc space vector quantities. Equation (A.6) and (A.7) is used to transform dq to $\alpha\beta$ and $\alpha\beta$ to abc respectively.

$$\begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} X_d \\ X_q \end{bmatrix} \qquad\qquad (A.6)$$

$$\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} = K \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & -\frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} \qquad\qquad (A.7)$$

A.2. PI Controller tuning parameters

Table A.1: Tuning parameters for point to point VSC-HVDC.

Parameter	Value
Vdc_Kp	15
Vdc_Ki	300
P_Ki	10
udc_Kp	10
udc_Ki	3
Q_Ki	15
Uf_Kp	0.1
Uf_Ki	0.1
I_Kp	0.4
I_Ki	85

Table A.2: Tuning parameters for 4 terminals [with droop, topology-1, 2(a)] VSC-HVDC.

Parameter	Value
Vdc_Kp	15
Vdc_Ki	200
P_Ki	15
udc_Kp	10
udc_Ki	3
Q_Ki	15
Uf_Kp	0.1
Uf_Ki	0.1
I_Kp	10
I_Ki	85

Table A.3: Tuning parameters for 4-terminals [with droop, topology-1, 2(b)] VSC-HVDC.

Parameter	Value
Vdc_Kp	20
Vdc_Ki	300
P_Ki	55
udc_Kp	1
udc_Ki	0.1
Q_Ki	15
Uf_Kp	0.1
Uf_Ki	0.1
I_Kp	0.4
I_Ki	85

Where, Vdc_Kp,Vdc_Ki are dc voltage controller proportional and integral gain, P_Ki is active power controller integral gain,udc_Kp and udc_Ki are dc voltage override controller proportional and integral gain, Q_Ki is reactive power controller integral gain, Uf_Kp and Uf_Ki are ac voltage override controller proportional and integral gain, I_Kp and I_Ki are the inner current controller proportional and integral gain respectively.