Real-Time Implementation of an Automatic Voltage Stabilizer for HVDC Control

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***Abstract*—Classic HVDC systems are prone to voltage instability when operating on weak AC grids. This paper describes the implementation of a newly developed Automatic Voltage Stabilizer (AVS) in an existing CIGRÉ Benchmark Model for HVDC Controls and compares its performance with the Voltage Dependent Current Order Limitation (VDCOL) method. The tools used for the study are the eMegaSim OPAL-RT real-time simulator and the PSCAD/EMTDC digital simulator. With AVS, the power transfer can be optimized and kept at or close to the steady state stability limit thereby compensating for deficiencies of VDCOL. Using two different simulation environments provides important information on their capabilities to develop and improve future power system controls.**

***Index Terms*—Classic HVDC, VDCOL, Automatic Voltage Stabilizer, Real-Time Simulation**

I. Introduction

CLASSIC HVDC systems are prone to steady state voltage instability when at least one of the AC grids that converters are connected to is weak or the grid becomes weak through certain causes, e.g., switching off AC lines or reactive power supply limitations. The short circuit power ratio in relation to the DC power to be transferred, the SCR, is a crucial quantity [1]. Values around 2.5 are considered as being weak but still possible to cope with. Since the capacitors of filter and capacitor banks determine to a high degree the stability they can be included in the SCR value by forming an equivalent SCR, the ESCR [2]. But aside of such considerations the real challenge is to apply available and to develop further analytical methods to define stability conditions and limits under inclusion of controls. This paper provides background information either directly or through references on the state of art to recognize and mitigate stability problems and it includes a newly developed method which for the first time is compared regarding performance with an already established method by using two transient simulators one of which is the digital simulator PSCAD/EMTDC and the other one is SimPowerSystems running on a real-time environment (eMegaSim OPAL-RT Simulator). The use of two different types of simulators permits to gather experience with regard to development and setup of main and control circuitry as well as run time duration and features for result evaluation.

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II. Background Information

A. Voltage Collapse in Classic HVDC Systems

The HVDC converter control concept is essential in ensuring voltage stability. DC voltage control is superior to constant extinction angle control [3] but DC voltage control cannot be maintained under all operating conditions. It was analytically shown that a SCR of 2 up to 2.5 relates to constant extinction angle control [3], [4]. In addition to these results related to steady state voltage stability additional means exist to control the HVDC systems under disturbed conditions as they occur, e.g., for AC line faults [5], [6], [7]. The ride through criterion requires continuing operation with the least amount of power reduction and the shortest recovery time. Converter controls permit to implement event triggered control algorithms. It is common practice to sense, e.g., distant breaker trips to perform predetermined stabilizing actions [6], [7], [8]. This is, e.g., applied in the Blackwater HVDC [6], [7] and in the Gezhouba-Shanghai transmission system [8]. Besides this important measure there is the also established voltage dependent current order limitation (VDCOL) [9] which is implemented as AC voltage dependent current order limitation in the PIDC transmission system [10].

Event triggered power order reduction (EVPOR) works reliably if the trigger signal is available for all probable events and a look-up table is provided in the engineering phase relating the permissible power order to switching states. However, sufficient high reliability can only be ensured in a radial system while a meshed grid will be too complex to incorporate all forthcoming grid changes. With regards to the second measure (VDCOL) which reduces the DC current order in response to decreasing AC or DC voltage, the problem lies in the difficulty to choose a suitable characteristic to reduce the DC current at a varying short circuit power ratio. An AC grid with a normally high ratio requires a different characteristic when the ratio goes down. However, there is no automatic adaption, voltage instabilities may occur.

Besides EVPOR and VDCOL there are possibilities to improve voltage stability by using additional equipment as the thyristor controlled reactor plus fixed capacitor (TCR+FC) and the static var compensator (SVC) which was in recent times realized through line commutated converters operating with zero DC voltage, i.e. short circuited DC side, but are now being replaced through the static compensator (STATCOM) utilizing the voltage sourced converter (VSC). For the systems and control engineers it is very essential to understand the reactive power/voltage behavior of a compound system consisting of Classic HVDC and reactive power compensating equipment. Due to discontinuous characteristics the system

can suddenly change from stable to unstable [3]. This can also happen when continuously controlled equipment like STATCOM and TCR+FC is utilized. Then EVPOR and VDCOL are up to now the only methods to avoid voltage collapse at detrimental conditions.

Although there was a lot of engineering capacity and brain put into the issue to stabilize Classic HVDC systems operating on weak AC grids [11], [12] the idea to remedy the stability problem by an self-adaptive Real-Time/On-Line method was surprisingly only pursued recently leading to the so called Automatic Voltage Stabilizer (AVS) [13], [14]. The method and corresponding apparatus is different from the available solutions since it is directly directed towards recognizing an impending voltage collapse at operation and takes immediate measures to prevent this. The theoretical base of this work was already laid in [3] and before in [4]. Fundamental for the treatment of steady state stability and to remedy stability problems is to recognize that voltage and transmission angle instability occur simultaneously if the AC terminal of the HVDC converter connected to a weak grid is not continuously controlled. So, there are not two different methods necessary. If the voltage is continuously controlled then there remains still the potential for transmission angle instability and the method can still be applied. The voltage and transmission angle stability problem is, of course, very relevant for Classic HVDC systems, but it is also an issue when the VSC type of HVDC is used. Then, even when voltage can be controlled, i.e. converter rating is sufficient to cover the reactive power need, transmission angle instability is an issue. The AVS is based on an on-line steady state stability analysis using a dynamic stability limit detection method [13]. The PV-characteristic in Fig. 1 provides information about a generic AC transmission system with regards to voltage instability.

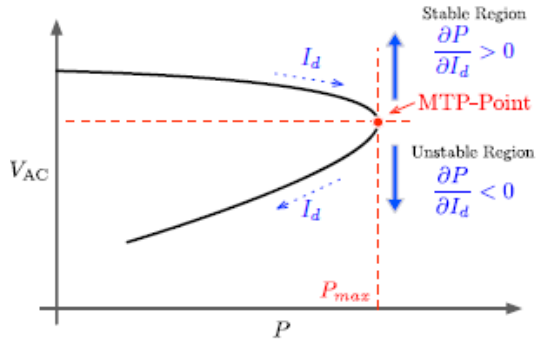


Fig. 1. PV-Curve and stability limit detection method

The uncontrolled AC voltage (V_{AC}) is at the receiving end of an AC transmission system. The voltage declines with increasing power up to the maximum transferable power (MTP) level, once the MTP-Point has been reached, it will decline with decreasing power. In general, this PV-curve holds also for an HVDC system being connected to an AC grid of moderate stiffness [1]. For the current control loop the upper branch is stable and the lower branch is unstable. On the upper branch DC current rises in proportion to the ordered DC power. If the MTP-Point is surpassed, the DC current continues to grow but the DC power declines. The conventional HVDC power controller is not able to detect this change, and the AC terminal voltage starts to collapse. The collapse can be halted through VDCOL. VDCOL does, however, not recognize if the system has already passed the stability border and that it is operating on the lower branch of the PV-curve. Besides voltage depression and efficiency deterioration this mode of operation has some other disadvantages as it became clear through theoretical analysis and preliminary PSCAD/EMTDC simulations using an own HVDC model. The results are summarized under Section II-B.

B. Possible VDCOL Problems

1) Asynchronous machines, thermostatic loads and distribution transformers —: With decreasing AC voltage, the operating point on the torque-slip characteristic of an asynchronous machine might move toward the critical slip value. It consequently increases the machine current which leads to voltage collapse and machine stalling when the VDCOL function is not able to limit the DC current increase on the upper branch of the PV-curve. A similar problem exists in connection with thermostatic loads and distribution transformers controlling consumer voltage via on-load tap changers.

2) Synchronous Generators —: If VDCOL does not stop the HVDC system from moving towards the lower PV-curve branch, electromechanical instability may arise. At the end of the present work such conditions were also studied. The results are not yet included in this article but commented on in Section V. Particularly in parallel AC/DC transmission systems the interaction between AC and DC is very crucial and VDCOL functioning and calibration need to be investigated. In [12] the necessity to study steady state characteristics to understand transient phenomena of parallel systems and to find remedial measures is stressed. Today's transient HVDC performance and control calibration needs are directly determined on a transient simulator, sometimes without preceding static stability investigations [9]. For strong AC grids this should not be a problem. However, this approach is insufficient for weak grids, as described later in this paper.

3) Calibration —: Calibrating VDCOL for a relatively strong system will not suffice when the system becomes weak in a non-anticipated way. Calibrating for a weak system and operating on a strong one will lead to unnecessary power curtailment.

4) Controls —: The gain of the controlled converter station is negative on the lower branch of the PV-curve. This does not permit stable DC power control.

The Automatic Voltage Stabilizer (AVS) [13], [14], which is described in Section III-B, does not experience the problems mentioned above. This is shown through various investigations, starting with building the model in Section III and model validation and comparative simulation results in Section IV. Comparison refers to VDCOL versus AVS performance on the one hand, and PSCAD versus OPAL-RT simulations on the other hand.

C. Benefits of Real-Time Simulation

The PSCAD digital simulator permits the set-up and simulation of truly complex power systems including power semiconductor equipment and necessary controls. The simulation time increases in proportion to configuration size and depends on the specific equipment needed. While for the

comparison study in this article PSCAD is sufficient, additional circuitry can from a certain amount on increase computation time to unacceptable values. Further studies that consider the enhancement of the AC network model and the study of three-terminal HVDC systems are planned. Thus, it is expedient to simulate the AVS with a real-time simulator (eMegaSim OPAL-RT simulator) and to get acquainted with its real-time features before considering more complex configurations. Both the PSCAD digital simulator and the eMegaSim OPAL-RT simulator contain an implementation of the CIGRÉ Benchmark Model for HVDC Controls, including the VDCOL function.

The main tasks of this work are the implementation and verification of the automatic voltage stabilizer for both simulators and the performance evaluation of the VDCOL function. Compared to analog simulators, digital Real-Time simulators use samples of the various system quantities and determine the next output of these quantities through some solution algorithm using previous outputs, previous inputs and the actual inputs. Due to the sampling period which has to cover the processing time of the samples as well as the time it needs to have the inputs stored in the computer memory and the outputs sent to actuators the notion of RT is relative. The predetermined time step used in our simulations is 50 μs, which allows us to sample up to 20 data points on a 1 kHz signal. With regard to firing signal generation and controls this is sufficient but regarding the exact determination of, e.g., lightning surges having a rise time of 1.2 μs this would not be sufficient. Usually, however, insulation coordination is not performed on a RT-simulator but on a Transient Digital Simulator as, e.g., PSCAD/EMTDC.

It has to be noted: a RT simulator permits calculations within any time frame, provided no real-time requirements have to be met. A main reason for using a RT-simulator in the industry is to be able to connect control cubicles and test its hardware and software before shipping to site. In our case the pursued RT simulation permitted to implement in a reasonable time frame a new stabilization method and to prepare a possible connection of real-time controls containing the stabilizer algorithm. Thus the results obtained are twofold: First it is possible to operate the HVDC system at or close to the stability boundary without inducing voltage instability which is important in respect to building a smart power system and secondly: Connection points between main circuitry measurements and the controls are identified for later connection and tests of control cubicles.

III. Modelling Needs

A. CIGRÉ Benchmark

The CIGRÉ Benchmark Model for HVDC Controls runs on a digital computer using an electromagnetic transient program. It permits to investigate steady state and dynamic control performance at weak AC grid conditions.

The model contains a 12 pulse/ 500kVdc/ 1000MW mono-polar long distance transmission system including all necessary filter circuits and capacitor banks to provide proper operating voltage quality (Fig. 2). The grids are formed by static grid equivalents. Implemented in the model is constant extinction angle control but not the transition from DC voltage control to minimum extinction angle control as it is actually installed in DC transmission systems [10]. Therefore, for this study inverter controls were complemented by DC voltage control. The transfer from DC voltage to minimum extinction angle control is a rather problematic point on the power-voltage characteristic of the inverter [13], [15]. In actual systems either the valve side AC voltage or the extinction angle can be controlled via the converter transformer on-load tap changer. This improves stability conditions [15]. However in the CIGRÉ Benchmark Model no tap changer is foreseen and also for the present study no such equipment was added.

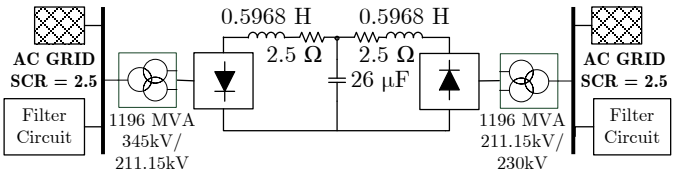


Fig. 2. CIGRÉ Model

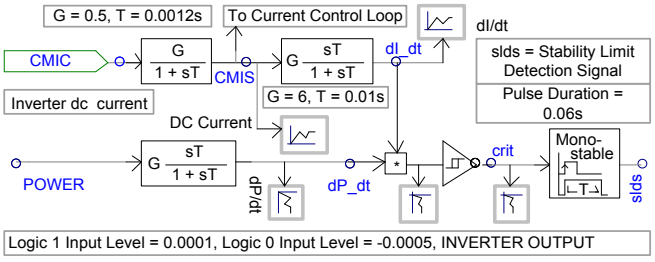
In order to determine the best suitable control solution for given grid conditions it is necessary to understand the coupled power/reactive power/controls relationships which permit to stay within ratings of main and auxiliary equipment and permit at the same time stability. Up to now the overall governing control principle as described in [16], [17] is the marginal current principle which is contained in the CIGRÉ Benchmark Model. Within this principle there is some freedom to exert certain controls as described above. The degree of freedom is known since long and new control concepts will probably mainly be directed towards inclusion of wide area measurements, real-time/online computations of sensitivities [3] and parallel HVDC model simulation in real-time to know the status and probable changes of stability conditions. Important today is to push main equipment to higher rating, e.g., DC operating voltage up to ±800 kVdc as it was achieved recently and to test new circuit related ideas, as, e.g., the capacitor commutated converter and active filter circuits. Multi-terminal Classic HVDC systems will probably be restricted to a minimum number of terminals as, e.g., the PIDC system - where on a bipolar DC line converters operate in parallel - and the three-terminal HVDC Transmission Québec - New England.

It should be of interest to mention here that the VSC type converter has made it easier for academia to participate in controls design and its simulation. There is no such relatively complex requirement as shifting the power control between the converters and marginal current compensation or to cope with the problem of commutations failures. The controls are relatively simple as compared to Classic HVDC controls. It appears presently that dq-control technique gets some preferred attention, but as to the opinion of the authors the interconnections with the AC grid, implementation of virtual inertia and rotor angle stability of mechanical generators operating in parallel to static generation [15] as well as the transmission angle stability receive not sufficient attention, particularly not so in links between weak AC grids and in offshore wind farm connections via HVDC systems where tight construction schedules exist and planned commissioning times have to be met. In view of this it is urgent to define a

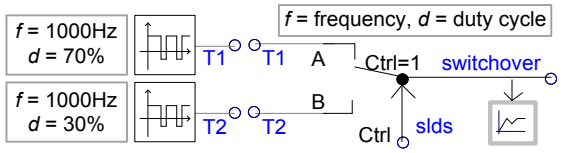
CIGRÉ Benchmark Model for HVDC Controls also for the VSC type HVDC transmission system and to distinguish between different model types according to requirements to be met when participating in overall grid controls.

B. AVS Implementation in PSCAD

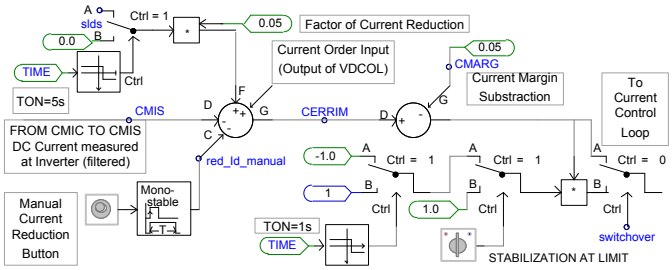
The PV-curve provides analytical means to distinguish between the upper and the lower branch by determining the derivatives of the DC power with respect to the DC current (Fig. 1). Essential for a statement on steady state stability is the sign of the quotient $\partial P/\partial Id$. Since $\partial P/\partial Id$ cannot be measured directly, it is determined by measuring the derivatives $\partial P/\partial t$ and $\partial Id/\partial t$ with respect to time, and forming the product of these derivatives resulting in: $\partial P/\partial t \times \partial Id/\partial t = crit$ (see Fig. 3a).



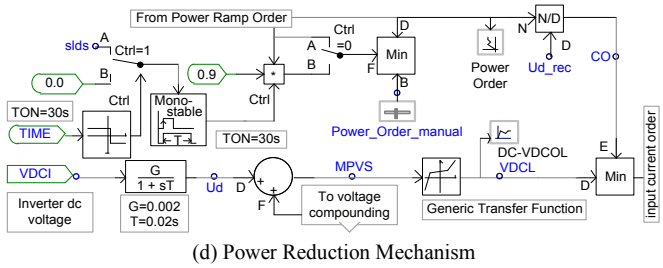
(a) Automatic Voltage Stabilizer (AVS)



(b) Switchover Signal Generation



(c) AVS Implemented in Closed Loop Control



(d) Power Reduction Mechanism

Fig. 3. PSCAD/EMTDC AVS Implementation

If only one of the derivatives with respect to time becomes negative, which indeed occurs when moving along the lower branch of the PV-curve, the product "crit" becomes negative. If both derivatives with respect to time are either positive or negative - which happens when the operating point moves along the upper branch - the product is positive, so we know that the operating point is on the upper branch.

The value of "crit" is passed to a hysteresis buffer that triggers a mono-flop which in turn sets the stability limit detection signal "slds". Fig. 3b illustrates how the "slds" generates a pulsed signal called "switchover" which operates finally the sign reversal switch. Two clock signals, T1 and T2, are embedded in the circuit. With T1 the operating point is pushed back up, with T2 it falls back to the lower branch. The displayed principle ensures a safe oscillation around the MTP-Point. Fig. 3c depicts the effect of the switchover signal. The two time-based switches can be disregarded. They are necessary to power up the system to nominal conditions without AVS control.

If the AVS is switched on ("Stabilization at Limit" in upper position), the feedback sign of the closed-loop current controller is switched between plus and minus depending on the switchover signal. A negative sign will change the current from increase to decrease. This leads the operating point back to the upper branch and then, since the "crit" value becomes positive, the sign is switched back to positive. In this way the operating point will revolve around the stability boundary. Instead of bounding the operating point around the stability border, the power order can automatically be reduced at the first occurrence of the stability limit detection signal (slds) (Fig. 3d). This signal triggers a mono-flop that in turn operates a switch which reduces the power order by a defined value. In [14] this is a value adapting itself to the MTP level, but this value is fixed for the test purpose in this paper.

Fig. 3d shows that VDCOL is DC based. This is indeed a limitation due to the fact that the AC voltage declines always earlier than the DC voltage [15]. However, for a weak AC grid with an SCR of around two there is only a very small AC voltage decline before the voltage collapses. That is, the difference whether using AC VDCOL or DC VDCOL is only marginal and not decisive for the functioning and the performance of VDCOL at weak grid conditions. If needed the change to AC voltage dependent VDCOL can be easily implemented.

C. Real-Time AVS Model Implementation

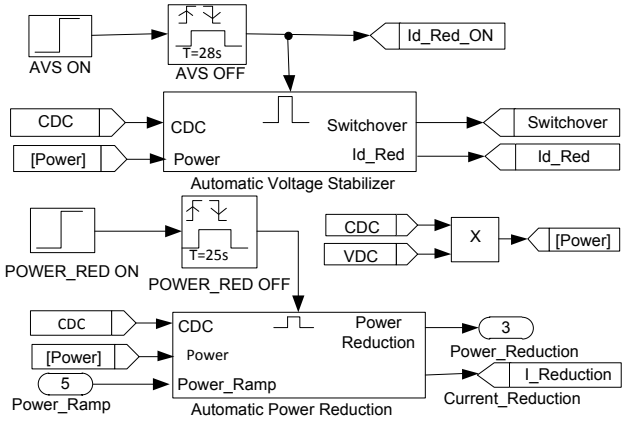
The AVS was implemented within the inverter control subsystem of the original model. Fig. 4a depicts the details of the AVS which was embedded. The measured DC current (CDC) and DC voltage (VDC) are multiplied to get the power transmitted over the DC link. The subsystems for the stabilizer (Fig. 4a and 4b) and the automatic power reducer (Fig. 4c) are equipped with a switch to set them active or inactive. The stabilizer is switched on after 35 seconds and stays active for 30 seconds, while the automatic power reducer is switched on at 67 seconds and remains active for 28 seconds. When the stabilizer is switched on, the "Id_Red_ON" function is set on too.

To avoid an operation at the stability boundary with the accompanying swings around the MTP point a power order reduction triggered by the aforementioned "slds" signal is necessary. The power reduction order has to appear when the operating point is on the upper branch. This is achieved by simultaneously issuing a current order reduction pulse.

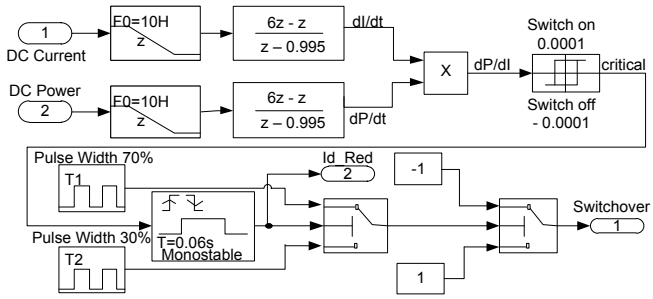
IV. Comparative Simulations

A. VDCOL Characteristics

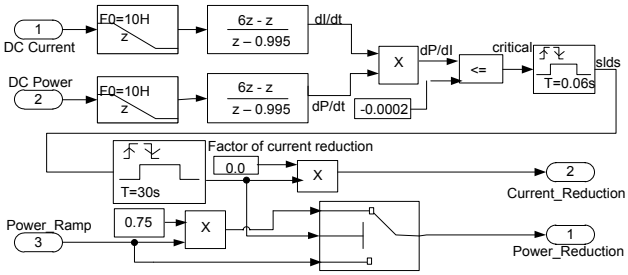
Weak grid here means that the internal reactance of the grid is set to a value resulting in a short circuit power ratio (SCR) of 1.9 at an internal AC grid voltage of 380 kV. It is assumed



(a) AVS Implementation



(b) AVS Stabilizer Subsystem

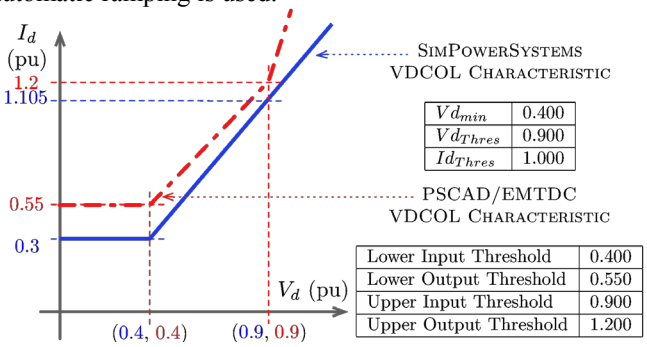


(c) Power Reduction Subsystem

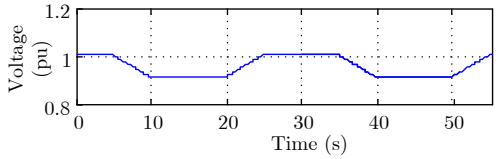
Fig. 4. AVS Implementation for Real-Time Simulation

that this SCR value results from a structural change with a SCR value of 3.33 before this change. For normally available SCR = 3.33 there is a protection against voltage collapse and at the same time, there is no unnecessary power curtailment if the voltage declines within the normal voltage band. If, however, the SCR changes due to a non-foreseeable and non-detectable event reducing the SCR value to below 3.33, e.g., to 1.9, then the calibration of the VDCOL characteristic is no longer appropriate and this is shown in this study.

The characteristic permits DC current overload of 1.2 at 0.9 p.u. DC voltage holding for the characteristic implemented in PSCAD controls. This is either a temporary overload or can even be continuous overload depending on the prevailing ambient temperature. The parameters given in Fig. 5a show that the VDCOL calibration values differ between PSCAD and SimPowerSystems (SPS) and accordingly the VDCOL characteristics are somewhat different as also depicted in Fig. 5a. Fig. 5b shows a controlled variation of the internal grid voltage to test the behavior of VDCOL, AVS and the AVS with automatic power reduction in the listed order. In PSCAD simulation the variation of the internal grid voltage can be accomplished manually or via an automatic ramp. Manual ramping is not possible with SPS due to time lags between the monitoring console and the real-time target, automatic ramping is used.



(a) VDCOL Characteristics

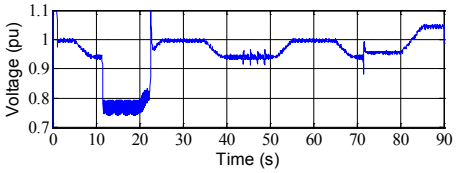


(b) Internal Grid Voltage – SPS

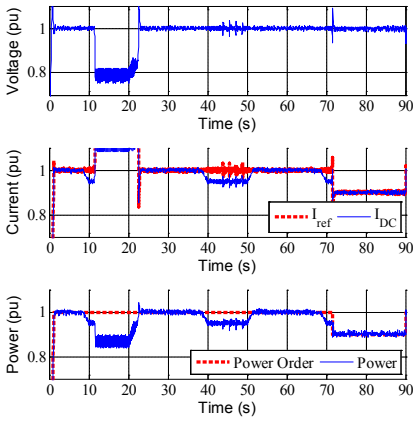
Fig. 5. VDCOL Characteristics and Internal Grid Voltage

B. Weak AC Grid on Rectifier Side

In this scenario the SCR at the Rectifier is 1.9 while the SCR at the Inverter is 2.5. Fig. 6a shows the response of the AC terminal voltage of the rectifier as a result of a variation of the internal grid voltage as shown in Fig. 5b.



(a) AC Terminal Voltage at the Rectifier

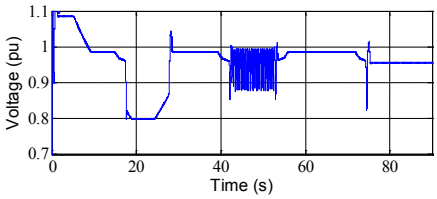


(b) Rectifier Oscillograms

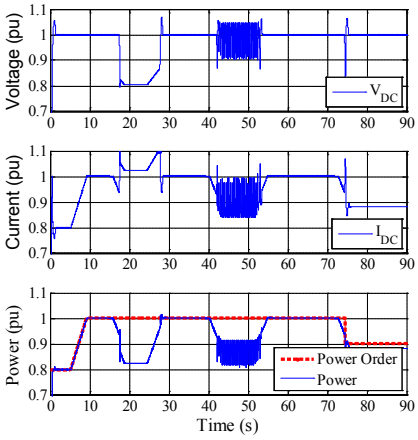
Fig. 6. Weak AC Grid on Rectifier Side - SPS Results

Only the VDCOL is activated during time 10-20 sec, which makes the voltage drop to somewhat above 0.8 p.u. The AVS is activated between 40-50 sec, which retains the voltage level around 0.9 p.u. The AVS with automatic power reduction is activated at time 70-80 sec. The ac voltage is kept above 0.9 p.u. Fig. 6b illustrates the comparison of the DC quantities for the three different control methods.

It is clear that without AVS, the operating point at VDCOL operation slides to the lower branch of the PV-curve. The operation of AVS without the power order reduction yields stable swings around stability limit and this swing can be removed by applying the automatic power order reduction. Fig. 7a and 7b depict the similar test on the PSCAD digital simulator. According to Fig. 6a to 7b the AVS implementation on both simulators provide similar responses. While the oscillating operating point will not be acceptable for a longer time it provides the proof that the system is actually kept around the stability boundary. Setting the power order to a lower value as soon as these swings occur, either manually or automatically, yields a stable system.



(a) AC Terminal Voltage



(b) Rectifier Oscillograms

Fig. 7. Weak AC Grid on Rectifier Side - PSCAD Results

C. Weak AC Grid on Inverter Side

The internal grid voltage shown in Fig. 5b is applied at the inverter. The SCR values are each 2.5 at the rectifier and the inverter. In this scenario only VDCOL and AVS with the automatic power reduction are tested. Only the VDCOL is activated during time 10-20 sec, the commutation failure occurs as shown in Fig. 8. In contrast to VDCOL, the operation of AVS, at time 40-50s, results to only a voltage dip and prevents the commutation failures. Similar simulation results were obtained from the PSCAD simulation not shown here.

D. Performance with embedded Asynchronous Machine

In this scenario the SCR at the rectifier is set to 1.9 while the SCR at the inverter is set to 3.3. In contrast to the previous scenarios, the DC power is decreased to 0.8 p.u (taking into account the demand of an asynchronous machine). The total power transfer on the AC line before the test is approximately the same level as in the previous scenarios. The AC terminal voltage of the rectifier shows a steep decline with solely VDCOL in operation (t = 10-30 sec), dropping to 0.6 p.u. (Fig. 9a). This low voltage level caused by the reactive power demand of the asynchronous machine is pulling the AC voltage further down. In real operation this would be prevented by tripping the machines but it has to be recognized that before this happens the *Vac* versus *Q* behavior of both the machines and the converter station determine in combination the slide towards the lower branch of the PV-curve and the converter might have already surpassed the nose of the PV-curve before the machines trip.

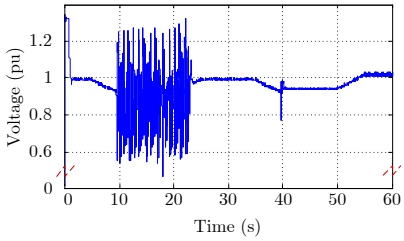
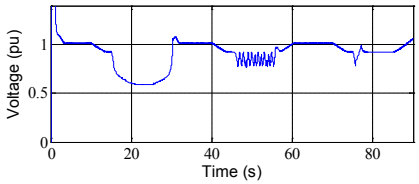
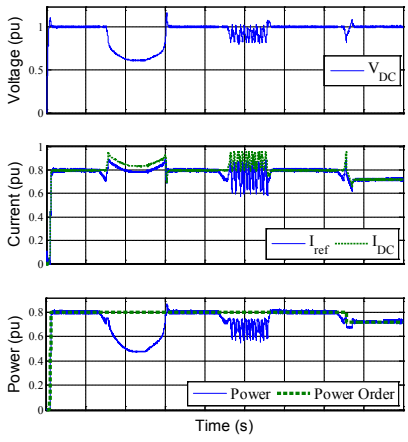


Fig. 8. AC Terminal Voltage Inverter - SPS

Fig. 9b shows that DC power decreases despite the DC current increase, this is a clear indication that the MTP-Point is surpassed. As in the previous test, the AVS and the AVS with the automatic power reduction are applied at time 40-60 sec and 70-90 sec, respectively, where both of them prevent system collapse.



(a) AC Terminal Voltage at the Rectifier

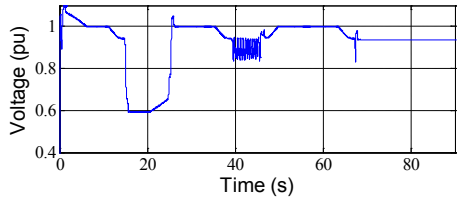


(b) Rectifier Oscillograms

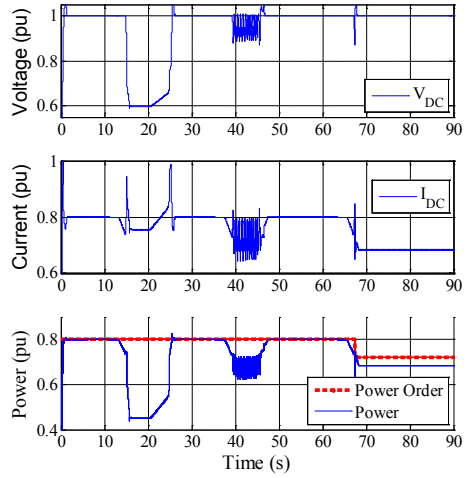
Fig. 9. Performance with Asynchronous Machine – SPS

Fig. 10a to 10b illustrate the similar response obtained from the PSCAD digital simulator. Fig. 11 shows the response of the asynchronous machine. VDCOL cannot stop the AC grid voltage decline. The asynchronous machine is sent over the pullout slip causing further voltage decrease. AVS prevents

this phenomenon either by keeping the operating point revolving around the maximum power point or by applying automatic power order reduction. Also here either manual reduction of the power set value or the implemented automatic power order reduction avoids swings around the MTP-level.



(a) AC Terminal Voltage at the Rectifier



(b) Rectifier Oscillograms

Fig. 10. Performance with Asynchronous Machine – PSCAD

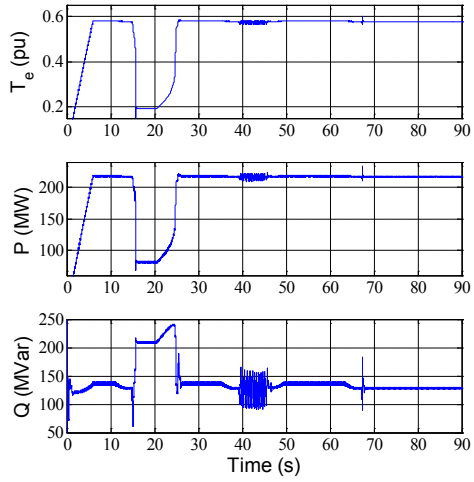


Fig. 11. PSCAD Oscillograms Asynchronous Machine

V. Conclusions

Classic HVDC systems operating in weak environments can be protected from voltage instability by performing Real-Time/On-Line stability analysis in parallel and in synchronism with the running power system and by using the outcome of the analysis to influence the HVDC power controller such that the power is kept at or close to the maximum transferrable power level. Real-Time/On-Line stability limit detection and ensuing stabilization are the two elements of the Automatic Voltage Stabilizer (AVS) which in a special form is complemented by Automatic Power Order Reduction (APOR) to provide a defined distance from the steady state stability boundary.

As compared to the state of the art which uses Voltage Dependent Current Order Limitation (VDCOL) the proposed method of AVS and APOR provide stable operation also at very detrimental conditions where the short circuit power ratio of the system changes between low and very low. It could be shown that there is no unique calibration of the VDCOL function fitting to different values of the systems short circuit power ratio. This can lead to a shift of the operating point to the lower branch of the voltage/power curve of the system. This means efficiency reduction due to low DC voltage and high DC current. In addition with the AC voltage being pulled down induction machines will go over the pullout slip and then the system voltage would totally collapse if the machines would not be switched off in due time. However, if switched off consumers would be affected dramatically.

The AVS/APOR functions remedy the problem by keeping the AC and DC voltage on a higher level and DC current on a lower level. Efficiency is higher and induction machine pullout is prevented, i.e. operation continues on a lower but stable HVDC power transfer level.

After conclusion of the work pertaining to this report the static grid on the rectifier side was replaced by an AC transmission system with synchronous generators at both ends. The system working with VDCOL only showed swings in the region of several Hz which were attributed to limit cycling of HVDC controls but the system could be stabilized with the AVS/APOR function.

Both the PSCAD and the Opal-RT simulator using SPS produced equal results. Since the first steps of implementation were always done on PSCAD there was already experience of equipment and controls interaction available before going to the RT-simulator. In PSCAD, since the run time was less than 100 sec and the computation time was about 4 min, it was not that much of a problem to wait for results, particularly not so since during the run certain ramps were initiated or performed manually working as an operator which means that the time to do this was anyway needed. A too fast run would have prevented an analysis and an immediate reaction during the run. Such test actuations are also possible in SimPowerSystems and they were accordingly implemented and actuated through certain predetermined control sequences.

Further investigations on expanded systems not belonging to the present topic and not reported here needed very long simulation times going over an hour with PSCAD. Such systems need real-time simulation not to waste the time of engineers sitting to wait for results which very often, in the beginning of set-ups and implementations are not that what is expected with the consequence of additional runs.

The conclusion is: To develop a certain size of converter and transmission main circuitry and to add internal and external controls is possible without real-time simulation. But from a certain point on there is no alternative in these days where real-time simulation equipment is on the market. What should be considered besides run time is the easiness of building, testing and changing circuits and configurations in the development stages. If once a circuit runs and is tested regarding its behavior under different grid and operating conditions it is relatively simple to implement more measuring

devices, to correlate results mathematically and graphically and to display more information.

VI. Further Work

The next steps planned for is the application of the automatic voltage stabilizer to the VSC type of HVDC transmission system connecting weak AC grids. Already available results show the viability of the AVS for transmission angle stabilization. Transmission angle stability is of significance for our electric power systems being under continued development and construction in the years to come.

Phasor Measurements Units used in Wide Area Measurements Systems can be used to support stable operation but as to recent study results they do not provide complete security since threshold values of angles where instability occurs show a high degree of uncertainty [18]. AVS/APOR closes this gap by becoming active if WAMS fails to recognize an impending stability problem. First results show that onshore AC transmission capacity can be utilized up to the static stability limit when power from offshore wind farms is injected via HVDC transmission systems. Also storage devices of relatively low energy capacity can operate in connection with the AVS and relieve the wind farm turbines from mechanical stress at AC line trips. Studies on this will include participation of offshore wind farms in automatic load frequency control under provision of virtual inertia implemented in the HVDC inverter feeding the onshore AC grid.

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VIII. Biographies

Kim Weyrich was born in Traben-Trarbach, Germany, on February 6, 1984. He was trained as an electrician for industrial Engineering from 2004 to 2008 at Papier-Mettler GmbH in Rhineland-Palatinate. After he studied electrical engineering at the University of Applied Science Frankfurt am Main, receiving B.Eng. degree in 2011 in cooperation with KTH Royal Institute of Technology Stockholm, Sweden, he became a research assistant at the University of Applied Science Frankfurt am Main, with main focus on electrical power system simulation. Since 2012 he is with REpower Systems SE in Germany working on Grid Integration of Offshore Wind Farms.

Rujiroj Leelaruji received the B.Sc. degree in electrical engineering from Sirindhorn International Institute of Technology (SIIT), Thailand, in 2004, and the M.Sc. degree in electric power engineering from KTH Royal Institute of Technology, Stockholm, Sweden, in 2007. He is currently a Ph.D. student within the Electric Power Systems (EPS) Division at KTH. His research focuses on the development and implementation of an algorithm for coordinating system protections and HVDC/FACTS controllers that can result in preventive measures mitigating voltage instabilities.

Walter Kuehn (M'1997) was born in Autenried in Germany on April 3, 1945. He studied Electrical Engineering at the FH Dortmund University of Applied Sciences and at the RWTH Aachen University in Germany, receiving the Dipl.-Ing. (FH) and the.Dipl.-Ing. (Univ) degree. After a fellowship at Stanford University where he started his doctoral thesis he joined the Institute of EE and Automation at the RWTH Aachen University. He wrote his dissertation on control and stability of a hybrid transmission system for which he was awarded the Dr.-Ing. degree by RWTH Aachen. His following industrial employment was with ABB working in the HVDC Systems Engineering department. He was HVDC systems engineer and overall technical project manager for several executed projects, amongst them Blackwater Back-to-Back Converter Station and Pacific Intertie HVDC Expansion. His last industrial position up to 1994 was with AREVA in Frankfurt, Germany, managing the network and line construction business.

Today he is a full time professor at the University of Applied Sciences in Frankfurt, Germany. He teaches Engineering and Project Management of Electric Power Systems with emphasis on HVDC transmission technologies.

Luigi Vanfretti (Student Member '03, M'10) became an Assistant Professor at the Electric Power Systems Department at KTH Royal Institute of Technology, Sweden, in 2010 and was conferred the Swedish title of "Docent" in 2012. He received the EE Degree from *Universidad de San Carlos de Guatemala* in June 2005, and was a visiting researcher at The University of Glasgow, Scotland, also in 2005. He received his M.Sc. and Ph.D. in 2007 and 2009, respectively, both in Electric Power Engineering from Rensselaer Polytechnic Institute, Troy, NY, USA. For his research and teaching work towards his Ph.D. he was awarded the *Charles M. Close Award* from Rensselaer Polytechnic Institute.

His main research interest is on the development of PMU data-based applications. He has served, since 2009, in the IEEE PES PSDP Working Group on Power System Dynamic Measurements, where he is now Vice-Chair. In addition, since 2009, he has served as Vice-Chair of the IEEE PES CAMS Task Force on Open Source. He is an evangelist of Free/*Libre* and Open Source Software.