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Integration of Renewable Energy Resources via Classic HVDC

Integration Erneuerbarer Energieerzeugung in das Drehstromnetz über HGÜ

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Frankfurt am Main, den 15.08.2011

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Eidesstattliche Erklärung

Hiermit versichere ich, Kim Peter Weyrich, geb. 06.02.1984 in Traben-Trarbach, die hiermit vorgelegte Bachelorarbeit nur unter Zuhilfenahme der angegebenen Quellen und Hilfsmittel selbständig angefertigt zu haben.

Kim Weyrich

Frankfurt am Main, den 15.08.2011

Foreword

First of all I want to thank Prof. Dr.-Ing. Walter Kühn for the opportunity I was given to work on this project in Frankfurt as well as in Stockholm and for his expertise with which he always helped me with words and deeds.

Further I want to thank Dr. Luigi Vanfretti and Rujiroj Leelaruji for their permanent support during my time in Stockholm.

List of Contents

1 INTRODUCTION/MOTIVATION

1.1 Benefits of AVS compared to VDCOL

Classic HVDC systems are prone to steady state voltage instability when the AC grid is weak or it becomes weak through certain causes like switching off AC lines or reactive power supply limitations. In order to avoid voltage collapse and power loss certain measures are currently taken. These measures are event triggered power order reduction or voltage dependent current order limitation.

The first measure works reliably if the trigger signal is available for all probable events. This can only be ensured in a radial system while a meshed grid will be too complex to incorporate all forthcoming grid changes. With regard to the second measure which reduces the DC current order in response to decreasing AC voltage the problem lies in the difficulty to choose the correct characteristic to reduce the current at varying short circuit power ratio. An AC grid with a normally relatively high ratio requires a different characteristic when the ratio goes down. But there is no automatic adaption possible. And because of this either the power is curtailed unnecessarily or the stability is in danger.

The task arising from these deficiencies was to search for a method and a mechanism which adapts to changing short circuit power ratios and provide stable voltage without unnecessary power curtailment or instability. This task was solved through [I] using the digital simulator PSCAD/EMTDC. The result out of this work is the “Automatic Voltage Stabilizer” which is based on an on-line steady state stability analysis.

The following PV-diagram (Fig. 1) provides information about a generic AC transmission system with regard to a stable or unstable state and the transition between both these states.

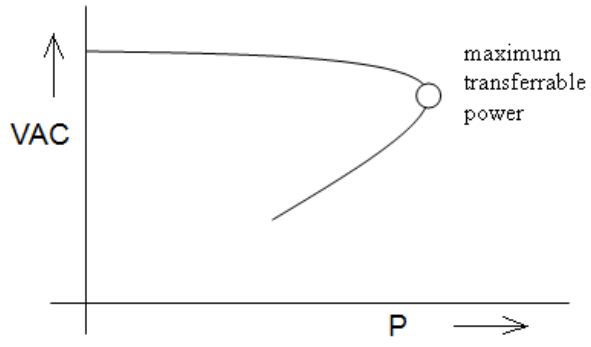


Fig. 1: PV-curve

VAC is the uncontrolled AC voltage (VAC) at the point of common connection. The voltage declines with increasing power up to the maximum transferrable power level (MTP-level) and continues to decline with then decreasing power. This PV-

[I] PCT/EP2010/055076, Method and Apparatus for Automatic Network Stabilization in Electric Power Supply System using at least one Converter

curve holds in principal also for an HVDC transmission system being connected to an AC grid of moderate stiffness. The upper branch is normally stable and the lower branch is unstable (for the normally applied control loop sign).

The maximum power point separates the stable and the unstable regions. On the upper branch the DC current rises in proportion to the DC power. The AC terminal voltage declines in order that the system finds a new state of reactive power equilibrium. When the maximum power point is surpassed the DC current continues to grow but the DC power declines. The AC terminal voltage collapses but the collapse can be halted through voltage dependent DC current order limitation (VDCOL). VDCOL does, however, not recognize that the system has passed the stability border and that the system is operating on the lower branch of the PV-curve.

While this effect of VDCOL is not really satisfying it has to be noted that If DC current limitation through the VDCOL function would not take place at all, a total voltage collapse and power loss of the HVDC system would occur.

With VDCOL the HVDC transmission system is saved to some degree but the influence of the low AC voltage on the rest of the power system can have further detrimental effects. E.g., asynchronous machines either consuming or generating real power (wind turbines) would deteriorate the whole situation.

The problem with hitherto existing investigations on the function and viability of VDCOL is that mostly directly dynamic analysis is performed without a preceding study on steady state voltage stability characteristics and quantitative separation of stable and unstable regions. Such steady state studies are, however, essential to understand instability phenomena as voltage collapse and are at the same time a prerequisite to design controls properly. Such investigations were to the author's best knowledge not performed in [II] when there occurred the blackout of the western power grid in 1996 and is also not conducted in the last available investigation on VDCOL [III]. Already for HVDC stations built about 30 years ago such steady state stability studies were done and they were necessary in order to provide stable operation at weak AC grids. Blackwater HVDC Back-to-Back Tie is an example for the application of the voltage sensitivity factor (VSF) which furnished the necessary information at design stage on the measures to be implemented in converter controls [IV].

[II] Richard Bunch, Dimitry Kosterev, Design and Implementation of AC Voltage Dependent Current Order Limiter at Pacific HVDC Intertie, PE-408-PWRD-0-01-1999.
[III] Arunkumar Muthusamy, Selection of Dynamic performance Control Parameters for Classic HVDC in PSS/E , Master of Science Thesis, Chalmers University of Technology, Gothenburg, 2010.
[IV] Hammad, A., Kuhn, W., A Computation Algorithm for Assessing Voltage Stability at AC/DC Interconnections, IEEE Transactions on Power Systems, Vol. PWRS-1, No. 1, Feb. 1986.

Summary on VDCOL Problems

- **Asynchronous machines and thermostatic loads**
  In pre-investigations we have seen a collapse of the VAC (the grid's AC voltage) when using VDCOL. That means, if the VAC is not high enough for asynchronous machines their demand of current rises critically pulling the voltage further down and the pull out point will be surpassed. Consumer side voltage of transformers is controlled via on-load tap changers of distribution transformers. Declining voltage in the high voltage grid is compensated on the consumer side by change of the transformer ratio. This increases the current on the high voltage side with further detrimental effect on the grid voltage.
- **Synchronous generators**
  After surpassing the MTP point of the PV Curve generators will run away. This occurs because the electrical torque is falling while the mechanical torque is kept constant (the turbine speed controller is too slow to react).
  Particularly when operating with parallel AC/DC transmission systems the interaction between both these systems is very crucial regarding transient stability when VDCOL is not calibrated properly [V], although AC voltage dependent VDCOL was used. Although in the [VI] the necessity to study steady characteristics to understand transient phenomena and to find remedial methods is demonstrated.
- **Calibration**
  Calibrating VDCOL for a relatively strong system (SCR = 3 or higher) does not fit for a system getting weak in a non-predictable way. The system collapses. Calibrating for a weak system (SCR = 2 or lower) and operating on a strong one will lead to unnecessary power curtailment. The above mentioned study on VDCOL [VII] assumed a single SCR value of 3 as actual operating conditions and took accordingly a calibration fitting to this value. That is, cases where the calibration does not fit the actual conditions are not included.
- **Inefficiency**
  The principle of the VDCOL brings along that the operation point can slide uncontrollably to the lower branch of the PV curve. The result is high current and low voltage which is unacceptable for long distance transmission systems.

[V] Richard Bunch, Dmitry Kosterev – Design and implementation of AC Voltage Dependent Current Order Limiter at Pacific HVDC Intertie (PE-408-PWRD-0-01-1999)
[VI] A. E. Hammad, Stability and Control of HVDC and AC Transmissions in Parallel, IEEE Transactions on Power Delivcry, Vol. 14, No. 4, Octobcr 1999
[VII] Arunkumar Muthusamy, Selection of Dynamic performance Control Parameters for Classic HVDC in PSS/E , Master of Science Thesis, Chalmers University of Technology, Göteborg 2010

- **Controls**
  The gain of the controlled converter station is negative on the lower branch of the PV-curve. Electromechanical swings are excited. And power modulation as it is sometimes used (e.g., in Pacific HVDC Intertie) would act into the wrong direction.

AVS Benefit

The AVS (automatic voltage stabilizer) [VIII] does not experience the problems discussed above. The theoretical assumptions were proved through some preceding tests on a rudimentary self-built HVDC system before continuing with a Benchmark model.

1.2 Why important to model and compare VDCOL and AVS in RT? What are the benefits?

First the question regarding “Real-Time” has to be answered.

What is Real-time? Press the switch and the light bulb turns on, would probably be the best illustration. We recognize the light at the same time as we switch on the bulb. Looking closer at it we would notice that there are delays having do with the mechanical speed of the switch, speed of light and, of course, processing time of our eye and brain.

Real-time has to do with the time range within which we want to determine the output of a process given a certain input.

Compared to analog simulators, digital RT simulators use samples of the various system quantities and determine the next output of these quantities through some solution algorithm using previous outputs, previous inputs and the actual inputs. Due to the sample time which has to cover the processing time of the samples as well as the time it needs to have the inputs stored in the computer memory and the outputs sent to the measuring terminals the notion of RT is relative. The pre-determined time step used in our simulations is 50μs, which allows us to sample up to 20 data points on a 1 KHz signal. With regard to firing signal generation and controls this is sufficient but regarding the exact determination of, e.g., steep front surges this would not be sufficient. Then the sample time has to be decreased.

RT simulation is used to test and verify systems that do not exist yet. In this way control cubicles delivered to site can be directly connected and commissioned

VIII - PCT/EP2010/055076, Method and Apparatus for Automatic Network Stabilization in Electric Power Supply System using at least one Converter;
- Control and Stability of Power Inverters Feeding Renewable Power to Weak AC Grids with No or Low Mechanical Inertia, Kuehn, W.;
- Real-Time Method to Prevent Voltage Collapse and Power Instability of HVDC Systems, Kuehn, W.

without changes in coding. The main reason for this method is eliminating errors in control and protection before they occur in a physically established system.

The real-time simulation performed in this work shall repeat and prove in the first step the results already obtained with the PSCAD/EMTDC digital simulator as a starting basis for further specific work. The intention is to take over the already existing AVS system from PSCAD and then to extend the surrounding power system to test further scenarios that would exceed the engine power of the digital PSCAD/EMTDC simulator.

The following steps shall be taken to verify the operation of the AVS controller on the OPAL-RT-Simulator.

- Repeat and prove the tests already realized with the PSCAD simulation environment.
- Add asynchronous machines to demonstrate their effect on stability in connection with the HVDC system operating on a weak grid (both for rectifier and for inverter). Interactions between AC grid voltage, HVDC and asynchronous loads shall be investigated and understood. From the preceding PSCAD/EMTDC studies it is known that decreasing AC voltage increases the reactive current of asynchronous machines pulling the voltage further down despite VDCOL being actuated. AVS prevents that collapse.
- Instead of the static voltage source, a synchronous generator shall be implemented. Investigation shall focus on the case where the maximum transferrable power point (MTP) is surpassed. Also here it is already known from the preceding PSCAD/EMTDC simulations that VDCOL is not able to prevent splitting apart two generators forming a two area system where one area is connected to HVDC. This scenario shall be sub divided into the case of a constant mechanical power order without a speed governor and another case including a speed governor.
- Implement a specific MATLAB code for the determination of the stability criterion. Use the continuously determined stability margin to set the power on-line.
- Investigate the performance of the AVS controller in multi-machine power systems and multi-terminal HVDC systems.

As became clear in the course of this work not all of these tasks could be processed. This was not unforeseeable due to dealing with a new simulator environment and software. However, the formulation of the tasks was deemed necessary in order to define the full scale of necessary work. Remaining items will provide interesting future work opportunities.

2 MODELLING NEEDS

2.1 CIGRÉ Benchmark

2.1.1 CIGRÉ Benchmark in PSCAD

The Cigré Benchmark Model for HVDC Controls was constructed in April 1991 to have a Benchmark for control and HVDC studies.

This Benchmark was used as a tool, to test and optimize HVDC control systems for connecting weak AC grids.

It contains a 12 pulse, 500kV, 1000MW monopolar transmission system.

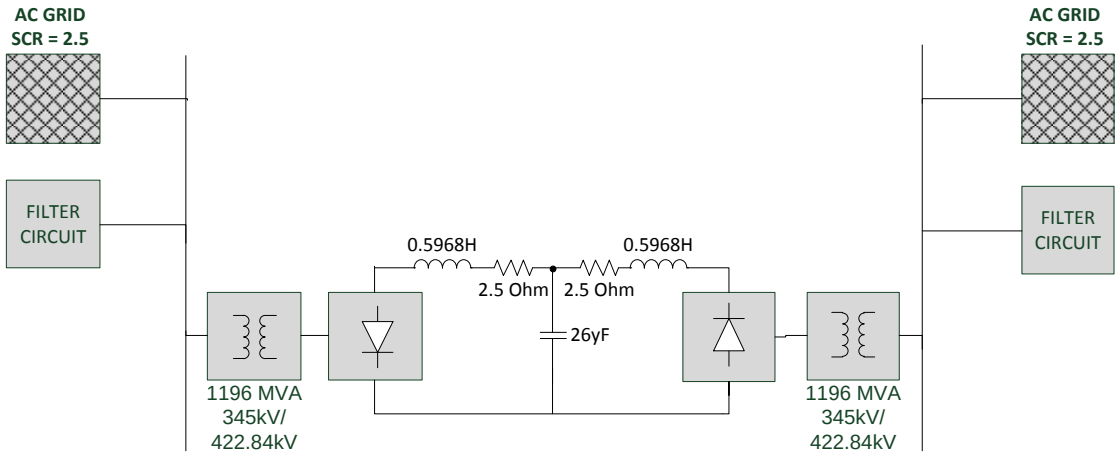


Fig. 2: Cigré Benchmark Model

On both ends of the DC transmission line a static grid with a SCR of 2.5 is modeled.

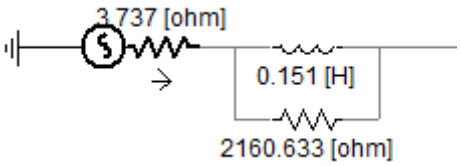


Fig. 3: AC Grid Rectifier

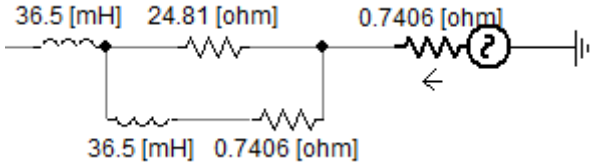


Fig. 4: AC Grid Inverter

It is the first Benchmark Model, to test control systems for remote HVDC transmission. The converters are the classical thyristor based 12 pulse (two 6 pulse converters in series with a 30 deg phase shift). The control mechanism behind this model is the following case. The rectifier is controlling the current, while the inverter controls the extinction angle gamma. This is an “old fashioned” principle of controlling the voltage somehow, and not state of the art anymore.

It’s equipped with the typical VDCOL function, as a safety function to prevent a sudden rise of the DC current while DC voltage drops, to serve the power demand

that is created on the inverter side. But regarding another suboptimal fact, the VDCOL function, as it is implemented in this Benchmark, is DC based. Due to the fact that AC Voltage drops before DC Voltage this is not the most efficient solution for the classic HVDC transmission system.[IX]

2.1.2 CIGRÉ Benchmark in SimPowerSystem

The real-time model implementation made by OPAL-RT deals with the same architecture as the original Cigré Benchmark Model from 1991.

But, in contrast to the original model it is enhanced with a lot more features regarding control and safety issues. The main task behind the OPAL-RT model is indeed primarily specializing on closed loop controls. This means, that the focus of that model is laid on specific control optimization, and in contrast to the original Benchmark, not on an overall investigation of the stability and performance of a HVDC transmission link connecting two AC-Grids.

For the pursued study it is, of course, in general a disadvantage that the Benchmark models differ from each other. However, as can be seen later-on this difference is actually not relevant with regard to a comparative statement of VDCOL versus AVS.

The default OPAL-RT Benchmark is constructed to reach a steady state after starting it, but with the strange property that the system shows permanent oscillations. To implement and test the AVS it is mandatory to bring the system to a normal steady state operating point through some corrections.

A lot of step functions are implemented in the default automatic start-up process of the model to allow investigations on the dynamic response of the controllers. This required massive modifications on the whole system before an implementation of the AVS could take part.

The differences in the Benchmark and the necessity to modify the unstable oscillating controllers make the already tight project time even a harder challenge.

[IX] M. Szechtman, T. Wess, and C. V. Thio, “First Benchmark Model for HVDC control studies,” *Electra*, no. 135, pp. 54–67, Apr. 1991

2.2 AVS Model and RT Implementation

2.2.1 AVS Implementation in PSCAD

This part of the thesis shows not only the particular implementation of the AVS in the CIGRÉ Benchmark, but also the first stages of getting into the working principle of a classic HVDC transmission system.

On the following tiers, an evolutionary process from a simple classic HVDC transmission system to the state of the art of a controlled system is demonstrated. The first steps were necessary to obtain the basic know-how of the working functions and controls of a classic HVDC System, in order to be able to implement the AVS mechanism in the SimPowerSystem model in a next step.

It should be mentioned that no detailed description of the working principle, inside the converters, i.e. the behavior of the thyristors itself, mechanism of PLL, etc. is explained in the following description. Just facts that have direct impact of the system behavior, especially the AVS and further implementations, are described in more detail.

On the last tier of this subproject the behavior of the AVS and the automatic power reducer are shown in a detailed description, including a comparison with the pure VDCOL mechanism.

Data and Values of different model parts, that are not explicit written on the specific parts, will appear in the appendix in form of a chart. In the further development of that basic circuit, just variation in data or new values will be shown in the system graphics. If there is nothing shown, the default data of the basic circuit is assumed. [X]

[X] Tiers 1 -5 based on internal results from Kuehn, W.

2.2.1.1 Tier 1 - Basic classic HVDC transmission System

This first stage of the project shows the Rectifier (GR) and the Inverter (WR), connected via a resistor as a simple model for a short DC line.

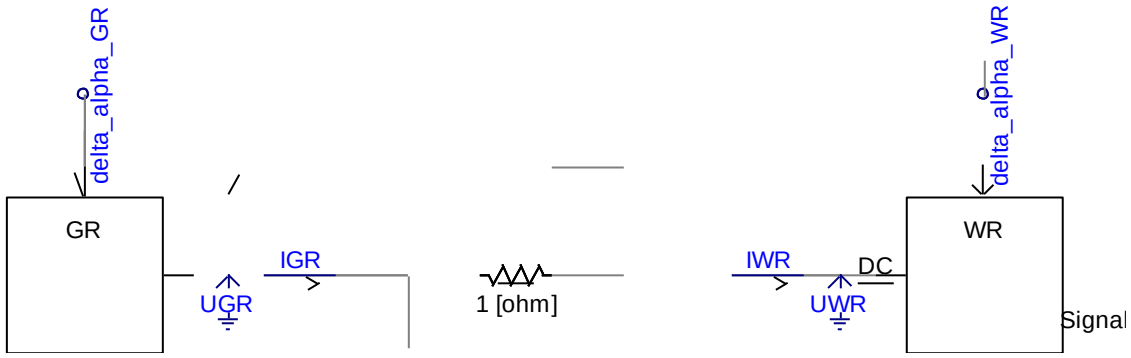


Fig. 5: DC Link

Also the basic control system of the HVDC transmission system is shown in Fig. 2 and a detailed description of the working principle can be taken from below.

The default control method of classic HVDC transmission is used here: the rectifier controls the DC current while the inverter controls the DC voltage, and in case the firing angle alpha hits its limit ($alpha\_min$=5°) the inverter takes over the current control.

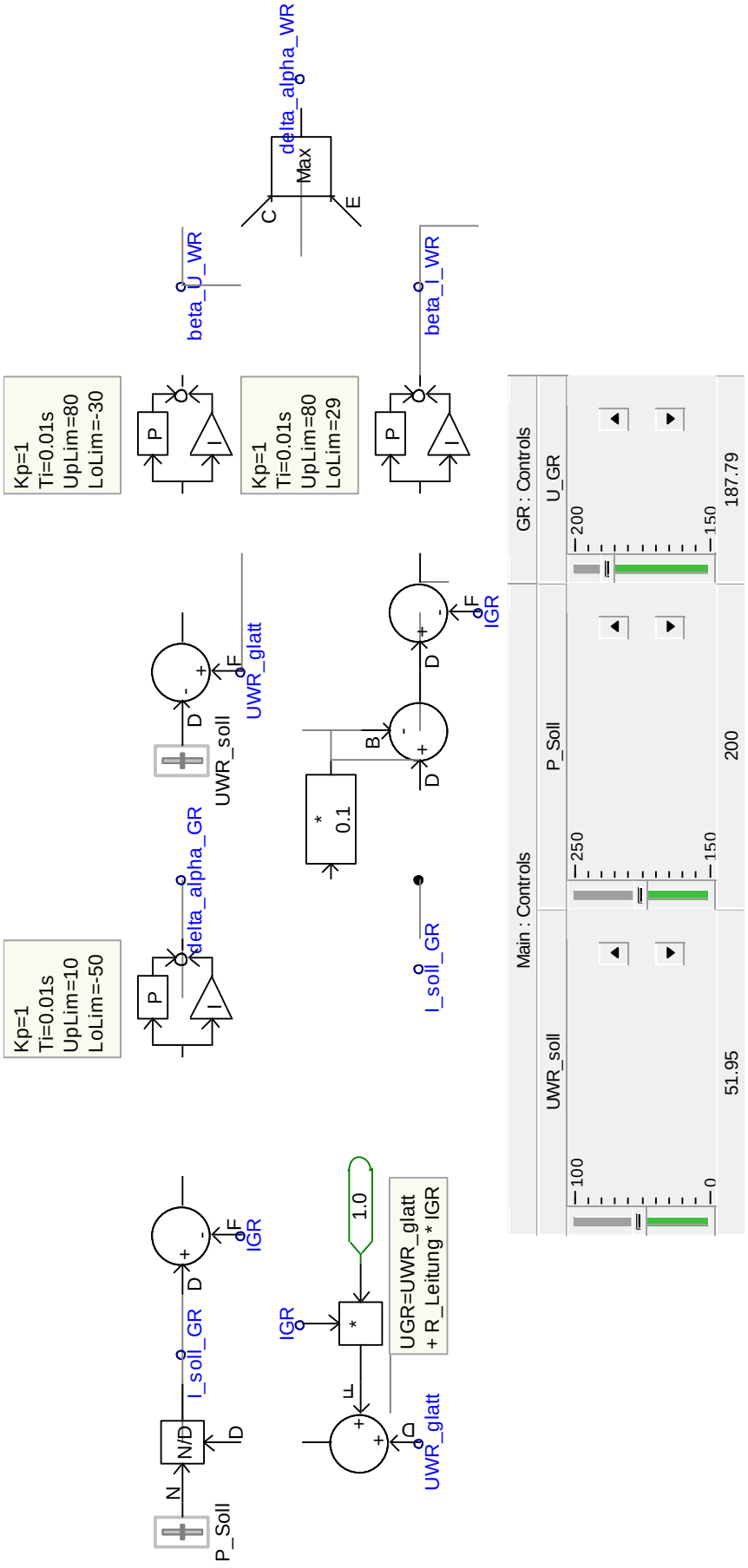


Fig. 5: Closed Loop Control System

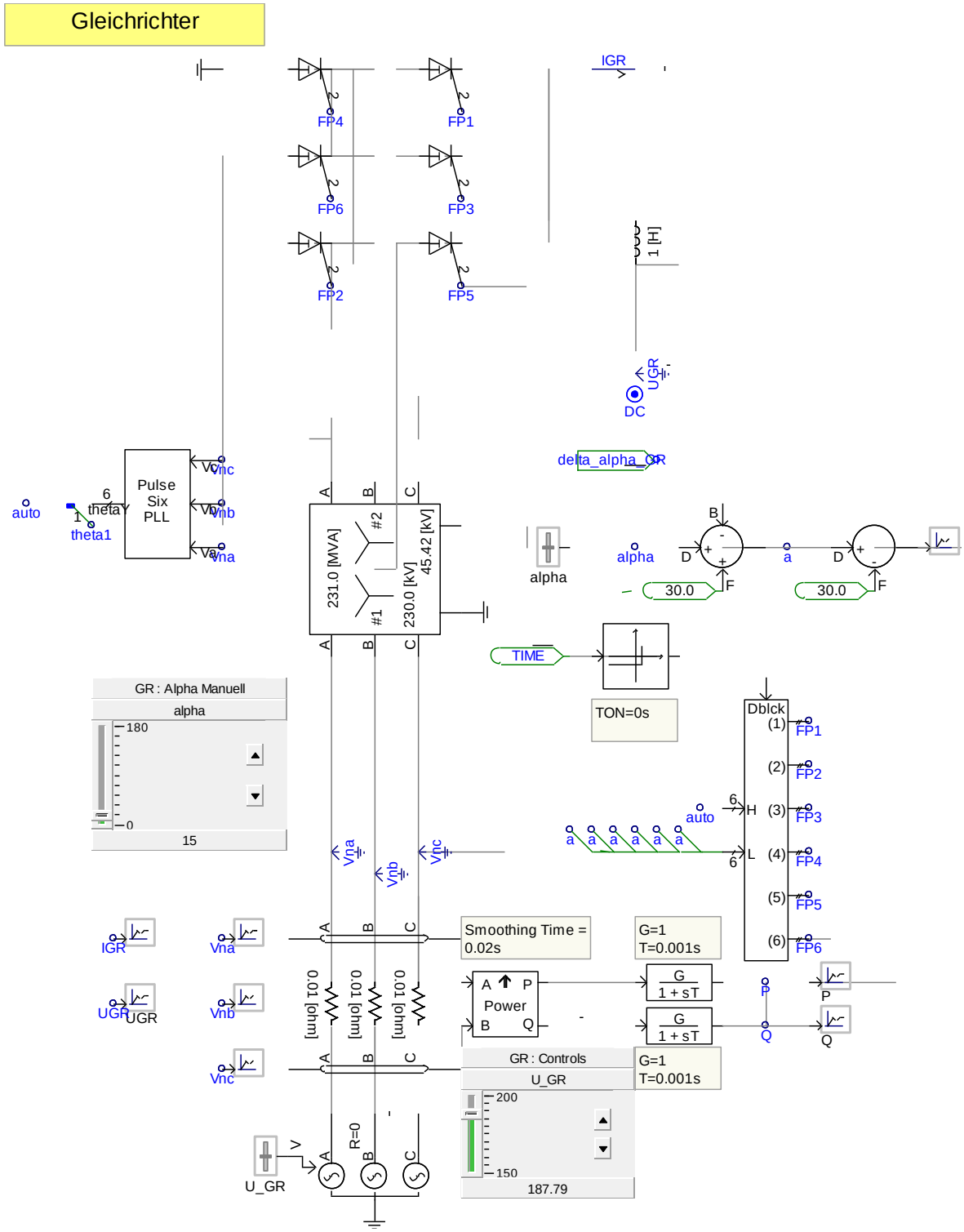


Fig. 6: Rectifier

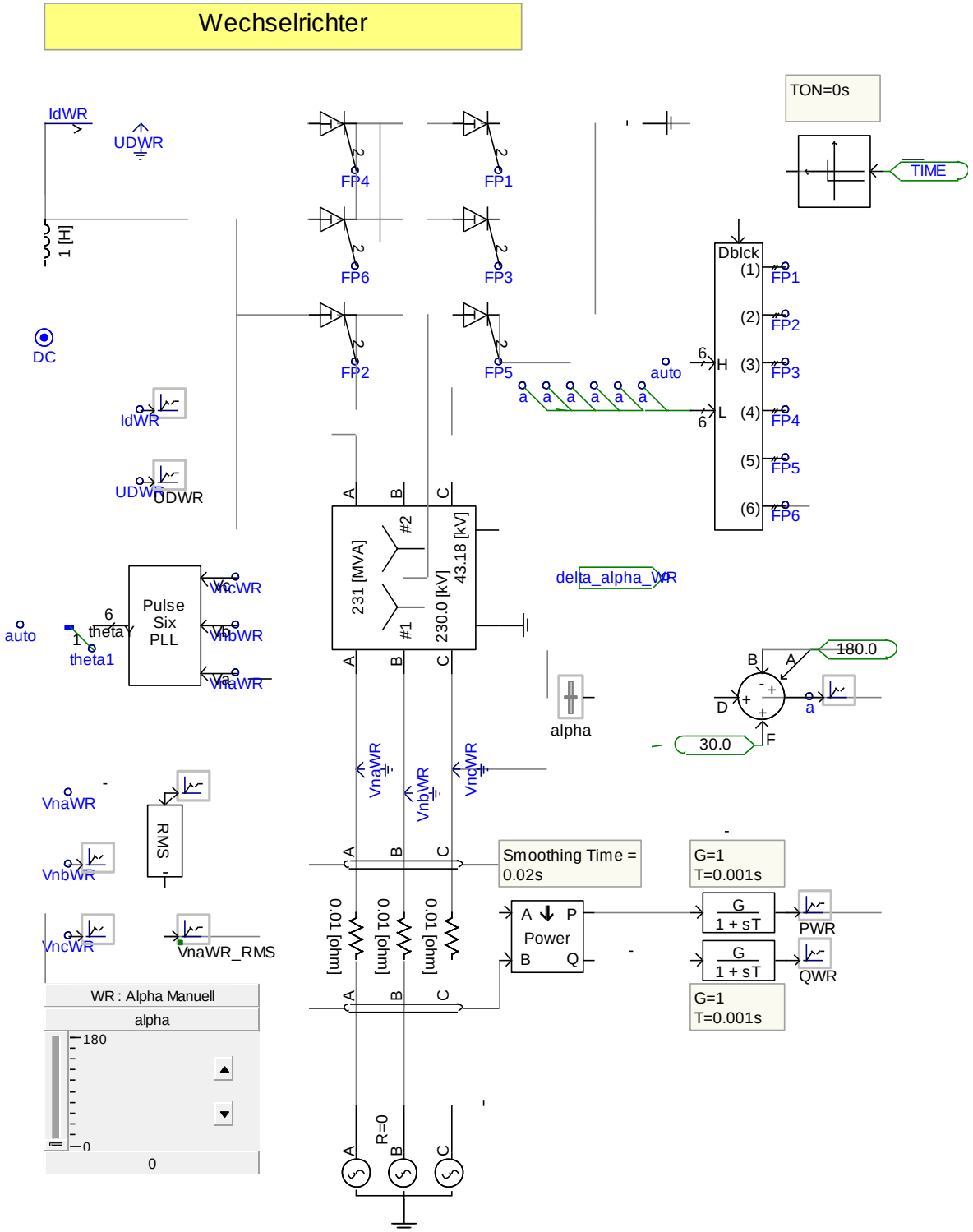


Fig. 7: Inverter

Nominal Conditions

To allow a further evaluation, the nominal conditions of the circuit should be explained.

$V_{DC} = 51.9\ kV$

$I_{DC} = 3.6\ kA$

$alpha\ GR = 15°$

$V_{AC\_Inverter} = 230\ kV$

$V_{AC\_Rectifier} = 230\ kV$

Due to a disadvantage of PSCAD, when using an external input value of the static voltage source, the Line-to-Ground value has to be chosen, and then the Peak Voltage Magnitude.

Due to that fact, the external Voltage input responds to the following equation:

$$V_{AC\_Extern} = \frac{V_{AC\_Rectifier}}{\sqrt{3}} * \sqrt{2}$$

$$V_{AC\_Extern} = 187.79\ kV$$

Rectifier Control

A basic P-I controller is used to the control the firing angle alpha of the rectifier. By dividing the Power demand by the given DC Voltage on the transmission line a reference value for the DC current (I_{soll_GR}) is generated.

The DC voltage is measured at the inverter and the loss on the transmission line is added to the reference value in order to have the right value for the input of the closed loop controller.

The DC voltage on the rectifier side responds to the following equation:

$$V_{Rectifier} = V_{Inverter} + (Resistance_{Line} * I_{DC})$$

This is equal to the German notation, as shown in the diagram:

$$UGR = UWR_{glatt} + R_{Leitung} * IGR$$

So the P-I controller is correcting the difference between the reference current I_soll_Gr and the measured value IGR on the transmission line. The actual firing angle of the rectifier is composed of the manually settable angle delta plus the change of the firing $delta_{alpha\_GR}$ which is the output of the P-I current controller. The angle of 30 degrees takes into account the difference in the zero-crossing of the commutation voltage and the phase voltage.

Inverter Control

The difference of the values for the measured DC Voltage UWR_{glatt} and the reference value UWR_{soll} is the input for the closed loop controller that is controlling the DC line voltage.

When firing angle $alpha$ hits its limit, the lower branch (Fig.2, current control branch) of the control system starts working. The working principle of this branch is almost the same as the one for the current control done by the rectifier, but without the consideration of any voltage loss on the transmission line, and a subtraction of the current margin value, which is necessary to ensure a save hand over process of the current from the rectifier to the inverter.

In our case, a value of 10% of the reference DC current is subtracted from the original value I_{soll_GR} and compared with the actual value IGR.

Both, the upper and the lower branch of the described control mechanism create a variable. For the upper branch (voltage control) it is $beta_{U\_WR}$ and for the lower branch (current control) it is $beta_{I\_WR}$. Both variables are inputs for a max-function, whose output $delta_{alpha\_WR}$ is the direct actuating variable of the inverter.

Results

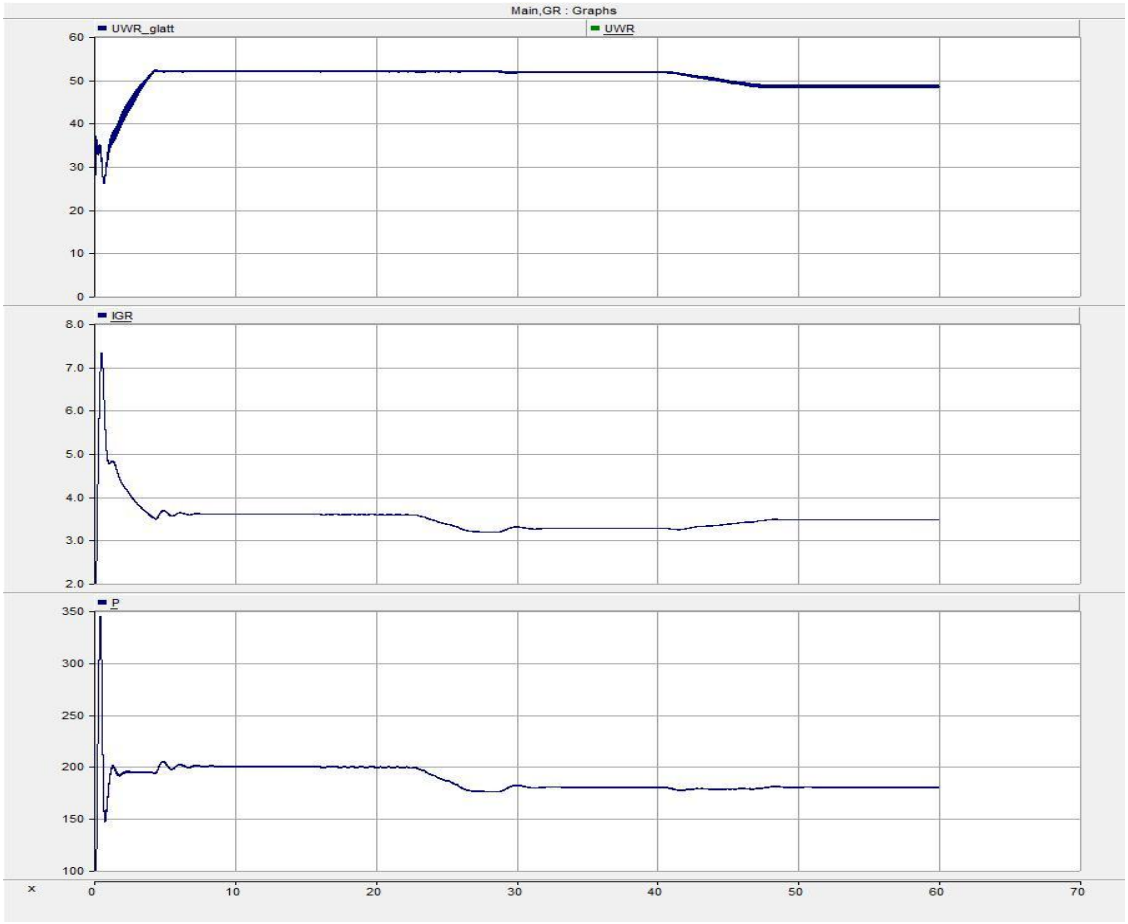


Fig. 8: Main Data

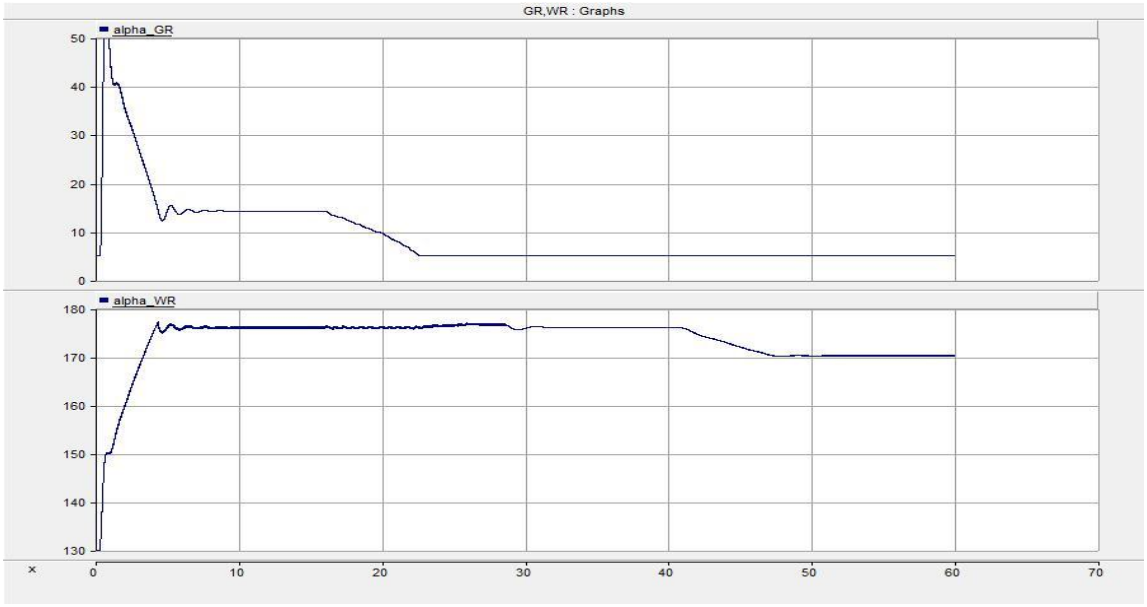


Fig. 9: Firing Angles

For the test scenario shown in the graphics above, the internal grid voltage of the rectifier is reduced.. This simulates a real event that can take part in any transmission system caused through either switching off AC lines or a disconnection of reactive power consumption. After the systems reaches a steady state at approximately 15 seconds the internal grid voltage on the rectifier side is reduced down to 180 kV and we can see the firing angle alpha hitting the limit and the hand over process of current control from the rectifier to the inverter (Fig. 9, Trace 1&2).

Due to that, a power drop down to 180 MW occurs, which is caused by the subtraction of the current margin of 10% (Fig. 8, Trace 3).

$$P = 200MW - 10\% = 200\ MW - 20\ MW = 180\ MW$$

At approximately 40 seconds the internal grid voltage drops further down to 175 kV and the already no-controlled DC Voltage (UWR_{glatt}) drops further down, while the DC Current (IGR) continues to increase (Fig. 8, Trace 1&2).

2.2.1.2 Tier 2 – Enhanced System with current margin compensation

As shown in the explanation of Tier 1, a Power drop of 10% (in our case 20MW) comes along with the hand over process of current control to the inverter and the consequential subtraction of the current margin. This circumstance is, for sure, a big disadvantage and requires a remedy.

The most adaptive and best solution for this is the implementation of an integrator that abolishes the difference of the current margin value in a smart way.

This principle is shown in the advanced main circuit display in the graphics below. It is important to know; from now on, only advancements in the model are explicitly shown in the graphs of the model. Parts that are not shown remain the same as in the basic circuit.

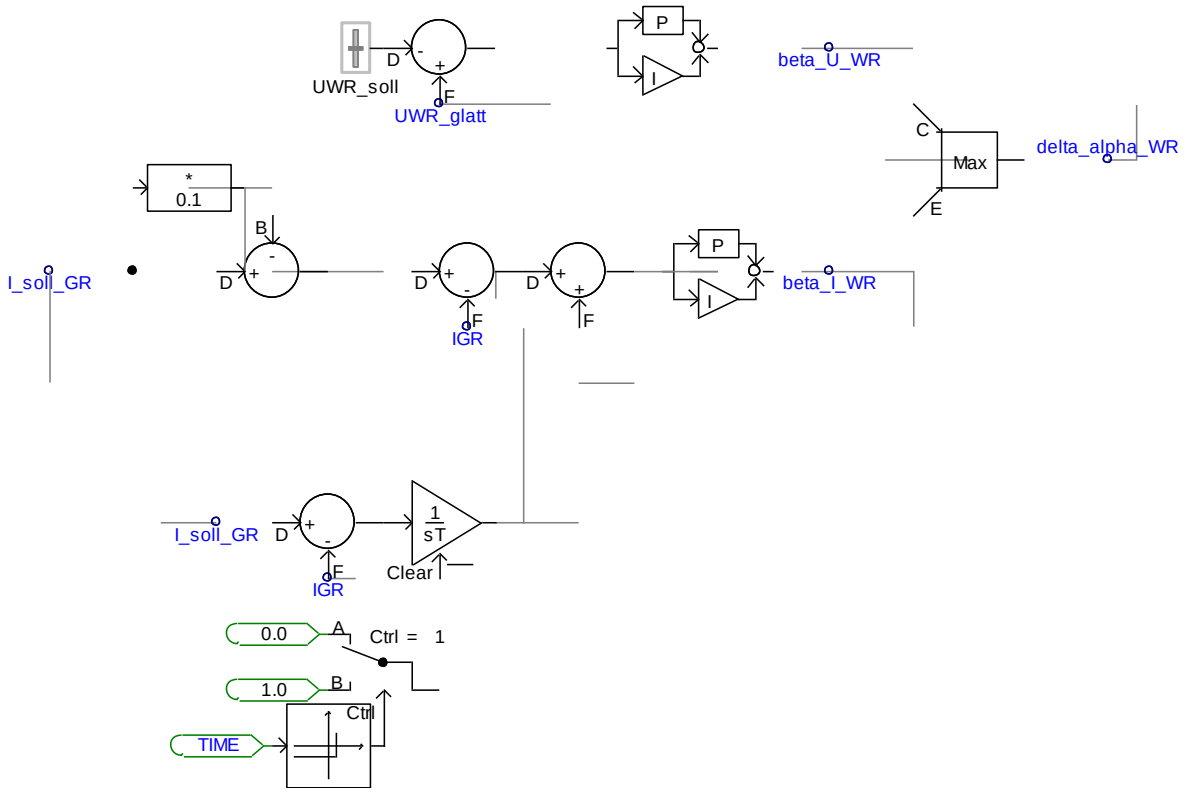


Fig. 10: Current Margin Compensation

The time based switch in Fig. 10 sets the current margin compensation of for the first 5 seconds of the simulation, to ensure a save powering up of the system.

The integrator used in that case uses a time constant of 0.7 seconds and the upper limit of its output is the fixed value of 0.36kA resulting from $Id_{margin} = I_{DC} * 10\% = 3.6kA * 0.01 = 0.36kA$ while the lower limit still remains at zero.

In this case now a ramp function, that increases and decreases the power order of the system is used to show the current margin compensation mechanism.

But some more modification had been done, the internal grid voltage of the rectifier V_{AC} is now in p.u., this is a useful modification in order to allow an easier handling and judging of the system in the further stages. Also the display of the reactive power Q (Fig. 12, Trace 4, green line) is now embedded in the diagrams. The duration of the test cycle is enlarged to 120 seconds, for some demonstration issues.

The applied power order function is shown in the graph below.

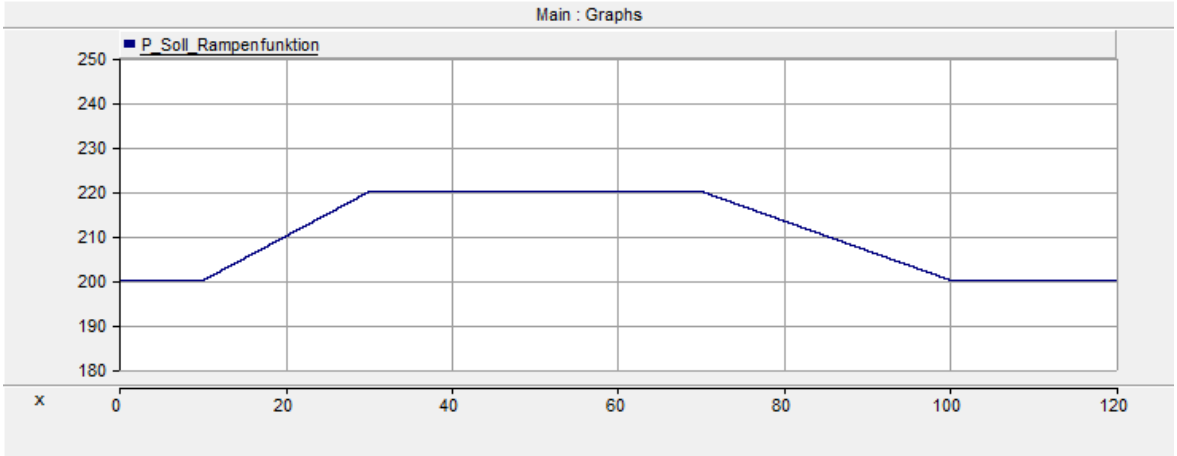


Fig. 11: Ramp Function 1

Results

After reaching nominal conditions at approximately 10 seconds, real power is ramped up to 220 MW (Fig. 12, Trace 4, blue line).

At almost 40 seconds, the internal grid voltage is ramped down very fast, to a value of 0.95 p.u. and the hand-over process can be seen on the diagrams. But in contrast to the results obtained with tier 1, in this case the power remains at its reference value and at 55 seconds the internal grid voltage is ramped back to nominal conditions and the power order is also ramped down to 200 MW again.

This may look quite good, regarding the power that is transmitted over the DC link, but another disadvantage shows up regarding the DC Current between 40-60 seconds (Fig. 12, Trace 3). Due to the fact that DC Voltage is not controlled anymore, and drops down, the current I_{GR} rises to a higher value in order to cover

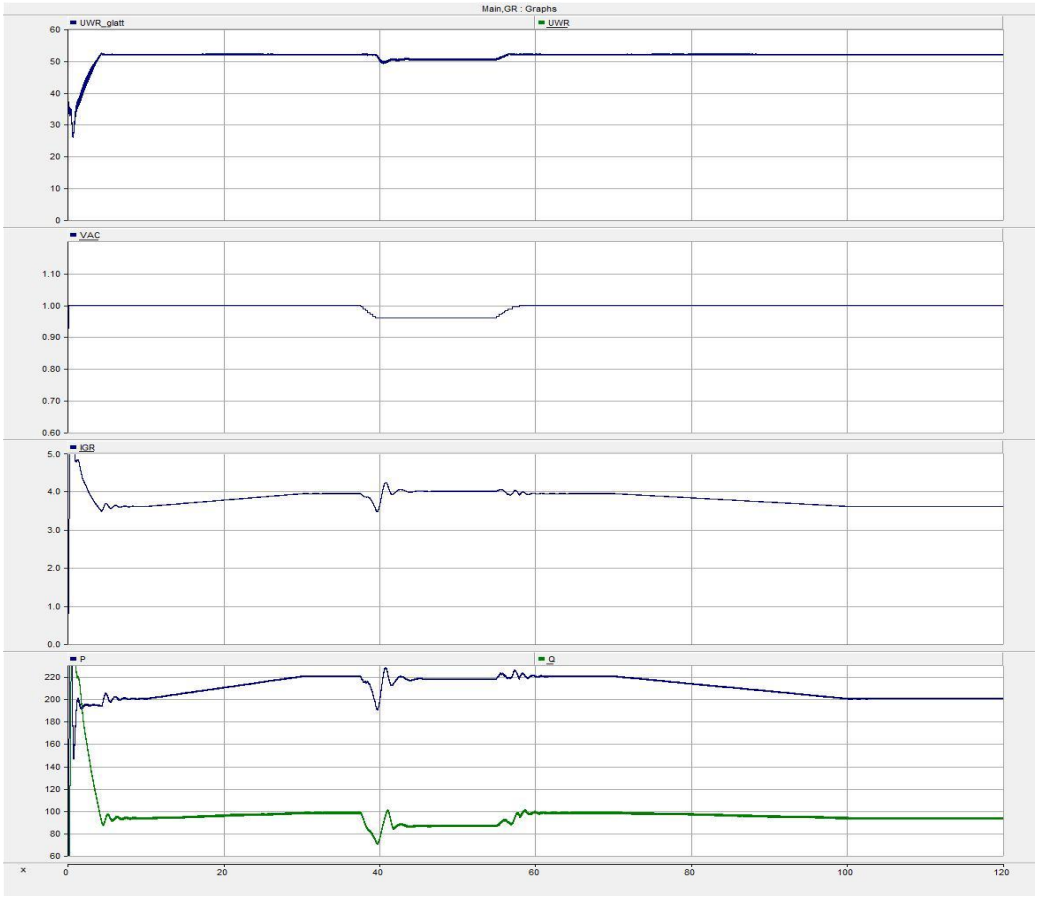


Fig. 12: Main Data

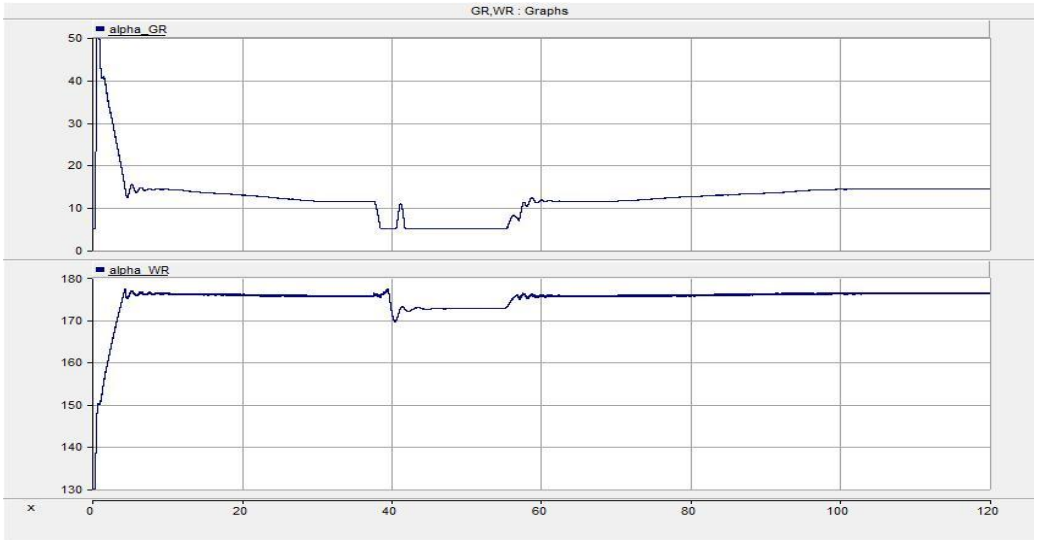


Fig. 13: Firing Angles

the power demand. If not limited, this can lead to unwanted consequences regarding thermal stress and transmission stability.

2.2.1.3 Tier 3 – Implementation of VDCOL

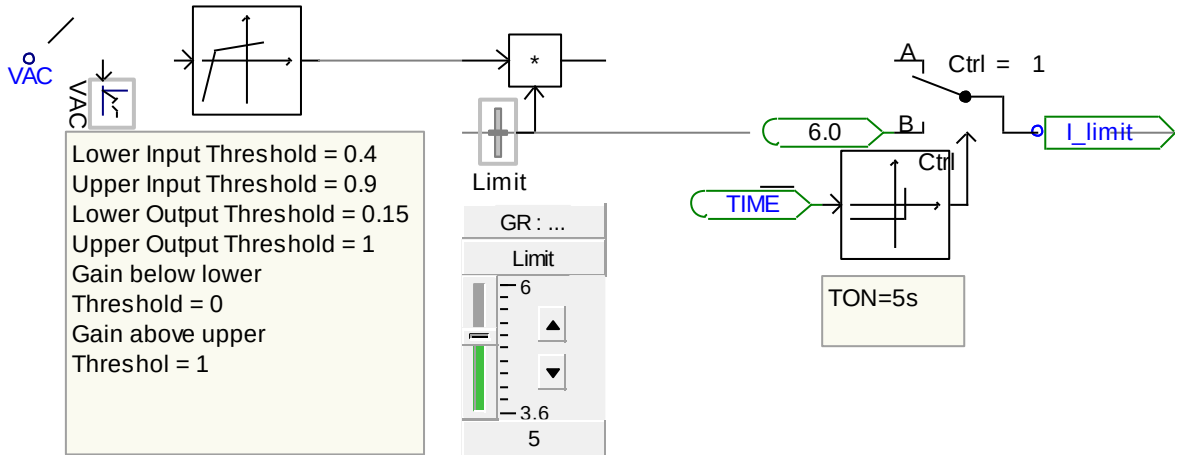
The previously mentioned DC current increase beyond a certain continuous value is for temperature rise reasons (rated value for nominal ambient conditions and some higher value for low ambient conditions and/or, e.g., 10 min overload) not permissible for an HVDC transmission system. Temporary short time overcurrents are permitted but they can cause voltage stability problems when operating on weak AC grids.

The stability problem can be illustrated with the following example. The Pacific HVDC Intertie connects in the Pacific Northwest Area the Celilo Converter Station, with the Sylmar Converter Station in the Los Angeles Area.

Considering the Celilo Station as the rectifier and the Sylmar Station as the inverter in order to have an energy transfer from north to south. As a main principle of classic HVDC the rectifier at the Celilo Station is controlling the DC current while the inverter at the Sylmar station is controlling the DC voltage. Due to a weak AC grid on the Celilo Rectifier Station, the firing angle alpha of the rectifier hits its limit with a corresponding DC voltage decline and according to the marginal current control principal DC current control is taken over by the inverter. The DC voltage decline causes the inverter to further increase the DC current in order to serve the power demand. But the further increasing DC current is increasing the reactive power consumption at the Celilo Rectifier Station, which again leads the AC Voltage to a further drop → A chain reaction occurs, and the whole transmission system can collapses.[XI]

This is the reason why VDCOL has to be implemented in the model.

Its main principle is a limitation of the DC current in dependency on the magnitude of the AC Terminal Voltage (VAC). The characteristic of the VDCOL function can be tuned via corner values of AC voltage and DC current and gains below above the corner values (Table in Fig. 2-11).



[XI] Richard Bunch, Dmitry Kosterev – Design and implementation of AC Voltage Dependent Current Order Limiter at Pacific HVDC Intertie (PE-408-PWRD-0-01-1999)

Fig. 14: VDCOL Implementation

Utilizing the table values the measured AC Terminal Voltage V_{AC} is the input for a transfer function, whose output is the new limited DC current order I_{limit}. To verify that VDCOL performs as desired the static ideal grid on the rectifier side has to be replaced by one with in internal inductance. Fig. 15 shows the replacement taking place in the rectifier circuit.

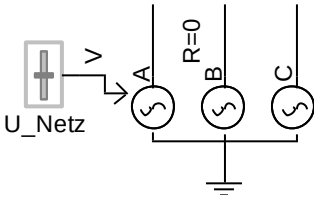


Fig. 15: Static Internal Grid

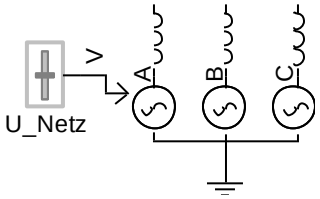


Fig. 16: Voltage Source with Internal Inductance

$$Internal\ Grid\ Inductance\ =\ 0.42mH$$

The value of the inductance was derived as follows:

SCR stands for Short-Circuit-Ratio and gives provides information about the voltage stiffness of the AC grid. The voltage source represents the internal voltage of the grid.

To establish a considerably weak grid we need an SCR about 2 or less. I.e. for a nominal power transmission of $P_{dn} = 200\ MW$, which is used in this model, the following formulas hold:

$$SCR = \frac{S_K}{P_{dn}}$$

$$SCR = 2 = \frac{400MW}{200MW}$$

$$L_{grid} = \frac{(Un_{grid})^2}{S_K*(2*\pi*50Hz)}$$

$$L_{grid} = \frac{(230kV)^2}{400MW*(2*\pi*50Hz)}$$

$$L_{grid} = 0.42H = 42mH$$

Because V_{AC} is already in p.u. and the DC current is still in kA, it needs to be multiplied with the “Limit” Value that is also shown in the graphic above.

In the closed loop control circuit shown in the graphic below, an implementation of a min-selector function became necessary, to ensure a limited maximum value of the current reference $Id_{ref}$for the rectifier. This is done by the minimum-selection of the two currents I_{limit} and I_{soll_GR} .

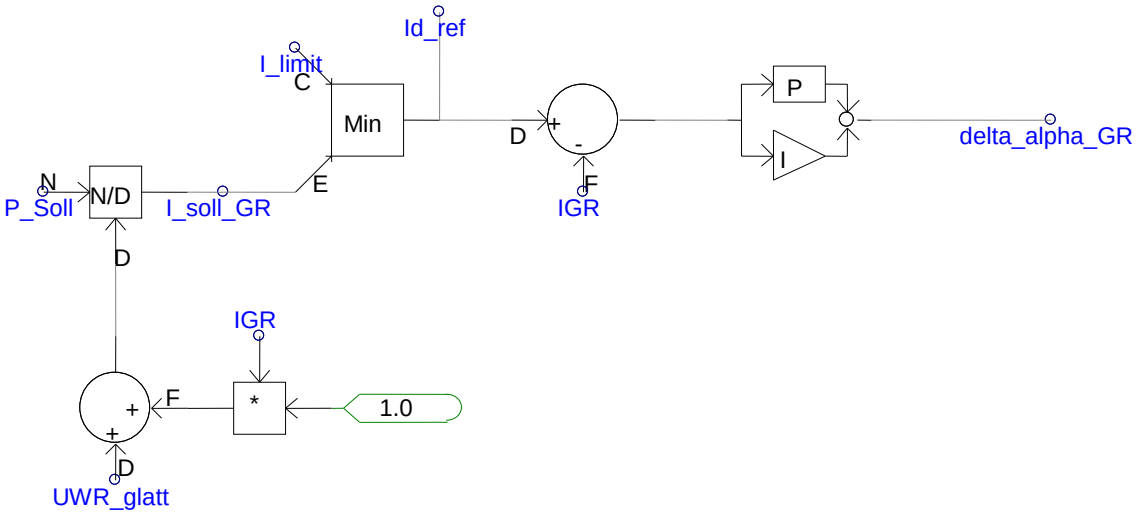


Fig. 17: Min Selector in Closed Loop Control

The output of that specific min selector is the new reference value Id_{ref} for all current controlling systems of the model.

Results

The same ramp function for the power order used in the case before is used here to show the working principle of the VDCOL.

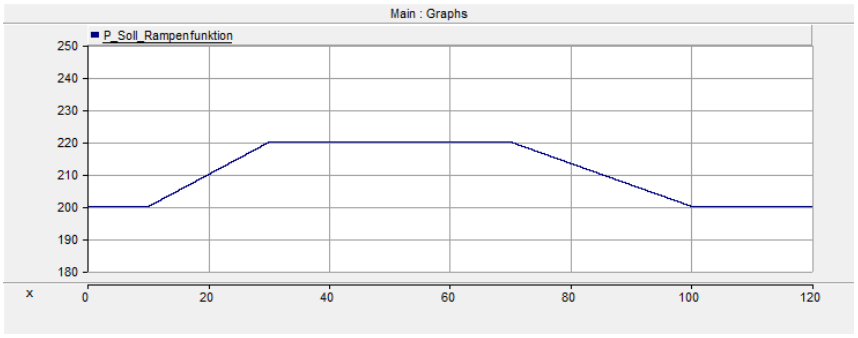


Fig. 18: Ramp Function 1

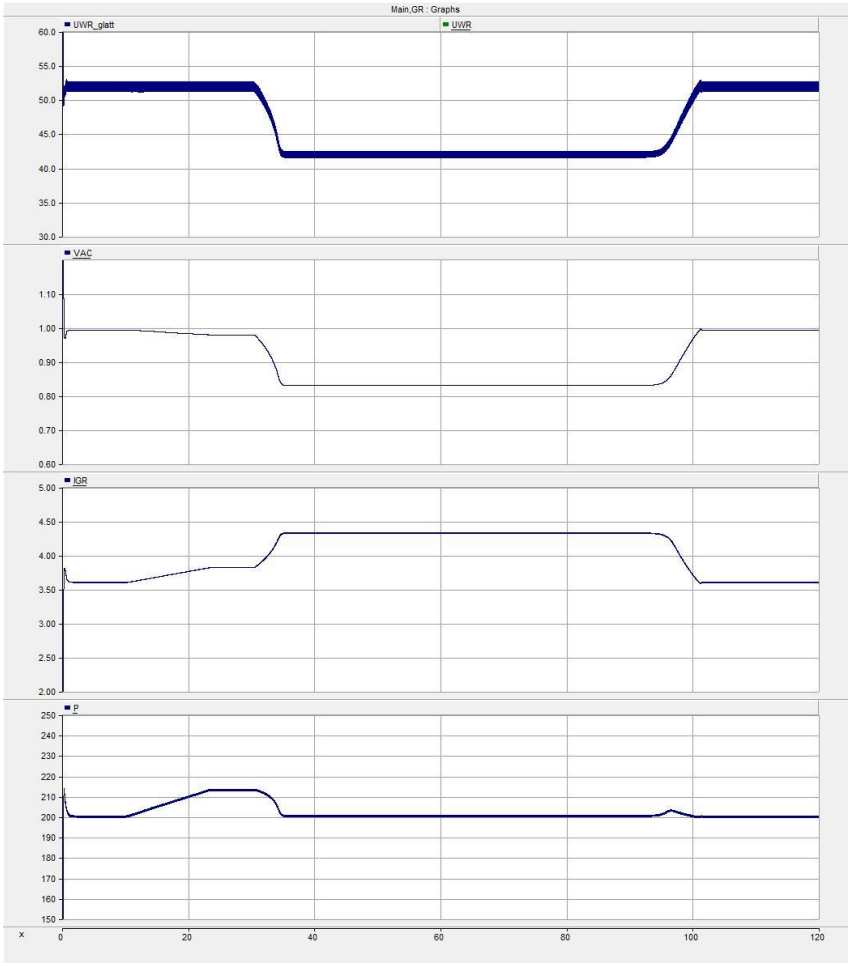


Fig. 19 Main Data

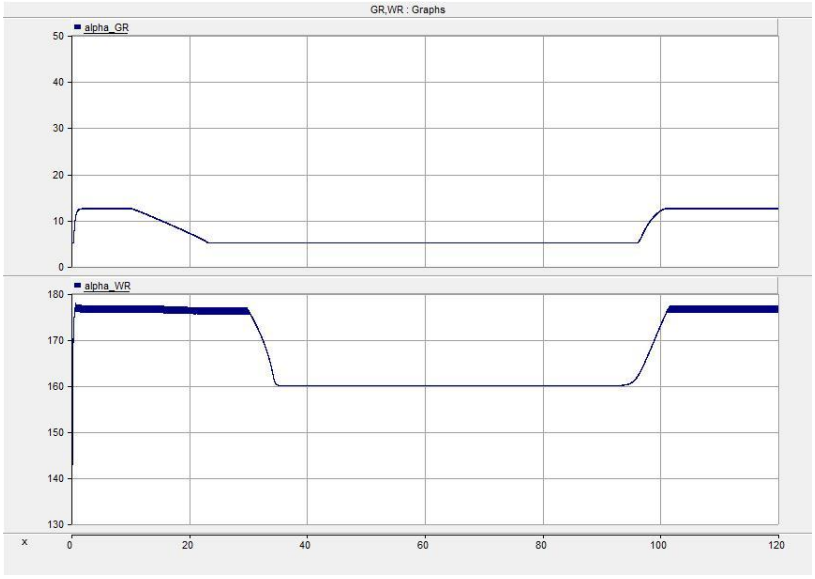


Fig. 20: Firing Angles

After the power order is ramped up to 220 MW, the graph shows a slight drop in the AC Terminal Voltage V_{AC} (Fig. 19, Trace 2). After approximately 30 seconds, the inverter takes over current control (Fig. 20, Trace 2). What we can see

accordingly, is a sudden drop in the AC Terminal Voltage V_{AC} and in the DC voltage U_{WR_glatt} (Fig. 19, Trace 1&2), this is caused by the fact, that the DC voltage is no longer controlled anymore. But then after approximately a few seconds, the VDCOL is activated and limits the sudden steep rise of the DC current I_{GR} (Fig. 19, Trace 3).

This mechanism protects the system against overload and can also protect against voltage collapse at certain given grid conditions.

However, as we can see there is the problem of a considerable reduction of DC and AC voltage with very detrimental consequences when we consider that DC power transmission over long distances requires for efficiency reasons a sufficiently high DC voltage and that consumers need a sufficient high AC voltage.

2.2.1.4 Tier 4 – Implementation of AVS

The prepared stages are completed at this point of the pre-project, and the time has come to implement the AVS in this model.

The graphic below displays the main circuit and gives an overview of the AVS implementation in this circuit. This mechanism is implemented in the closed loop control circuit.

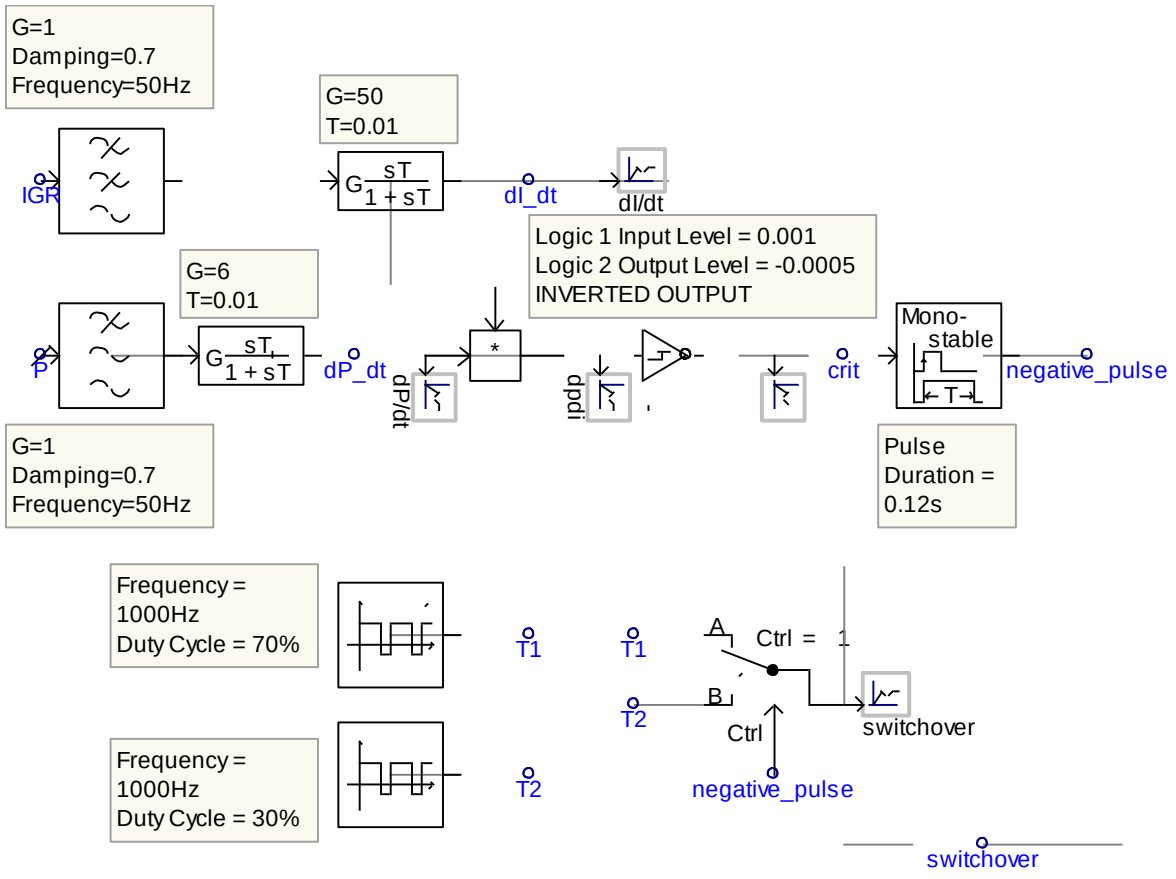


Fig. 21: AVS Mechanism

At this stage of the project there will be no further explanation of the working principle of the AVS. This will be done in a later stage, where we show its working principle on the basis of the Cigré Benchmark model; this will be more useful regarding a comparison of PSCAD and SimPowerSystems. In that further stage the AVS is fragmented in its different parts and each part is explained in detail regarding its working principle and what its meaning is regarding the whole AVS mechanism.

Just some basic explanations regarding its way of acting, should be mentioned here to allow a judgment of the upcoming results.

The graphic below displays the implementation of the AVS in the basic closed loop control circuit of the inverter. Furthermore it is just the signal *switchover* that triggers the switch, as shown below, with the result of a change of the algebraic sign of the current control unit from positive to negative.

This fact leads the operation point to be shifted back to the upper (**stable**) branch of the PV-Curve. The mechanism of how the AVS actually decides if the sign should be positive or negative, is shown the Fig. 21. As mentioned before, a detailed description of “How exactly” that works comes along with the Cigré Benchmark introduction.

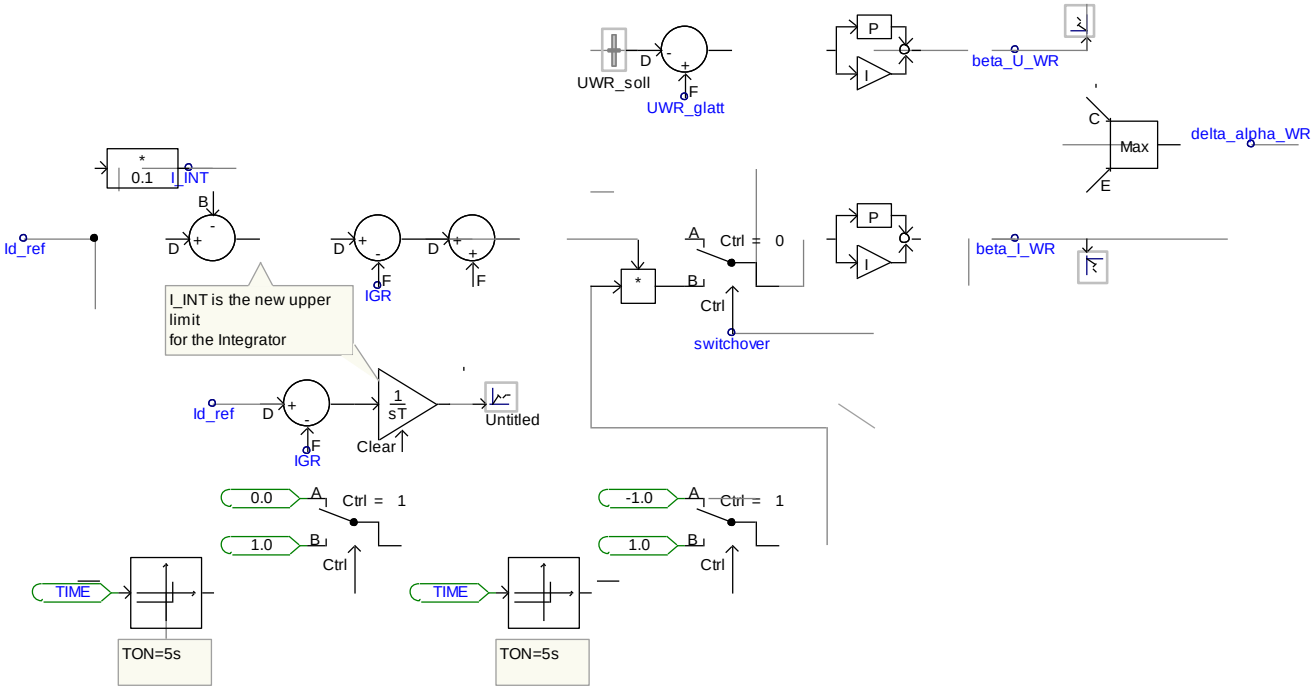


Fig. 22: AVS Implementation in Closed Loop Control

The second time based switch in Fig.22 was implemented due to ensure a safe ramping up of the system, without the AVS interrupting it.

Results

This scenario deals with a new ramp function for the power, and the simulation time is reduced to 60s, to become equal in time with later test scenarios this modification become necessary.

The new ramp function is shown in Fig. 23 below.

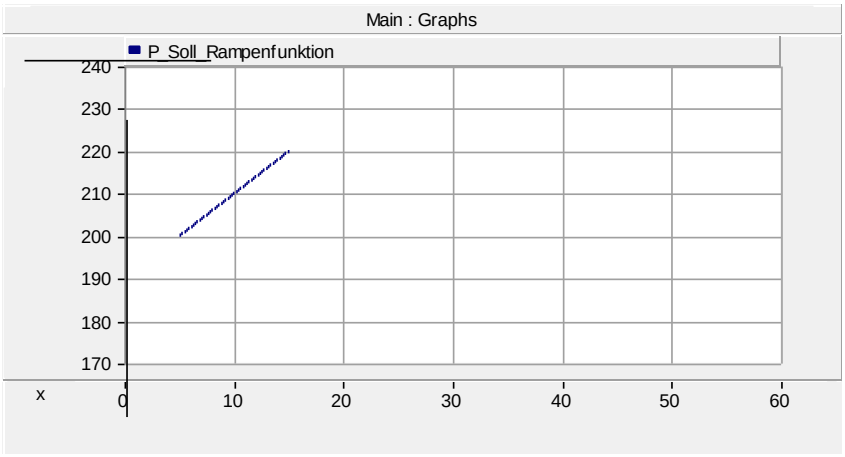


Fig. 23: Ramp Function 2

After increasing the power order to 220MW (Fig. 23), we can see the firing angle $alpha_{GR}$ (Fig. 24, Trace 1) hits it's limit at about 12 seconds, the hand over process of the current control is initiated, and at about 18 seconds, the inverter has taken over the control (Fig. 24, Trace 2).

But, in contrast to the previously shown results, the DC voltage U_{WR_glatt} and AC voltage V_{AC} depression (Fig. 25, Trace 1&2) and the steep rise of the DC current I_{GR} (Fig. 25, Trace 3) don't show up. This is due to the effect of AVS being active in that model.

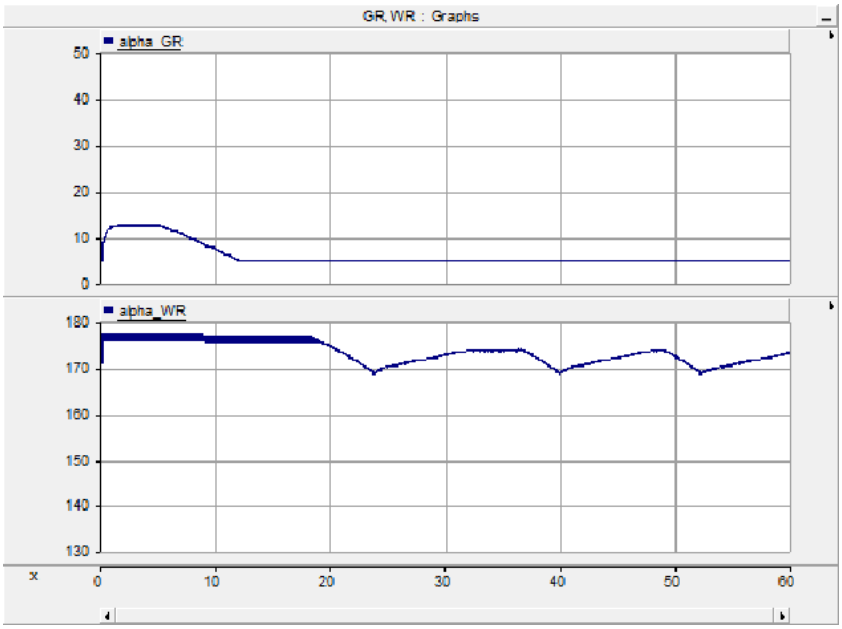


Fig. 24 Firing Angles

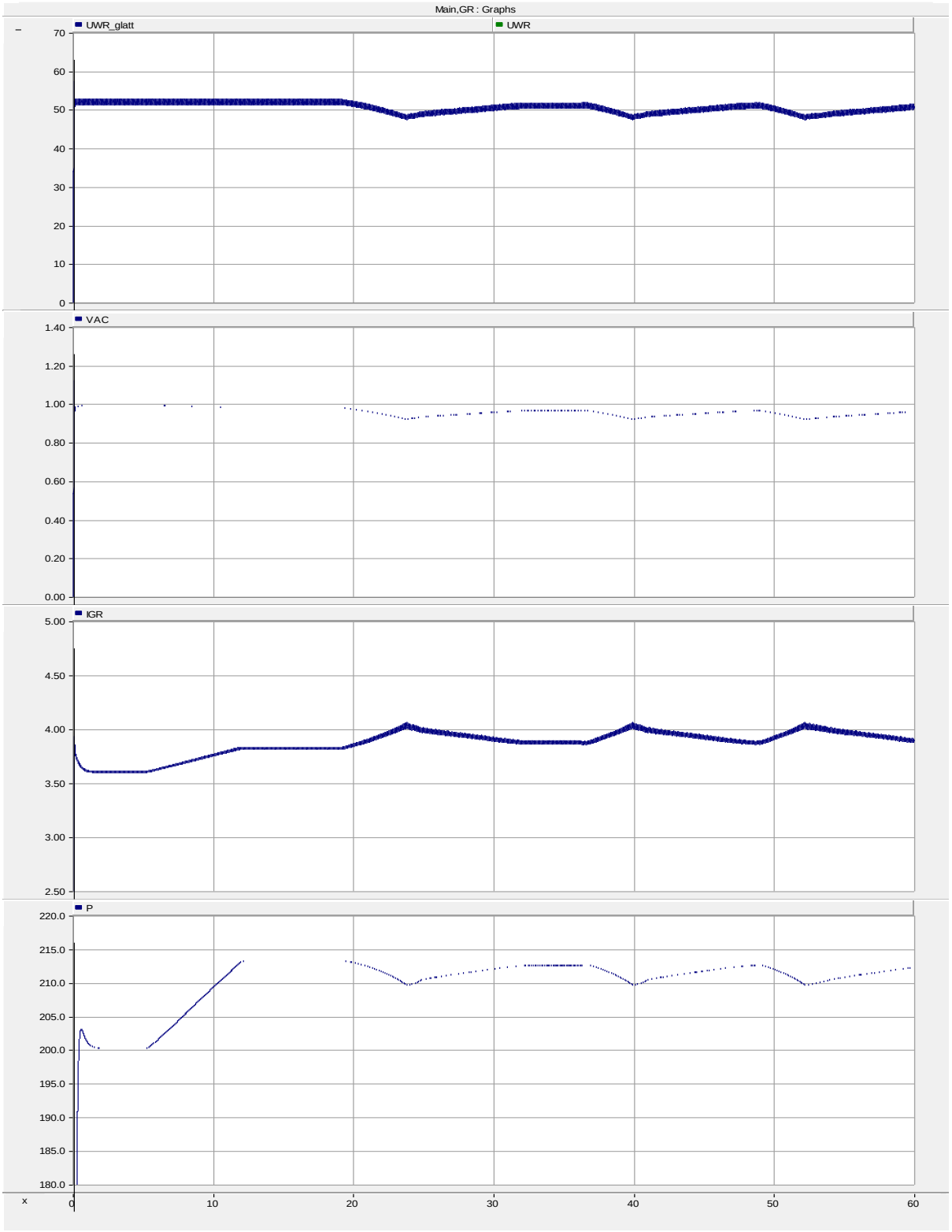


Fig. 25: Main Data

The AVS is recognizing that the MTP-Point (Maximum Transferable Power Point) is surpassed on the PV-Curve and shifts the operating point back to the upper (**stable**) branch of the PV-Curve. The operating point revolves around the MTP-Point thus keeping the system stable.

2.2.1.5 Tier 5 – Adjusting to Cigré Benchmark nominal conditions

This is the final stage of the “pre-project”. In this stage, the nominal conditions of the Cigré Benchmark Model are applied to this internal development. No simple “value-copy-procedure” was applied, but an own calculation was made in order to reach the nominal conditions of the Cigré Benchmark Model. Due to the tight time constraints that go along with this project, idealistic assumptions were made, in order to avoid a waste of too much time regarding those issues.

The biggest difference between this model and the original Cigré Benchmark is indeed the fact that this model uses a 6 pulse thyristor group, whereas the original model uses a 12 pulse thyristor group. That circumstance is not only a difference, but a big challenge regarding the performance and design of the filter circuits. This lays back to the advantage that 5th and 7th harmonics disappear when using a 12 pulse thyristor group.

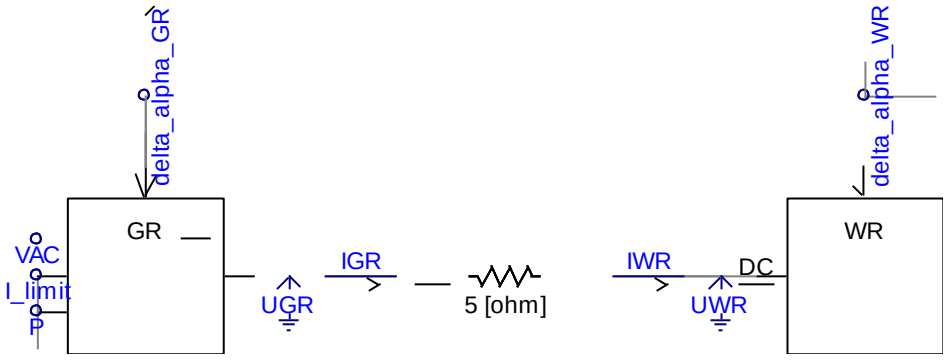


Fig. 26: DC Link

Fig. 26 shows the new DC Link, modeled with a resistance of 5 Ohm, like it takes part in the Cigré Benchmark. This value was just copied from the original model, like the inductance of the transmission line following in Fig. 27 & 28.

The outputs V_{AC}, I_{limit} and real Power P of the rectifier subpage GR, became necessary, due to scoping and controlling purposes, needed in the closed loop control circuit.

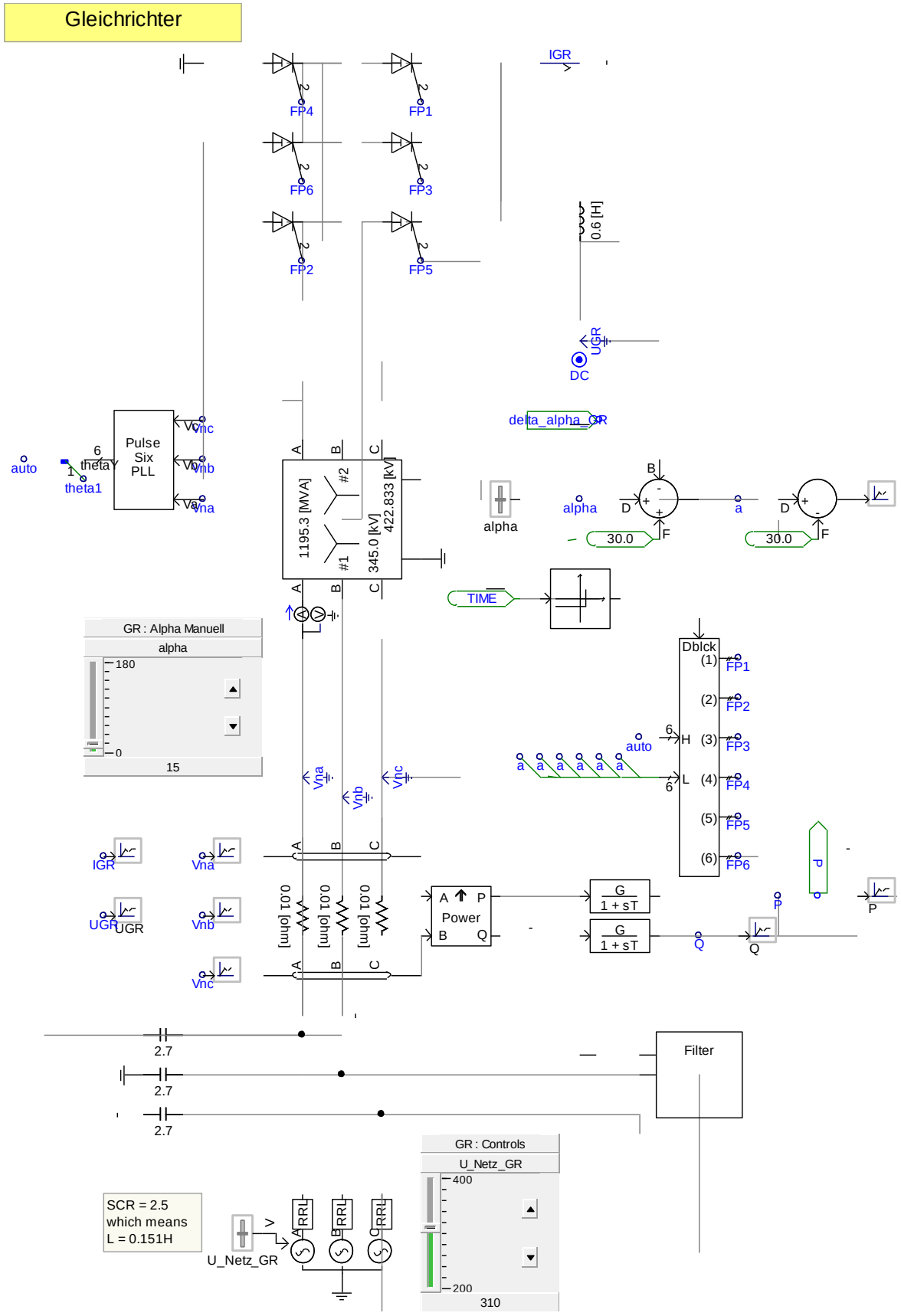


Fig. 27: Rectifier

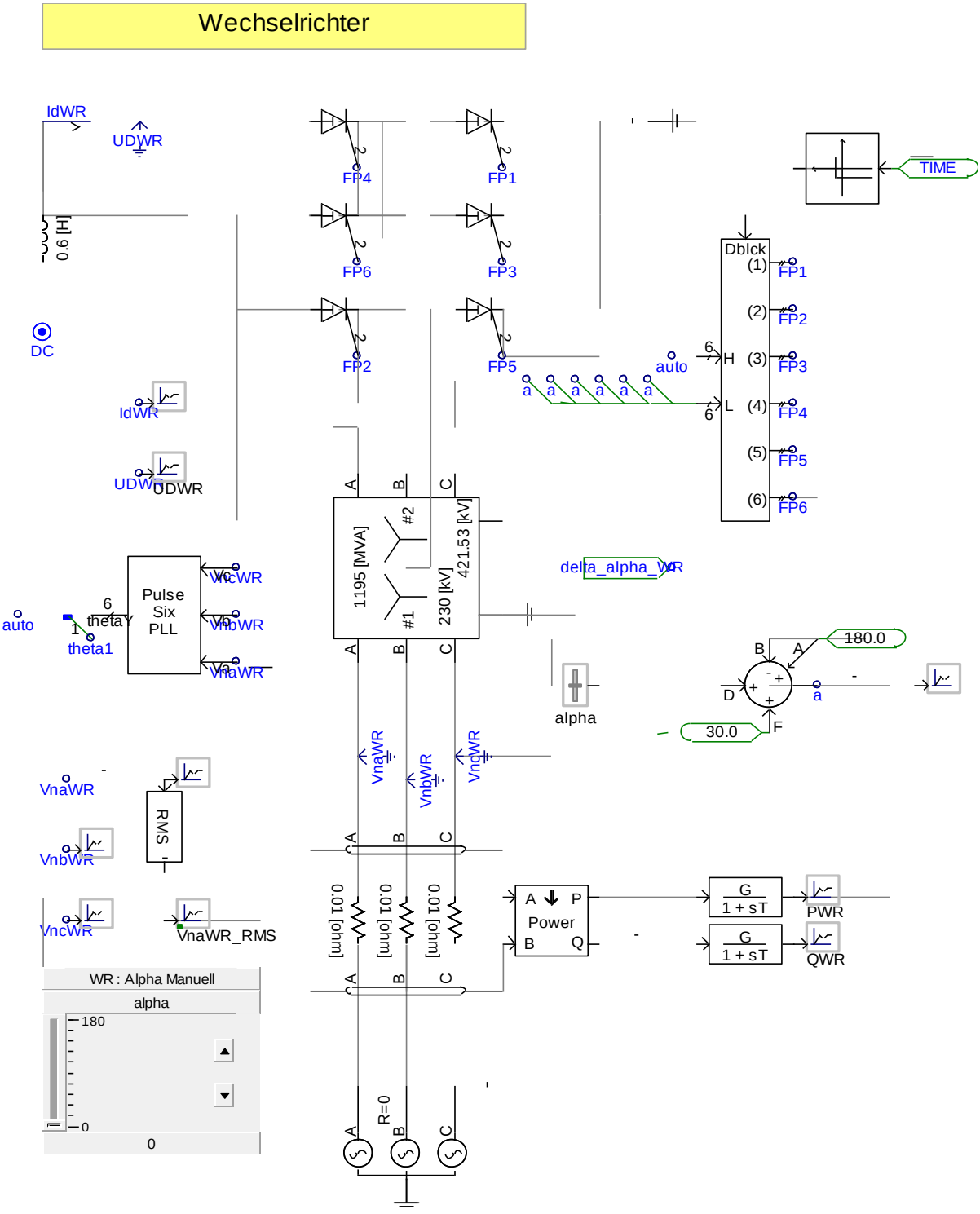


Fig. 28: Inverter

For the exact data of the used resistance, inductance and the architecture of that specific source please refer to chapter 2.2.1.

The following contains a main data calculation as it is usually performed as starting base within HVDC systems engineering. The nominal firing angle of the rectifier is 15 deg and the extinction angle of the inverter is 18 deg. The relative short circuit voltage of the converter transformer is 18 %.

Variable Description

$U_{di0} = Ideal\ \ No - Load\ Direct\ Voltage$

$U_{dn} = Rated\ Direct\ Voltage$

$S_{Transformer} = Apparent\ Power\ Converter\ Transformer$

$I_{dn} = Direct\ Current\ on\ Line$

$U_{l,Bridge} = Valve\ \ Side\ Voltage\ Transformer$

General Formulas

$$U_{di0} = {U_{dn,Rectifier}}\Big/{(cos\alpha_n - \frac{u_k}{2})}$$

$$U_{l,Bridge} = {U_{di0,\ 6Pulse\ Bridge}}/{1.35}$$

$$U_{l,Bridge} = {U_{di0,\ 12Pulse\ Bridge}}/{2.7}$$ (for completeness, not used in our model)

$$S_{Transformer} = 1.047 * U_{di0} * I_{dn}$$

Current Calculation

$$I_{dn} = {P_{dn}}/{U_{dn}} = {1000MW}/{500kV} = 2kA$$

Calculation for Rectifier

$$U_{di0} = {U_{dn,Rectifier}}\Big/{(cos\alpha_n - \frac{u_k}{2})} = {500kV}\Big/{(cos15° - \frac{0.18}{2})} = 570.82\ kV$$

$$U_{l,Bridge} = {U_{di0,\ 6Pulse\ Bridge}}/{1.35} = {570.82\ kV}/{1.35} = 422.833\ kV$$

$$S_{Transformer} = 1.047 * U_{di0} * I_{dn} = 1.047 * 570.82kV = 1195.3\ MVA$$

Calculation for Inverter

$$U_{\Delta,DCLink} = I_{dn} * R_{DCLink} = 2kA * 5\Omega = 10kV$$

$$U_{dn,Inverter} = U_{dn,Rectifier} - U_{\Delta,DCLink} = 500kV - 10kV = 490kV$$

$$U_{di0} = {U_{dn,Inverter}}\Big/{(cos\alpha_n - \frac{u_k}{2})} = {490kV}\Big/{(cos18° - \frac{0.18}{2})} = 569.07\ kV$$

$$U_{l,Bridge} = {}^{U_{di0,\ 6Pulse\ Bridge}}/_{1.35} = {}^{569.07\ kV}/_{1.35} = 421.53\ kV$$

$$S_{Transformer} = 1.047 * U_{di0} * I_{dn} = 1.047 * 569.07kV = 1191.63\ MVA$$

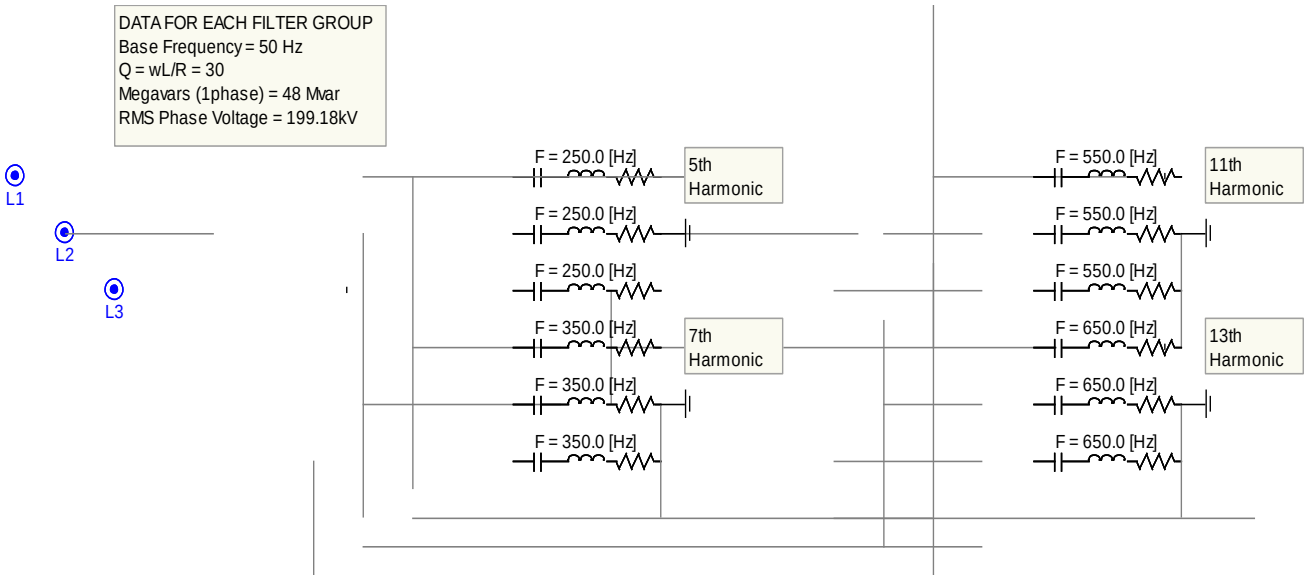


Fig. 29: Filter Circuit for Rectifier

Calculation for Filter Circuit

$$Q = P * \tan(\varphi)$$

$$\varphi = \arccos\left(cos(\alpha) - {}^{u_K}/_2\right) = \arccos\left(\cos(15°) - {}^{0.18}/_2\right) = 28.845°$$

$$Q = P * \tan(\varphi) = 1000MW * \tan(28.845°) = 550.78\ Mvar$$

For the purpose of filtering the 5th,7th,11th and 13th harmonic, the following approximate calculation is done

$$Q_{Filtergroup_{1Phase}} \approx \frac{Q_{Filtergroup}}{3} \approx \frac{Q}{4}$$

$$Q_{Filtergroup} \approx \frac{Q}{4} \approx \frac{550Mvar}{4} \approx 140Mvar$$

$$Q_{Filtergroup_{1Phase}} \approx \frac{140\ Mvar}{3} \approx 48Mvar$$

As mentioned before, all values that are not explicitly shown aside the hardware parts in the model, remain at the previously adjusted values that are visible in the figures of the foregoing stages.

For a better overview of the closed loop control circuit, it is split in its different parts.

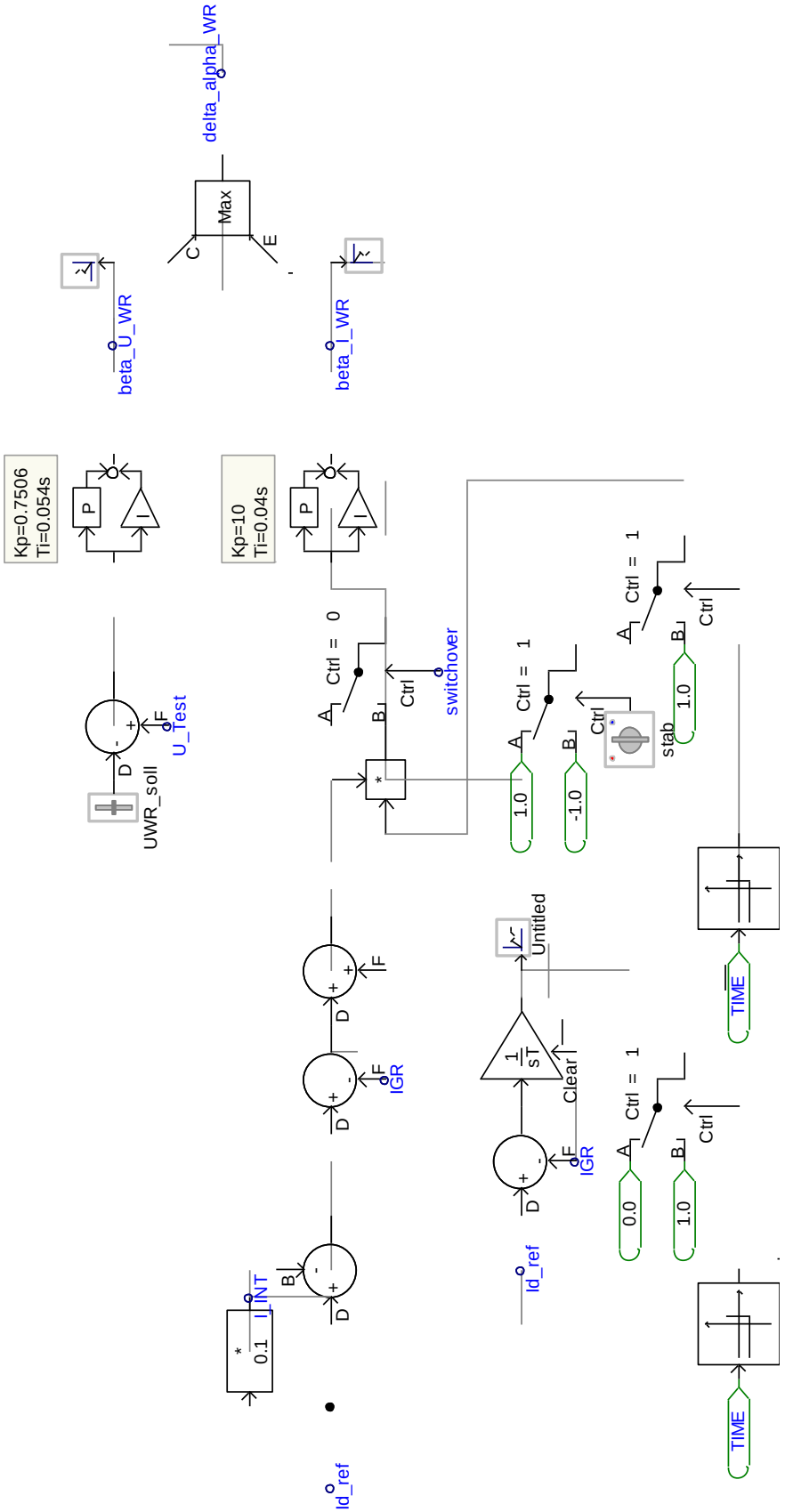


Fig. 30: Inverter Control

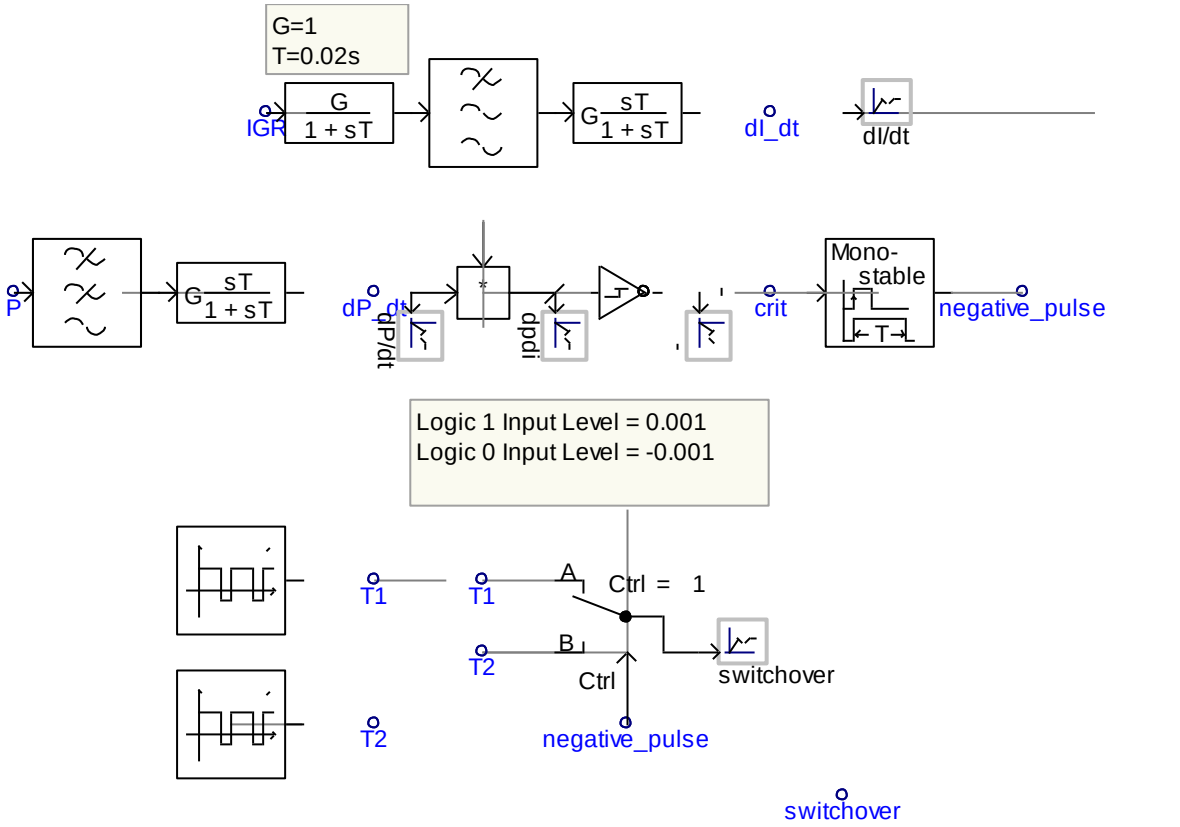


Fig. 31: AVS Mechanism

Regarding the AVS Mechanism 2 differences are introduced: the switching borders of the hysteresis are symmetrical now and a new real pole filter has been implemented. The new transfer function became mandatory to filter out the harmonics from the DC current.

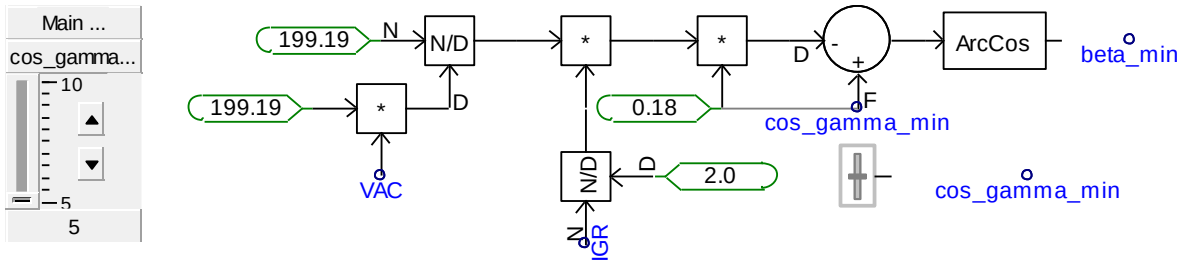


Fig. 32 Gamma Min Control

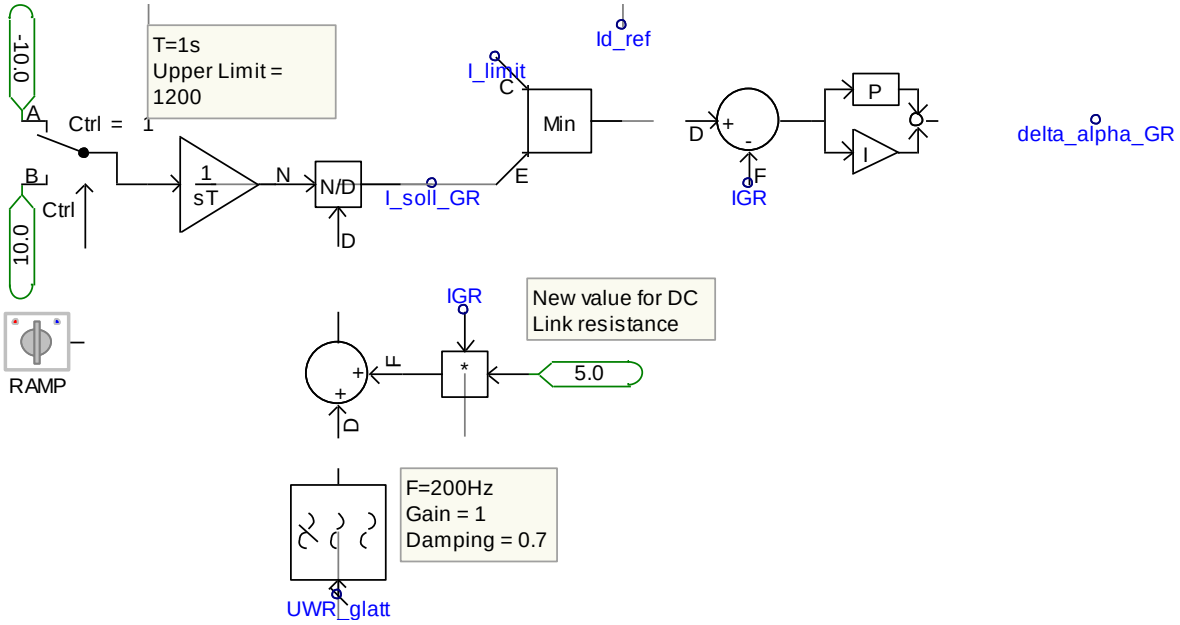


Fig. 33: Rectifier Closed Loop Control

Results

The following results of this final stage of the PSCAD/EMTDC digital simulations represent a comparison of VDCOL and AVS and are based on a previously performed test scenario that was done in collaboration with the first examiner of this work.

Starting the power ramp from 900 MW (Fig. 34, Trace 4) the nominal power of 1000 MW is adopted at 20 sec. Then DC current I_{GR} (Fig. 34, Trace 3) and DC voltage U_{WR_glatt} assume their rated values. Here the inverter DC voltage U_{WR_glatt} (Fig. 34, Trace 1) is shown which - at nominal DC current - is by 10 kV lower than the rectifier DC voltage due to the voltage drop across the DC line resistance.

The AC terminal voltage (Fig. 34, Trace 2) at the rectifier is 1 p.u. (345 kV) at nominal DC current.

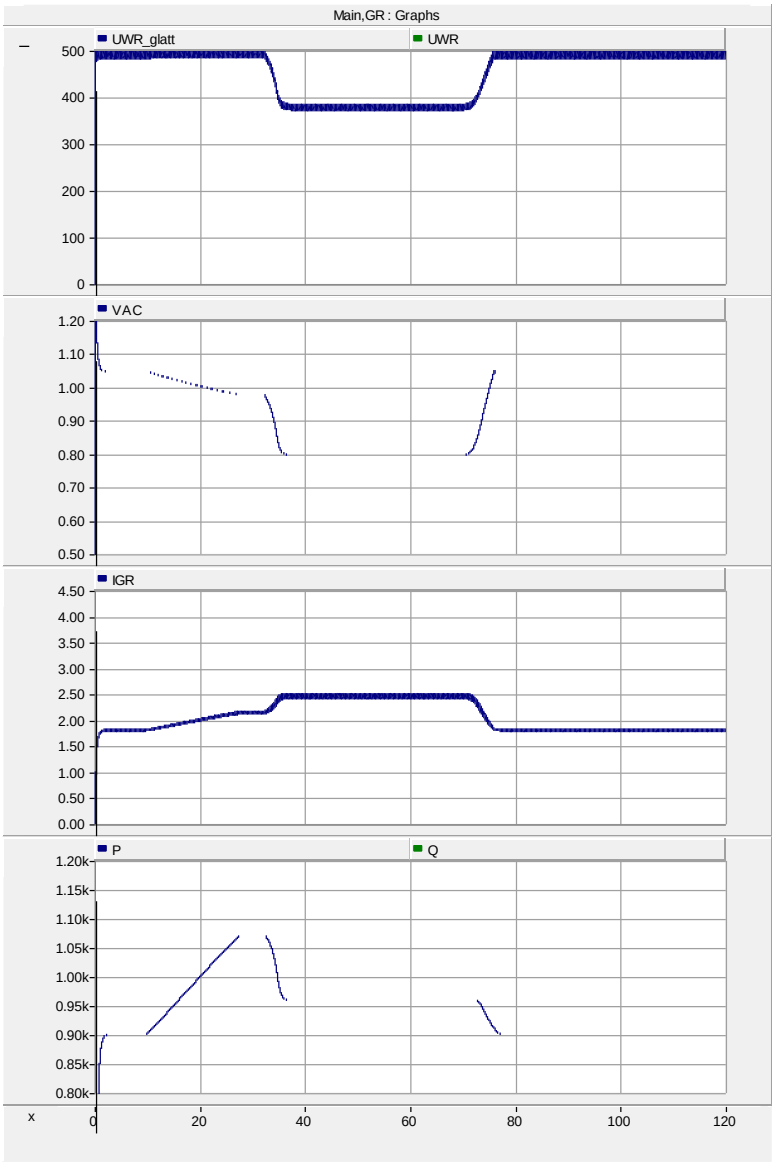


Fig. 34: VDCOL Graphics

As long as the DC voltage can be controlled – i.e., as long as the rectifier firing angle does not hit its lower limit of 5 deg – the current grows in linear proportion to the DC power. When the lower firing angle limit is reached the inverter takes over DC current control according to the marginal current principle. The DC voltage which is normally controlled via the inverter firing angle can then no longer be maintained since the inverter has to control the DC current.

In order to compensate for the decreasing DC voltage the DC current grows increasing in turn the overlap angle of the rectifier. In connection with the current increase this increases the reactive power consumption of the rectifier with an accelerating decline of the AC grid voltage. The VDCOL function limits further decline but only after the nose of the PV characteristic of the rectifier is surpassed. Minimum AC grid voltage is here 0.8 p.u.; other VDCL calibration values yield other minimum values.

When the power order is ramped back (after t = 70 s) to its former lower value the operating point returns to the upper branch of the PV curve. Finally the original operating point from the beginning of the test is resumed.

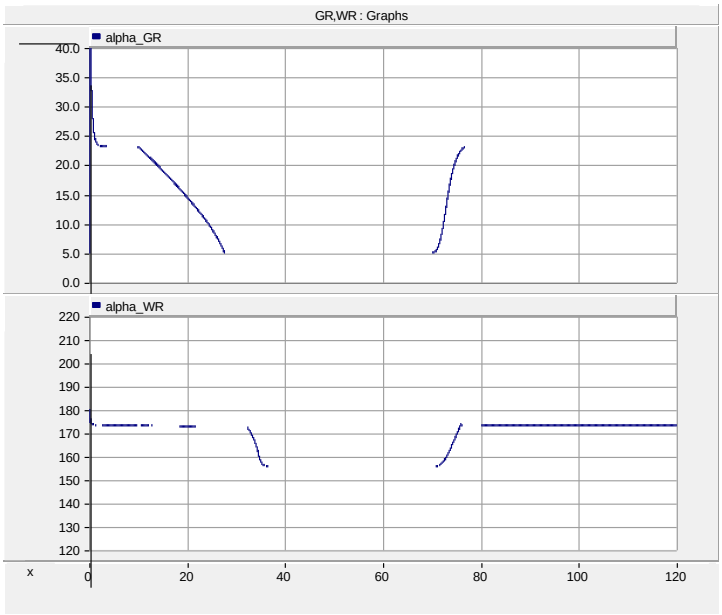


Fig. 35: Firing Angles

When the rectifier angle ($alpha_{GR}$) hits its minimum value there is a handover of current control between rectifier and inverter in accordance with the marginal current control principle. When the rectifier AC grid voltage returns to normal the rectifier assumes again current control and the inverter DC voltage control via the firing angle of the inverter ($alpha_{WR}$).

Fig. 36 shows the important PV-diagram that permits to judge whether our system is stable in the steady state or not. There are two branches the upper one of which is stable and the lower one of which is unstable (for the normally applied control loop sign).

There are two branches the upper one of which is stable and the lower one of which is unstable (for the normally applied control loop sign).

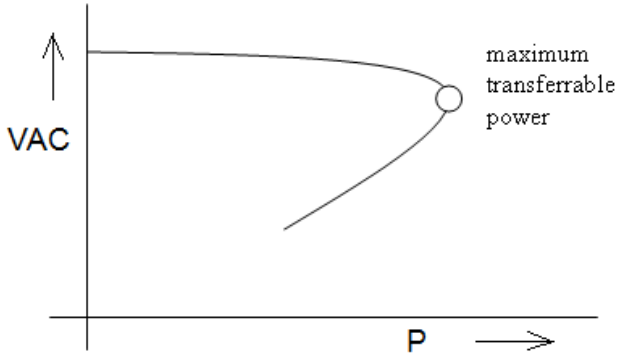


Fig. 36: Theoretical PV-Curve

The maximum power point (marked with red dot) separates the stable and the unstable regions. On the upper branch the DC current rises in proportion to the DC power (x- Axis). The AC terminal voltage (y-axis) declines accordingly. When the maximum power point is surpassed the DC current continues to grow but the DC power declines. The AC terminal voltage collapses but the collapse is halted through the VDCOL function. VDCOL does, however, not recognize that the system has passed the stability border and that the system is operating on the lower branch of the PV-curve.

While this effect of VDCOL is not really satisfying it has to be noted that If DC current limitation through the VDCOL function would not take place at all, a total voltage collapse and power loss of the HVDC system would occur. With VDCOL the HVDC transmission system is saved to some degree but the influence of the low AC voltage on the rest of the power system can have further detrimental effects. E.g., asynchronous machines either consuming or generating real power (wind turbines) would deteriorate the whole situation.

Now we take a look at how the automatic voltage stabilizer (AVS) manages the situation of reaching the power transfer limit.

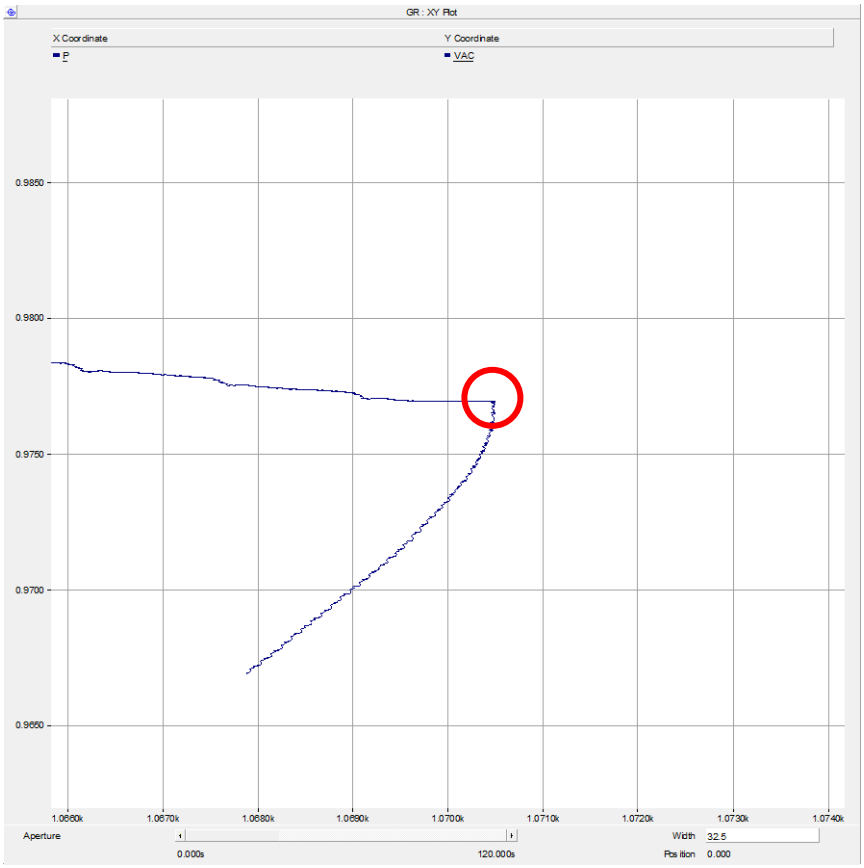


Fig. 37: Experimental PV-Curve VDCOL

The starting conditions are the same as above. The power ramps up and it reaches the maximum power point. There it stays while revolving with small swings around the maximum power point.

In contrast to VDCOL no voltage collapse takes place. The AC terminal voltage is kept within the normal voltage range not causing any problems for any other eventual equipment connected to the grid.

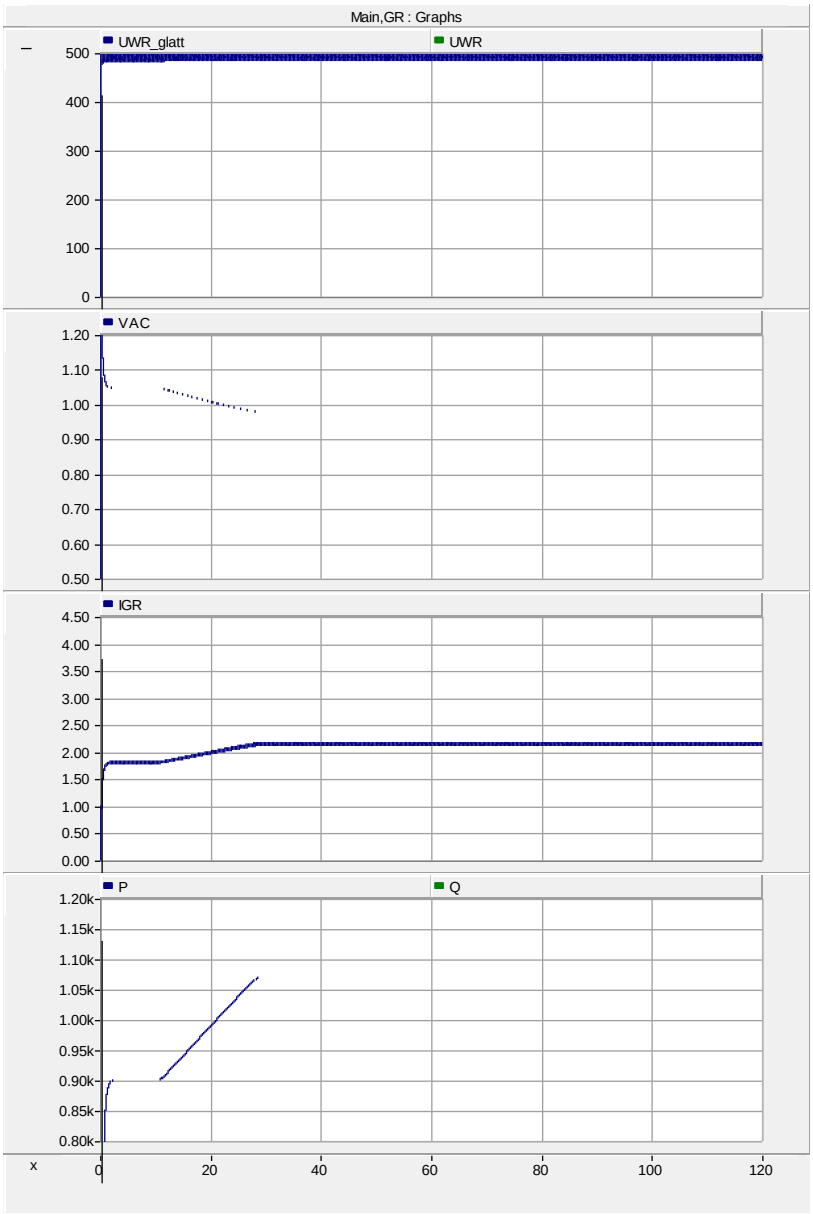


Fig. 38: AVS Diagram

But because the AC voltage of the rectifier is not pulled down as done with VDCOL the DC voltage does not experience this sudden decline (as with VDCOL).

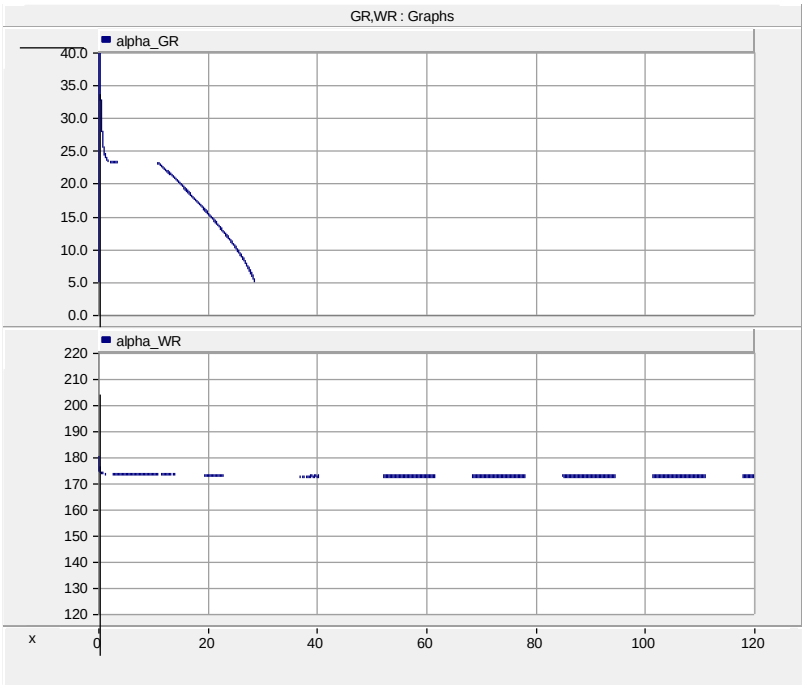


Fig. 39: Firing Angles

How the AVS stabilizes the operation can be recognized from the PV-Curve shown in Fig. 40 (y-axis: V_{ac} ; x-axis: P_d).

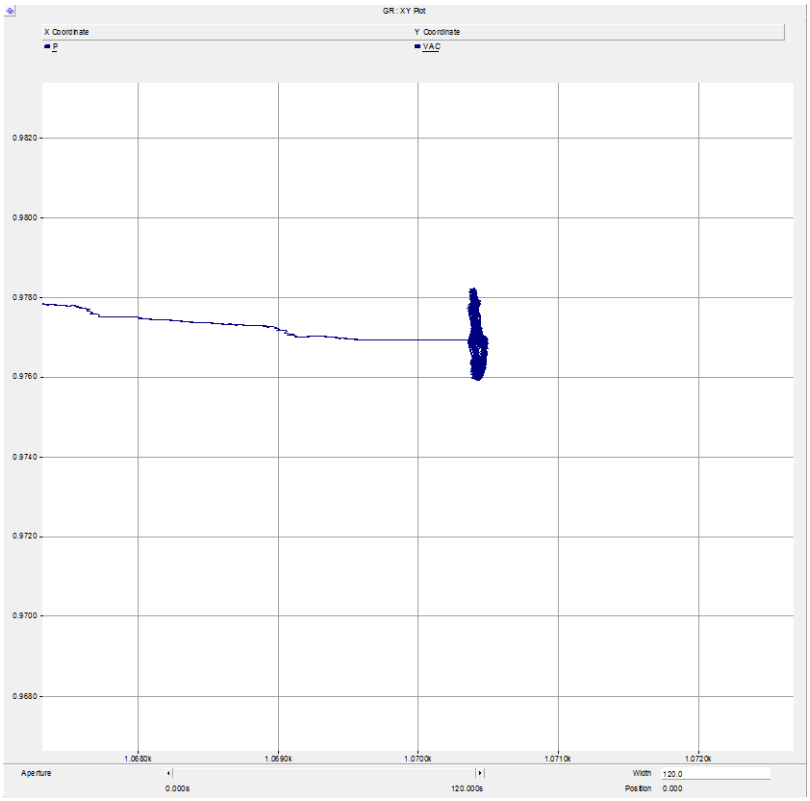


Fig. 40: PV-Curve AVS

The AVS recognizes the transition over the maximum transferable power (MTP) point and keeps the system at this point. Actually the operating point revolves around the MTP point and keeps in this way the system from sliding down on the lower unstable branch of the PV-curve.

2.2.1.6 Cigré Benchmark Model

The preparing stages of this project are completed by now, and we take a closer look at the Cigré Benchmark Model for HVDC Controls. The main data are already shown in chapter 2.1.1. In this chapter rather a detailed view of the implementation of the AVS in the inverter control subsystem is illustrated.

For better understanding of the later simulation results that are compared with each other, the rectifier and inverter grid are explicitly shown here, to clarify the test environment. The following figures show the only modification in the default Cigré Benchmark Model.

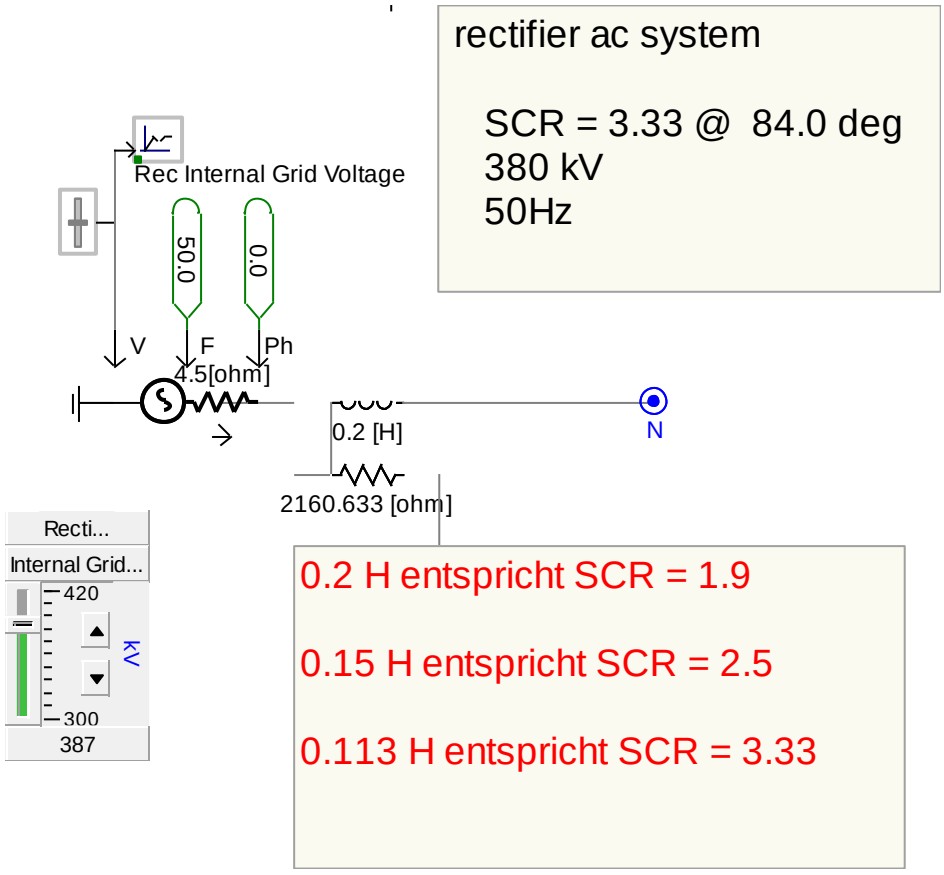


Fig. 41: Rectifier AC System

Which specific test case, i.e. which SCR is chosen for rectifier and inverter is marked for each case in the comparative simulation results in chapter 3.

Due to the imense size of the inverter control subpage, it's embedded as in object at this point.

Inverter_Control.jpg

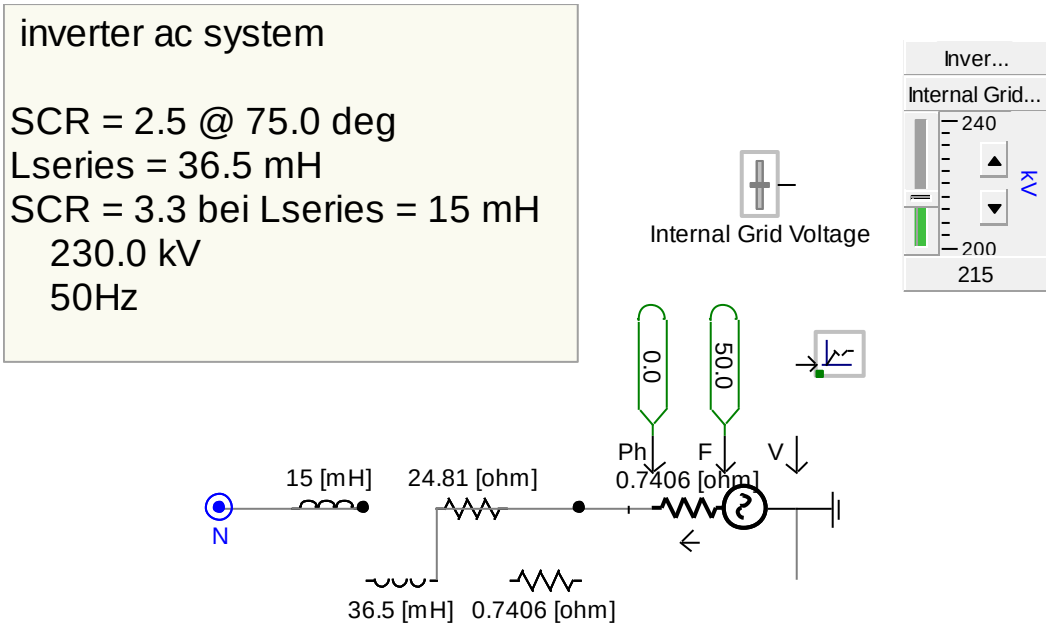


Fig. 42: Inverter AC System

On the following pages a detailed description of the parts that were enhanced within the inverter control are inlustrated.

It should be mentioned that only the henceforth illustrated add-ons are important. All other mechanism, that are not part of the original model are simply embedded for test purposes

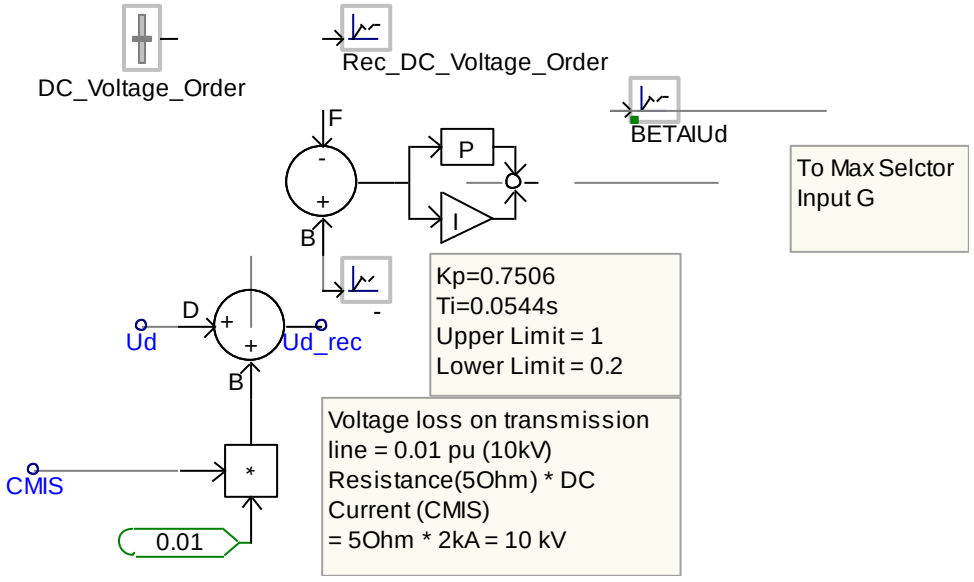


Fig. 43: Voltage Control Implementation

Shown in Fig. 43 is the voltage regulation, which is embedded in the inverter control circuit. The default model uses the “old-fashioned” gamma regulator to control the DC voltage. Constant extinction angle control is detrimental for voltage stability and, therefore, no longer used in installations. Nowadays DC voltage

control via the inverter is usual and therefore, the PSCAD models was changed accordingly. This allows then a comparison with the SimPowerSystem model as done in the next chapter.

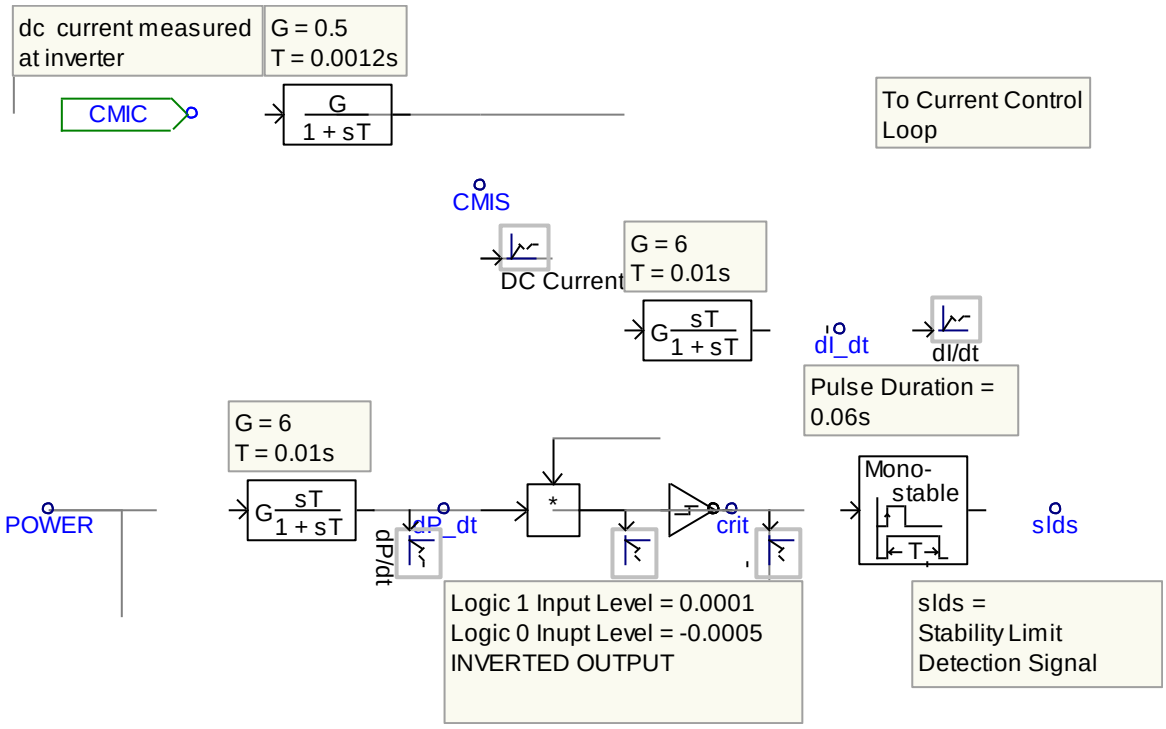


Fig. 44: AVS

Fig. 44 shows the main part of the AVS. Now the point is reached to explain its method of acting in detail. The best explanation is definitely with the help of the previously introduced PV-Curve (Fig 45).

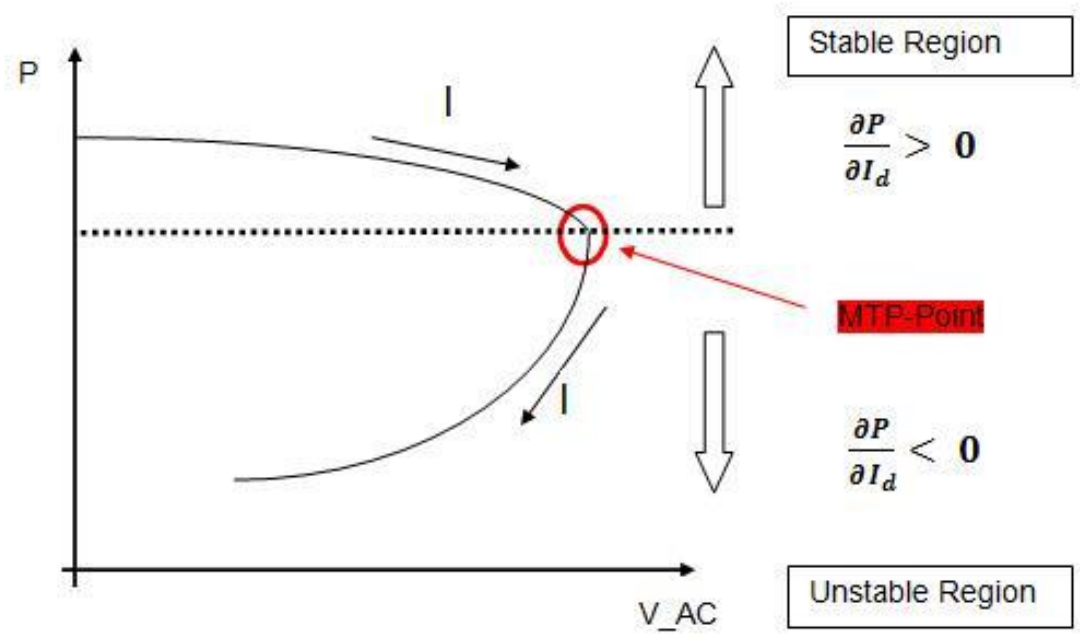


Fig. 45: PV-Curve

In Fig. 45 we can divide the PV-Curve into two regions, in the upper branch being the loci for stable operating points and the lower branch not permitting stable operation with the normally applied power control loop sign.

We see that a change in power comes along with a change in DC current. On the upper branch DC power increases with DC current, on the lower branch DC power decreases with increasing DC current. This provides the possibility to detect whether the operating point lies on the upper or on the lower branch by forming the quotient $\frac{\partial P}{\partial I_d}$.

The quotient $\frac{\partial P}{\partial I_d}$ cannot be measured directly but we can measure the derivatives with respect to time $\frac{\partial P}{\partial t}$ and $\frac{\partial I}{\partial t}$. Exactly this is done with the corresponding transfer functions in Fig. 44.

In the next step these two quotients are multiplied:

$$\frac{\partial P}{\partial t} * \frac{\partial I}{\partial t} = \text{crit}$$

If only one of the derivatives with respect to time becomes negative, which indeed occurs for the power with respect to time when moving along the lower branch of the VP-curve, the product “crit” becomes negative. If both derivatives with respect to time are either positive or negative which happens to be when the operating point moves along the upper branch the product is positive, so we know that the operating point is on the upper branch.

The value of “crit” is passed to a hysteresis buffer that triggers the monoflop that in turn sets the stability limit detection signal “slds”.

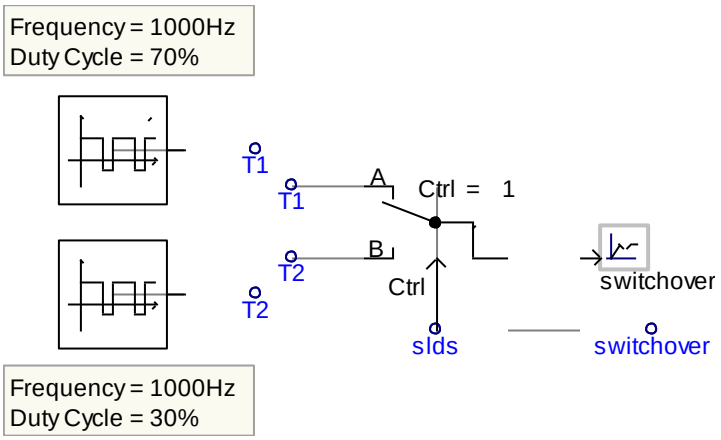


Fig. 46: Generating Switchover

Fig. 46 illustrates how the “slds” generates a pulsed signal named “switchover”, which is the actual switch that shifts the operating point back to the upper branch by reversing the sign of the power control loop.

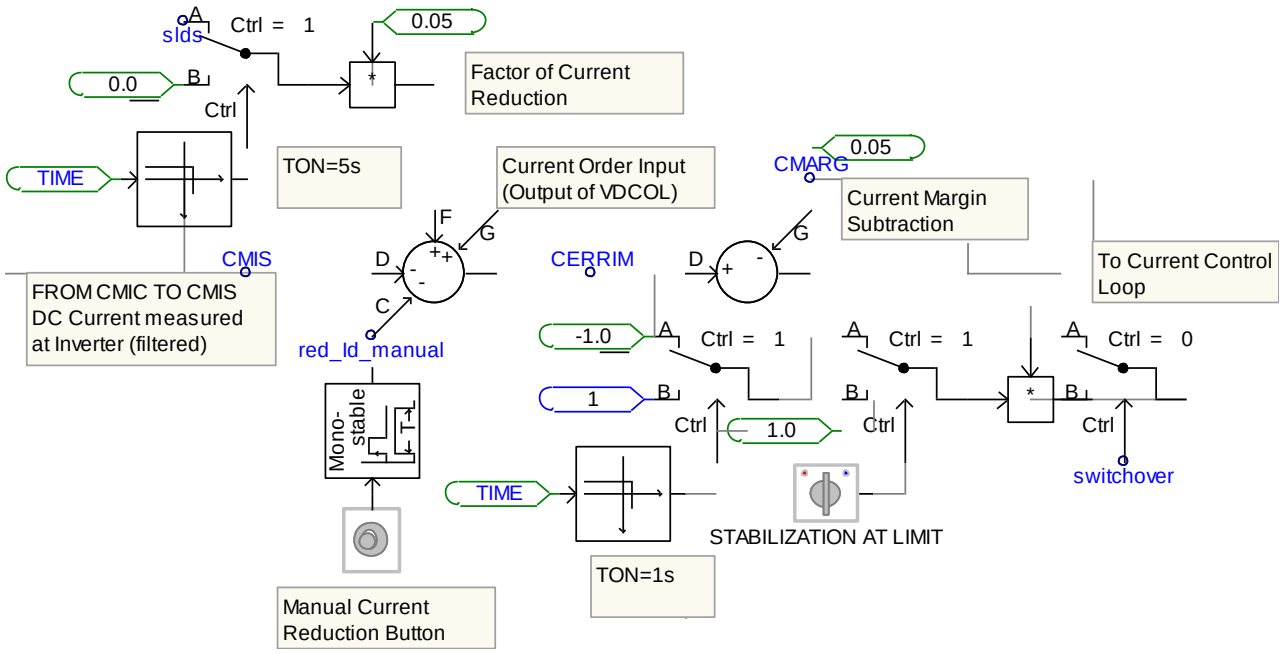


Fig. 47: AVS Taking Action in Closed Loop Control

To ensure a safe oscillation around the MTP-Point, the two signal generators are embedded in the circuit. This means, with 70% the operating point is pushed back up while 30% of the cycle is used to let it fall down to the lower branch again. The displayed principle ensures a safe oscillation around the MTP-Point. The frequency of the generators are purposefully selected with the given magnitude.

Fig. 47 clarifies the working principle of the previously illustrated switchover signal. First, the two time-based switches can be disregarded, again they became necessary in order to power up the system to nominal condition without a disturbance by the AVS. If the AVS is switched on (STABILIZATION AT LIMIT switch in upper position), the pre-sign of the further closed loop control for the current regulation will be multiplied by -1 causing the current to change from increase to decrease. This leads the operating point back to the upper branch.

Taking a closer look at the first summing point, more precisely on the input “F”, shows an addition of a current reduction factor. This mechanism is necessary to ensure a “100%” safe AVS function. On the first sight, it may look strange, because the current should be reduced, in order to avoid a breakdown of the voltage, and therefore a subtraction should be part of the first summing point. BUT, because the plant sign is negative on the lower branch of the PV-Curve, the sign has actually to be positive to reduce the current.

Fig. 48 and 49 show that utilization of this signal as input “F” of the summing point in Fig. 47 guarantees stable operation immediately at the stability boundary

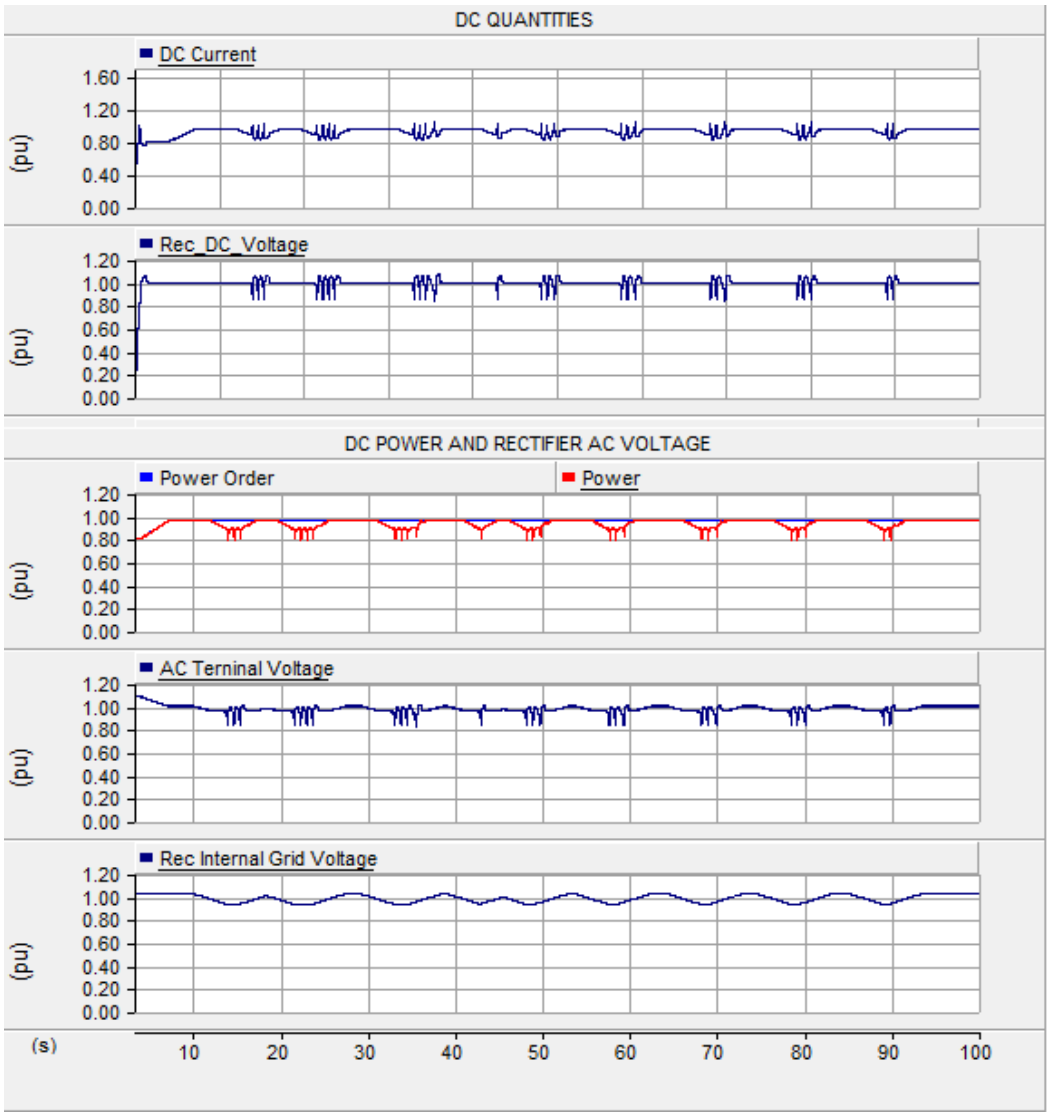


Fig. 48: Operational Quantities at Stability Boundary – safe operation

The next Fig. shows the various control signals with the following meaning:

Annunciator: annunciates that to the operator that the system operates at its stability limit

dI/dt derivative of DC current with respect to time

dP/dt derivative of DC power with respect to time

crit: output of the threshold block indicating locus of operation on the PV-curve

dpdi: product of both derivatives

slds: binary stability limit detection signal used for sign switching

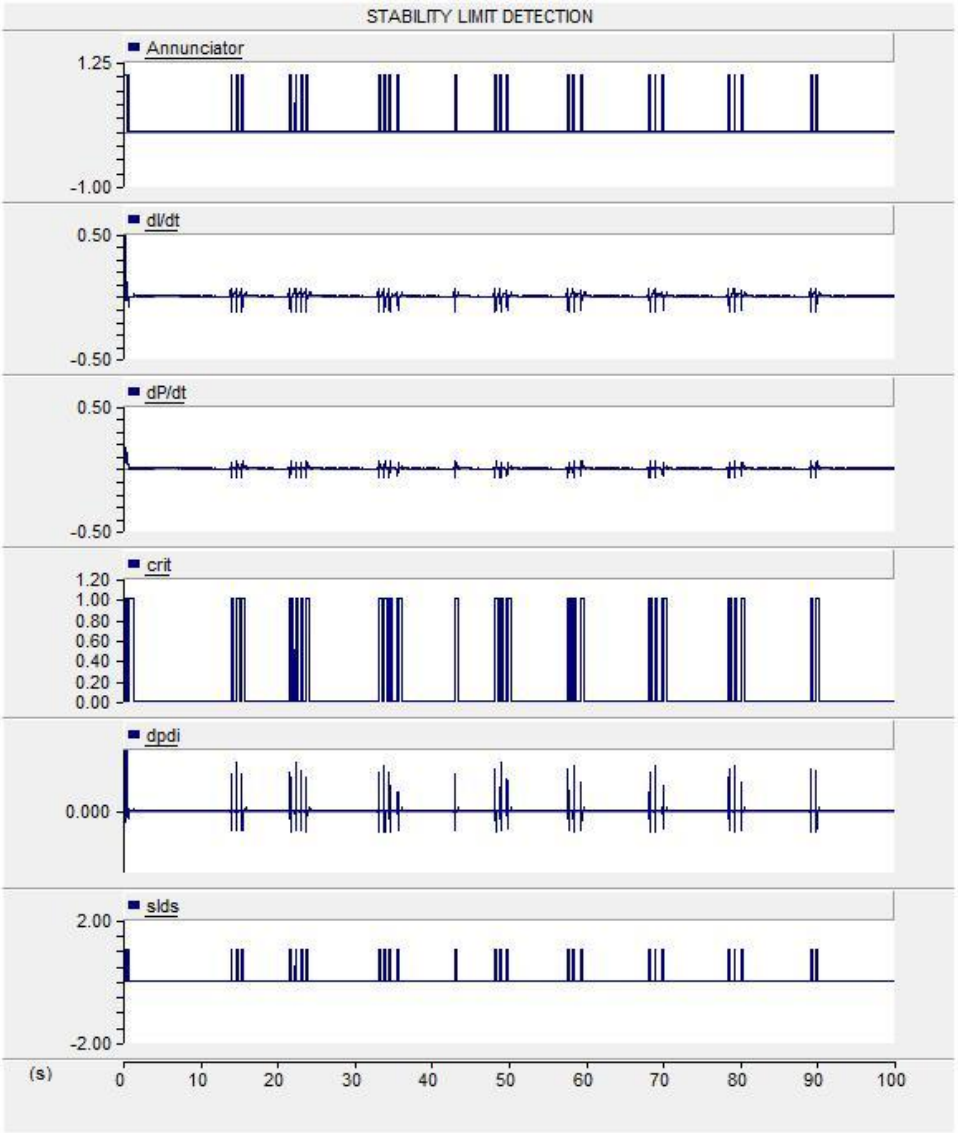


Fig. 49: Control Signals at Stability Boundary – safe operation

The upcoming part shows another method of AVS operation. Instead of an operation with a revolving operating point around the stability border, this mechanism reduces the power order automatically with the impact of a removal from the stability boundary towards the stable region.

The working principle is quite easy to understand. Transgression of the stability boundary is recognized by the AVS and further steps are initiated.

The “slds” signal triggers the monoflop that in turn reduces the power order by a defined value. In this case the power is reduced by 10% to a new value of 0.9 p.u. For the test purpose this is a fixed value. In [XII] this is a value adapting itself to the maximum transferable power level.

XII PCT/EP2010/055076, Method and Apparatus for Automatic Network Stabilization in Electric Power Supply System using at least one Converter

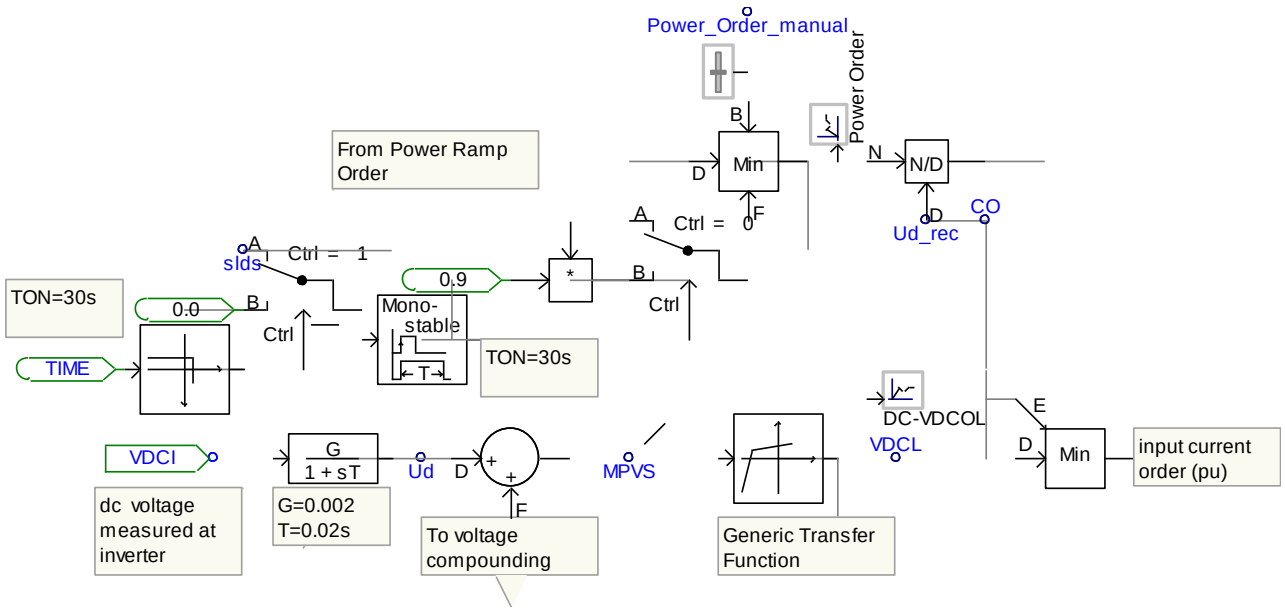


Fig. 50: Power Reduction Mechanism

Another important fact, which is illustrated in Fig. 50, is the DC based VDCOL. This is indeed not the smartest way, due to the fact that AC voltage sooner declines than the DC voltage. However, for a weak AC grid with an SCR of around two there is only a very small AC voltage decline before the voltage collapses. That is, the difference whether using AC voltage dependent or DC voltage dependent DC current order limitation is used, is actually marginal and not decisive for the functioning and the performance of VDCOL.

The data table of the DC based VDCOL table can be found in chapter 3.1.

2.2.2 AVS Implementation in RT

A complete description of the Cigré Benchmark Model can be found in the appendix. For a basic understanding the chapter 2.1.2 should provide enough information.

Before an implementation of the AVS could be done some massive preparations of the Cigré Benchmark Model became mandatory.

The following chapters illustrate how the model has been modified and give a brief demonstration of how it works.

The problematic with SimPowerSystem is the fact that a model becomes highly confusing with the amount its complexity is growing. As already mentioned before, this is a big disadvantage of that specific application development system.

Therefore a complete system description is attached in the appendix that should help to abolish the inconsistencies that may occur in the upcoming chapters.

2.2.2.1 Adjusting the Closed Loop Controls

For sure it is a disadvantage if a system model is delivered with oscillations in the closed loop control circuits. Before an AVS implementation could take part in this project, the control circuits have to be adjusted.

Fig. 51 displays the challenge of a permanent oscillating control circuits. This problem is caused by the two weak AC grids, on the rectifier and inverter side. As previously mentioned, this is not a general problem of the model, but a problem of the adjustment of the regulators. As seen in the PSCAD models, with the right settings the system is working, despite of the weak AC grids.

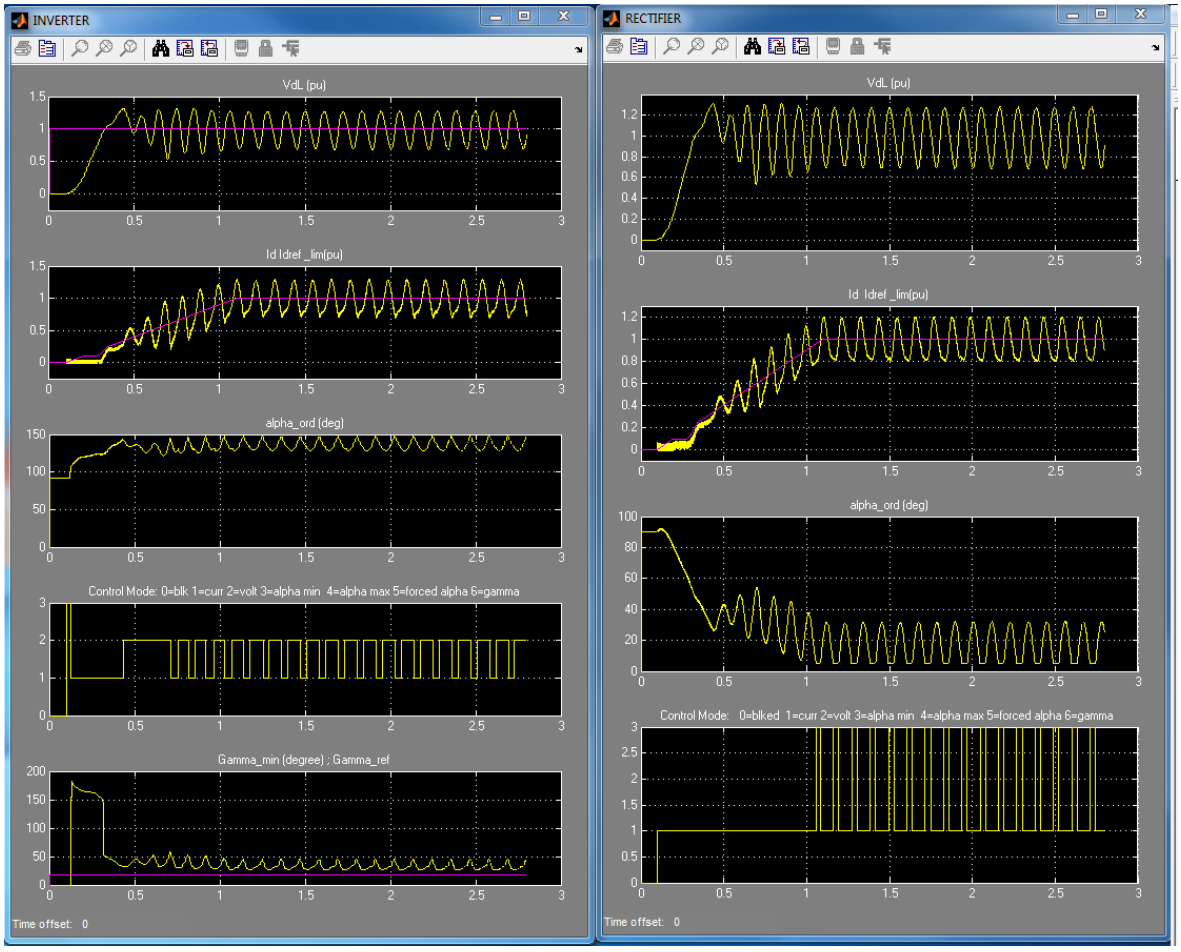


Fig. 51: Inverter and Rectifier Control Response

At this point, the default console is used to display the graphics. The left one illustrates the data of the inverter, while the right one illustrates the Rectifier. The traces display the DC voltage, DC current, alpha order, Control mode and for the inverter gamma min (from top to bottom). There is no detailed description, because it is not important at this point, important is the permanent oscillation, visible in the diagrams.

Fig. 52 shows the mask to set control parameters. However, the parameters set were not becoming active, they were overwritten.

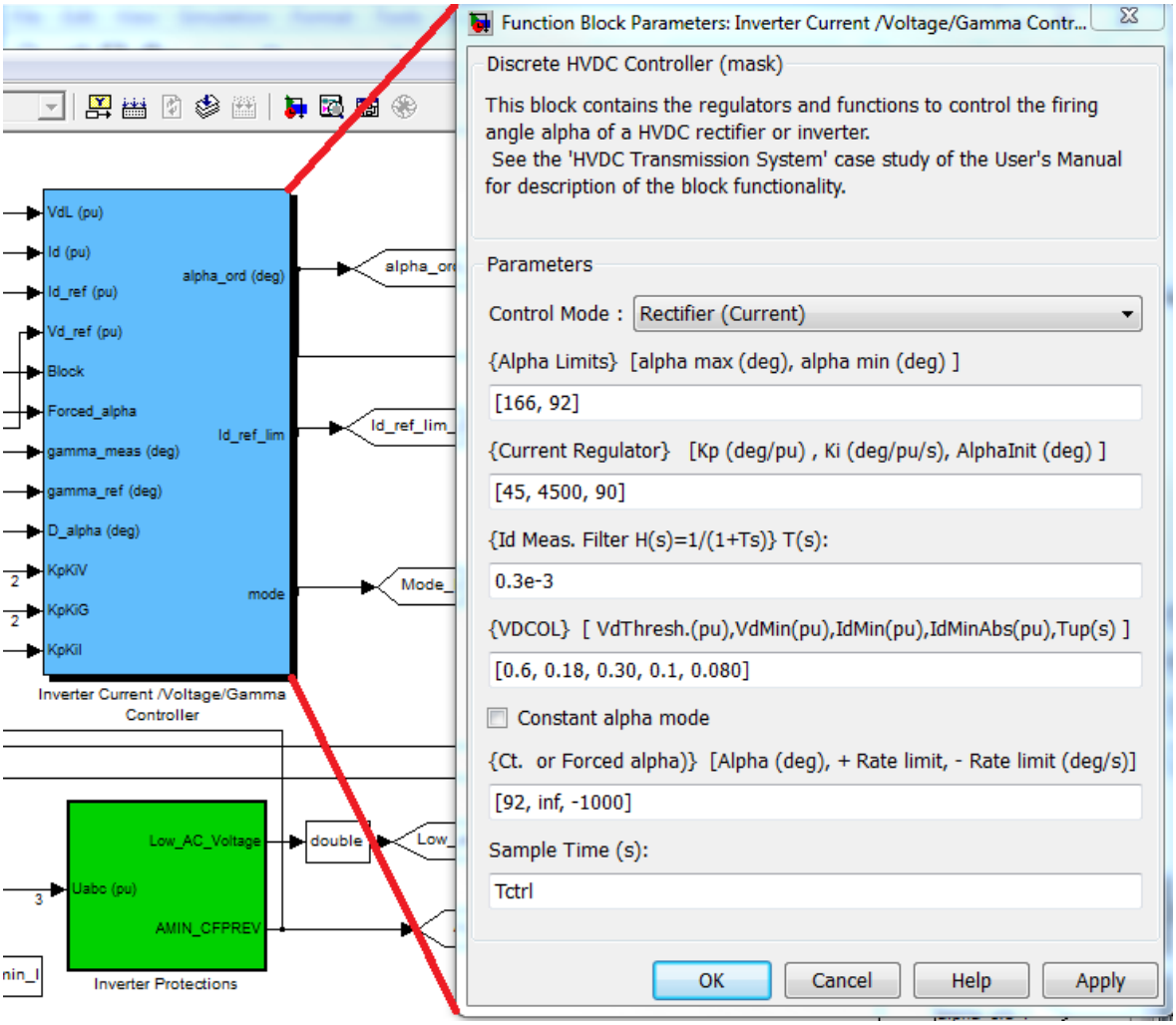


Fig. 52: Inverter Controls

But to ensure that system performs in real time all the input signals set up in the console module have to pass the OPComm block.

The console module runs asynchronously to the computation, done in the Opal RT simulator. All subsystem inputs must pass the OPComm block first, before any operation can be done to them.

This means that the values that were previously set up in the mask, were overwritten from those in the “ctrlset” box shown below in orange (Fig. 53).

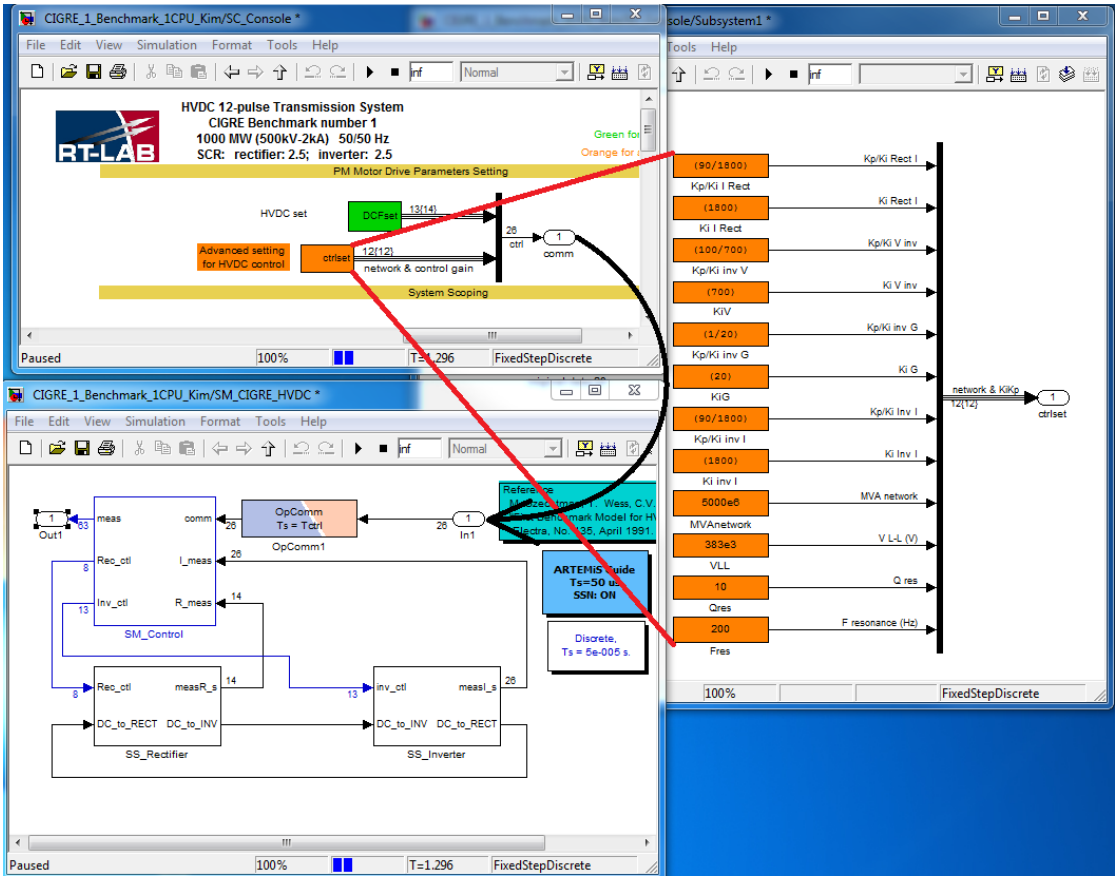


Fig. 53: Parameter Operation

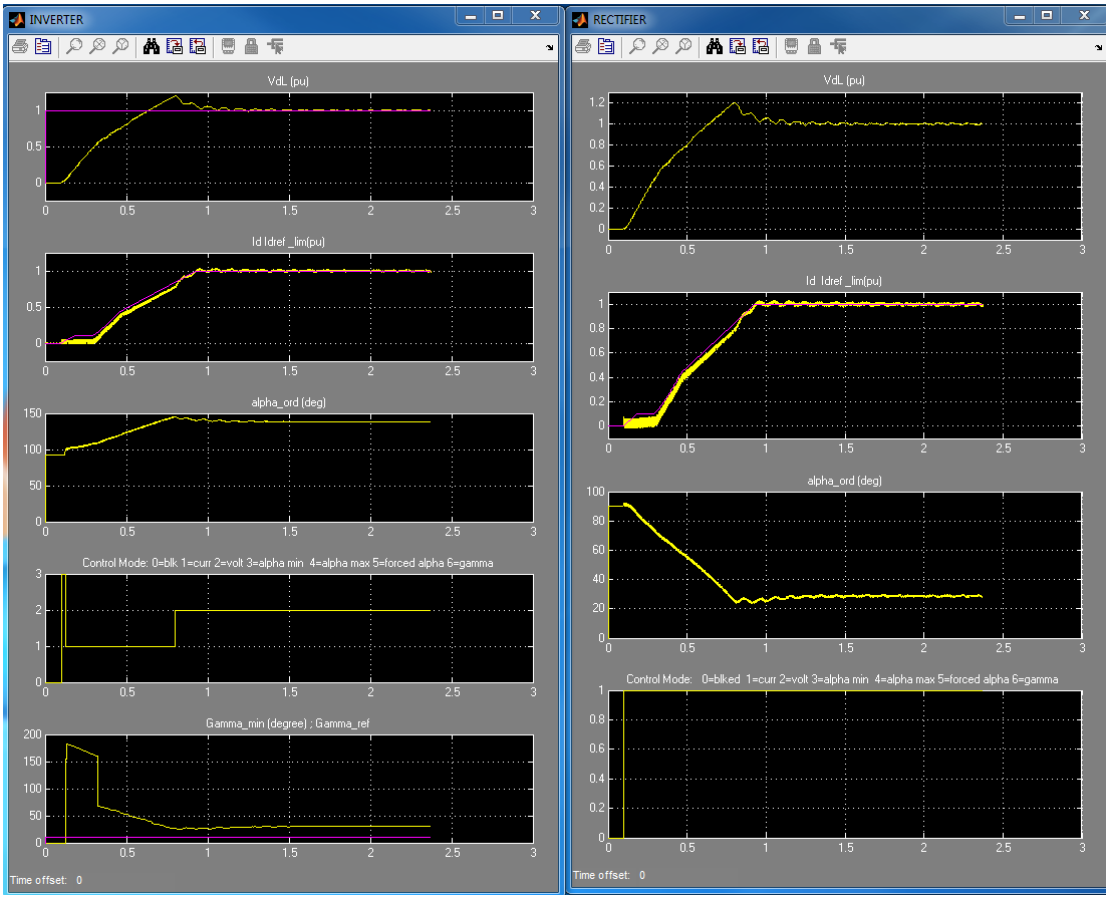


Fig. 54: Control Response with Adjusted Data

After calibration of the closed loop control data some better results could be obtained regarding the response of the system.

The adjusted data values of the controllers can be found in the appendix.

Problems appearing while calibrating the controllers:

- While in PSCAD the gain of the controllers is in [rad], SimPowerSystem uses [deg/p.u.]
- PSCAD uses the integral time constant to describe the behavior of the Integrator, whereas SimPowerSystem uses [deg/p.u./s].

This difference does not permit to directly adopt the controller parameters from PSCAD.

2.2.2.2 Adjusting Circuit to Nominal Conditions

After a suitable solution for the control mechanism was found, the circuit needs to be adjusted for nominal condition. And furthermore some manual controls were embedded to perform some value changes in order to test the behavior of the AVS and the system was enhanced with some measurements.

Some major problems occurred with the adjustment of the subsystems for the internal grid.

In fact variables can be used to set up the value of the internal grid voltage in such a model. But a “in the loop” change of the value is not possible.

Just for an initial value the internal grid subsystem adopts the value that was written into a variable.

A direct manual change in the parameter mask indeed take part while the simulation is running, but regarding a further real time simulation, this mask is not available anymore.

So a change of the library file was necessary to obtain a solution for an “in the loop” variation of the internal grid voltage (Fig. 55)

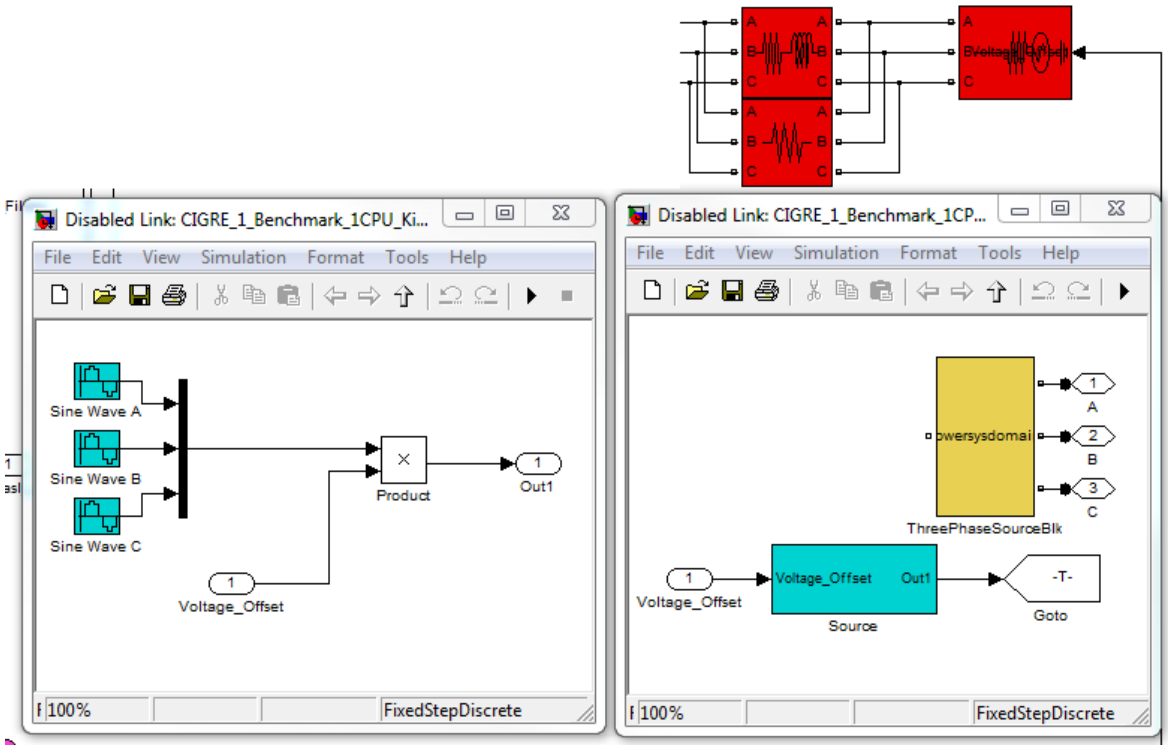


Fig. 55: Internal Grid Voltage Modification

2.2.2.3 Real Time Simulation Setup

After a working setup of the Cigré Benchmark Model was obtained in the SimPowerSystem environment, a conversion to a real time acceptable code became necessary.

As simple as that sounds a standard c code serves that task. The RT-Lab interface is used to generate that code and establish a connection to the OPAL RT servers. But any other compiler could be used for it instead.

First, the RT-Lab environment has to be configured and later build the c-code as shown in Fig. 56.

On the Execution tab, some basic adjustments have to be done. E.g., the software on which the server is operating, time constraints if wanted, etc.

A quite important point is the Real-Time simulation mode. More on that is written in the manual that is attached.

Fig. 57 shows the assignment dialog. There the hardware settings are made. If the model is separated in more than one subsystem there is the property to exclusively choose on which core this specific subsystem is computed in the later real time simulation.

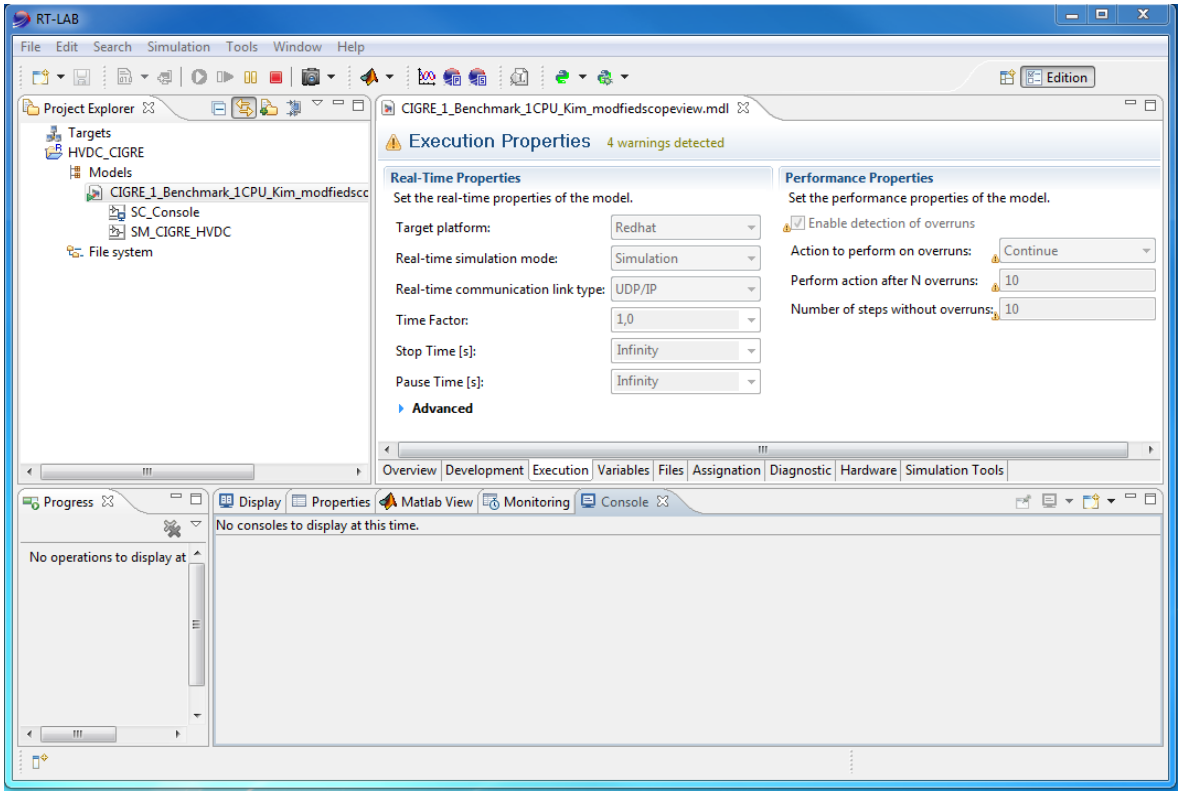


Fig. 56: Real Time Software RT-LAB

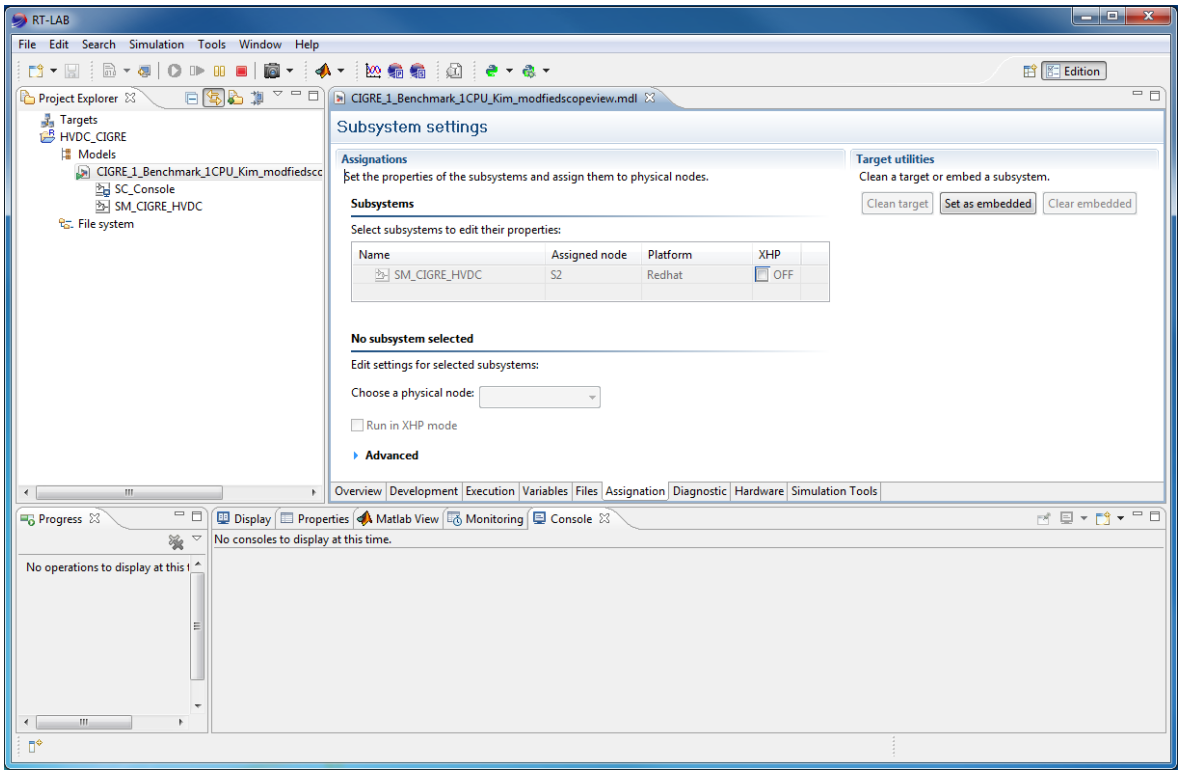


Fig. 57: Assignment Dialog

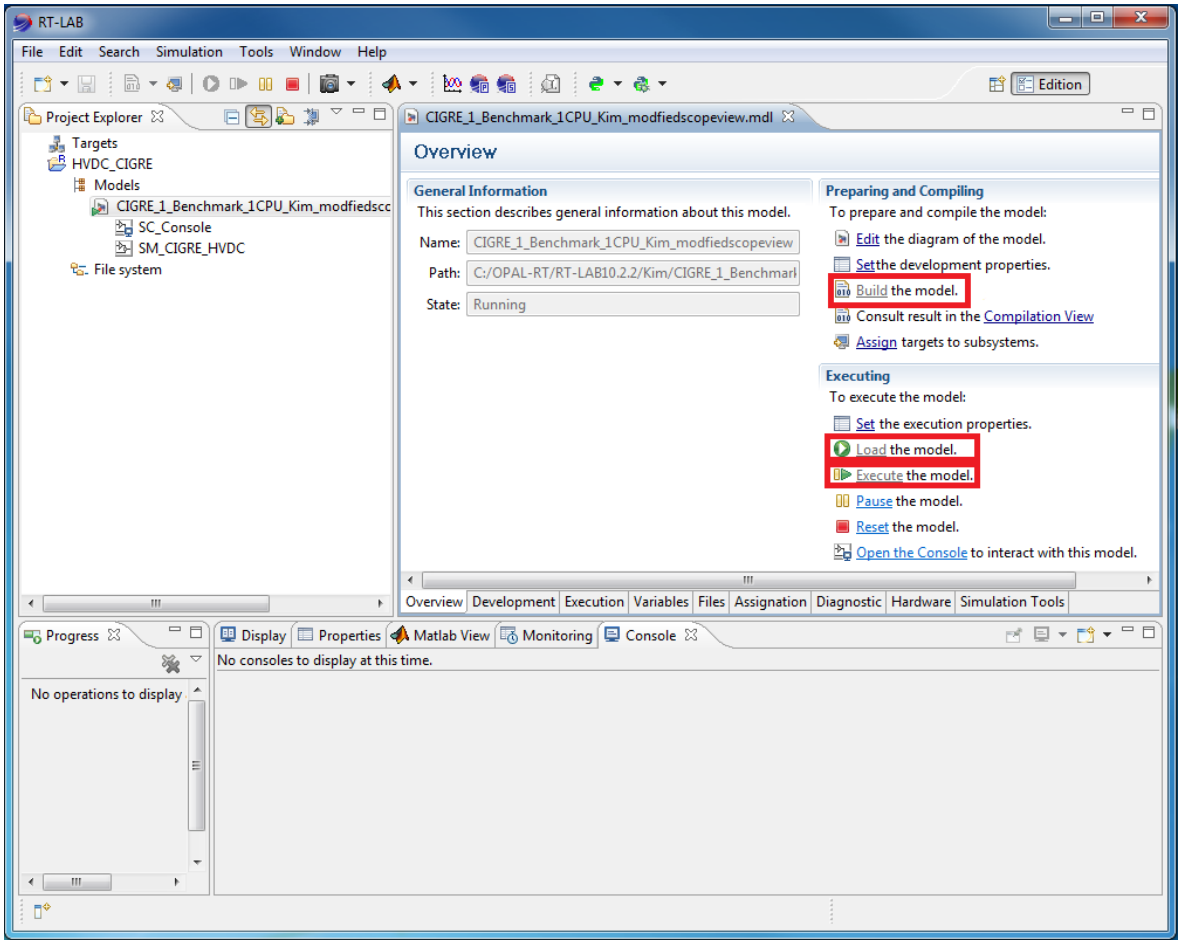


Fig. 58: Real Time Execution

After configuring the RT-Lab the final conversion is done.

- Build the model
- Load the model
- Execute it

2.2.2.4 Real Time Observation

After setting up the RT-Simulation, some test runs were done. Massive problems arose, caused by an unacceptable delay of the console.

Till today no real solution and no the origin of that problem has been found. Also the OPAL-RT support could not offer a suitable solution for the problem.

Neither a reduction of the scopes, that are visible in the console nor any reduction of the step-time, sample-time, etc. made an impact on the performance of the console subsystem.

But after checking with a special tool, served by the library of the RT simulator, the diagram below shows a perfect real time processing of the simulator, but not as a result in parallel to the simulation itself but through post processing.

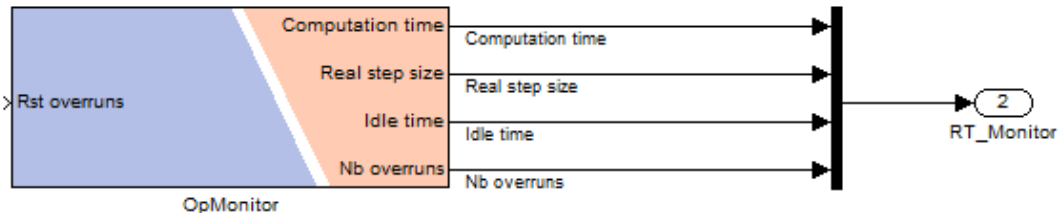


Fig. 59: Real Time Monitoring

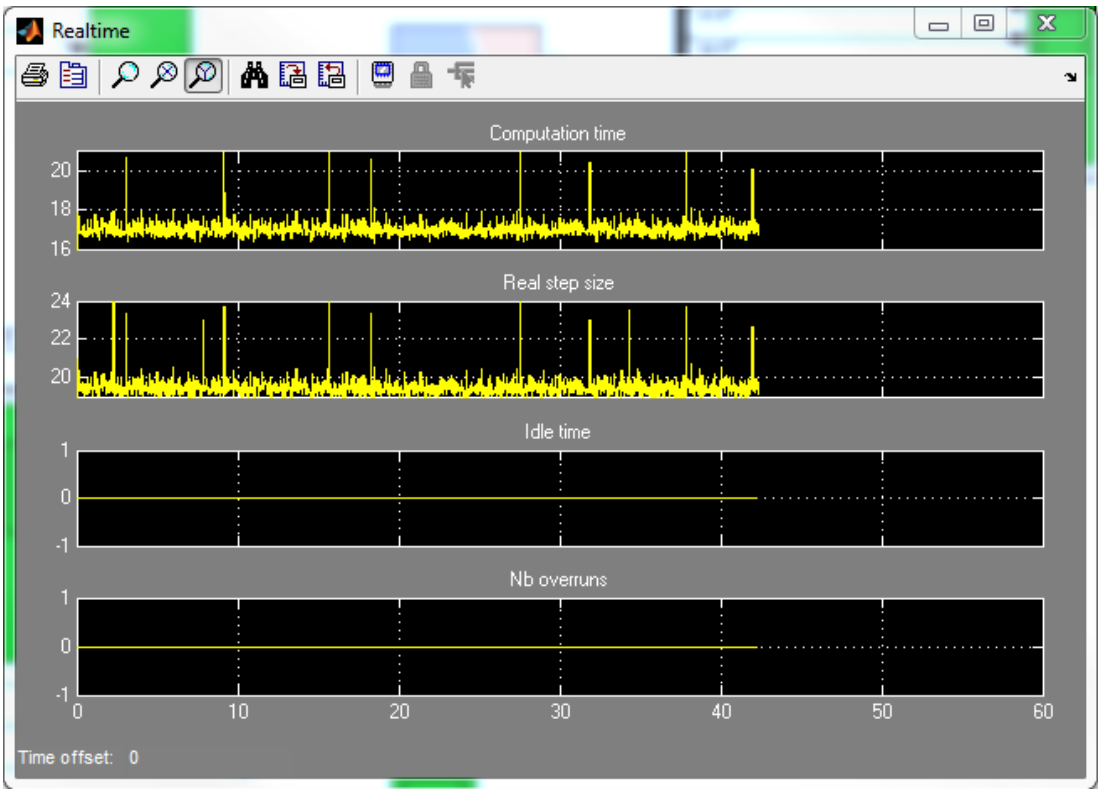


Fig. 60: Real Time Data

2.2.2.5 Current Margin Compensation/Discretization

To ensure a right working transfer of the current control, normally provided by the rectifier to the inverter, a calibration of the current margin is essential.

The same problems occurring while calibrating and optimizing the controllers took place here. The mask is the same for adjusting the values of the rectifier or the inverter. Sadly a change in the mask of the rectifier, even if the inverter is selected in the tab, does not mean that a change really makes an impact on the circuit.

In this very case, a change of the current margin in the mask of the rectifier leads the system to a whole collapse. And even a change back to the former value of that specific parameter doesn't set the system running again. A complete restart and new loading of the model, incl. shutting down Matlab is indispensable.

This special case occurs when exceeding the stability border of the transmission system. Again the final values of the current margin are found in the appendix.

Detailed information, regarding the State-Space stability is shown in the appendix at chapter 4.3 (Specific information provided on p. 23).

The solving system used by the OPAL RT simulator needs a discretized model to run in fixed-step mode. Therefore the later implementation of the AVS has to work with discretized differentiators.

2.2.2.6 AVS Architecture in SimPowerSystems

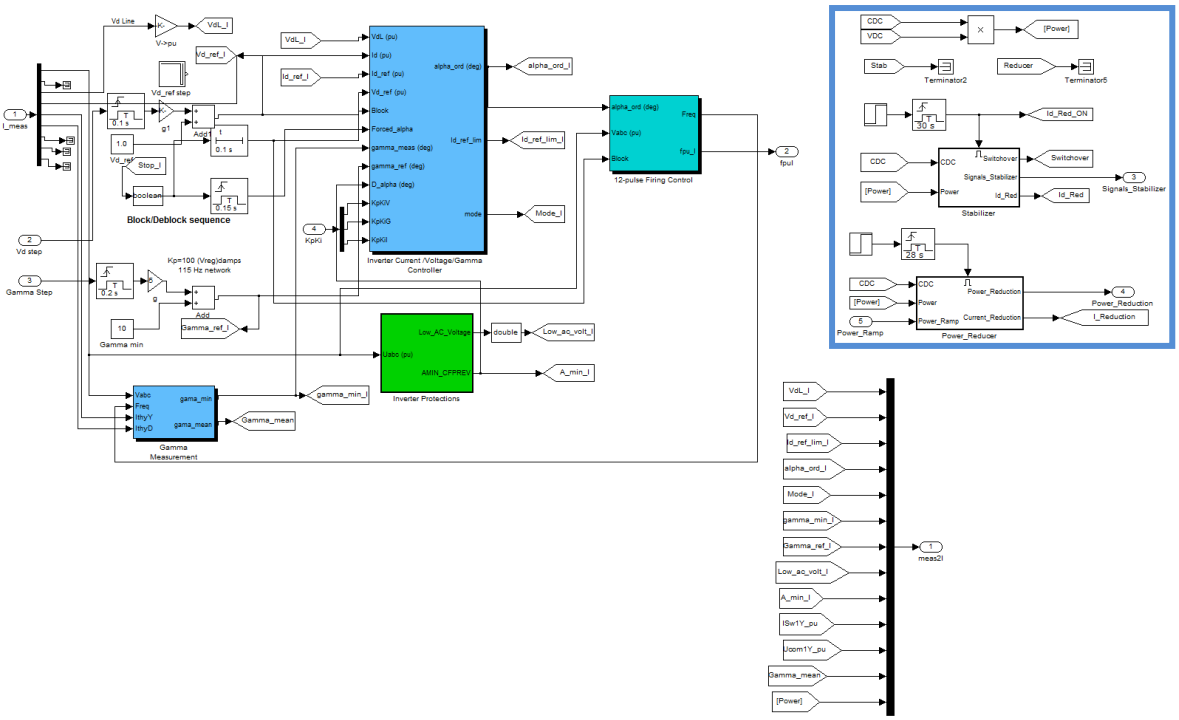


Fig. 61: Inverter Control

Fig. 61 illustrates the inverter subsystem control mechanism, where the AVS is implemented. Regardless the low resolution of the graphic should it just serve the task to show where the AVS in implemented. A detailed description of that specific subsystem can be found in the appendix.

In Fig. 62, we see the zoomed details of the embedded AVS in the inverter control subsystem (Fig. 61, blue box). The measured DC current (CDC) and DC voltage (VDC) are multiplied to get the power, transmitted over the DC link.

The subsystems for the stabilizer and the automatic power reducer are equipped with a switch to set them active or inactive. The stabilizer is switched on after 35 seconds and stays active for 30 seconds, while the automatic power reducer is switched on at 67 seconds and remains active for 28 seconds. When the stabilizer is switched on, the Id_Red_ON function is set on too.

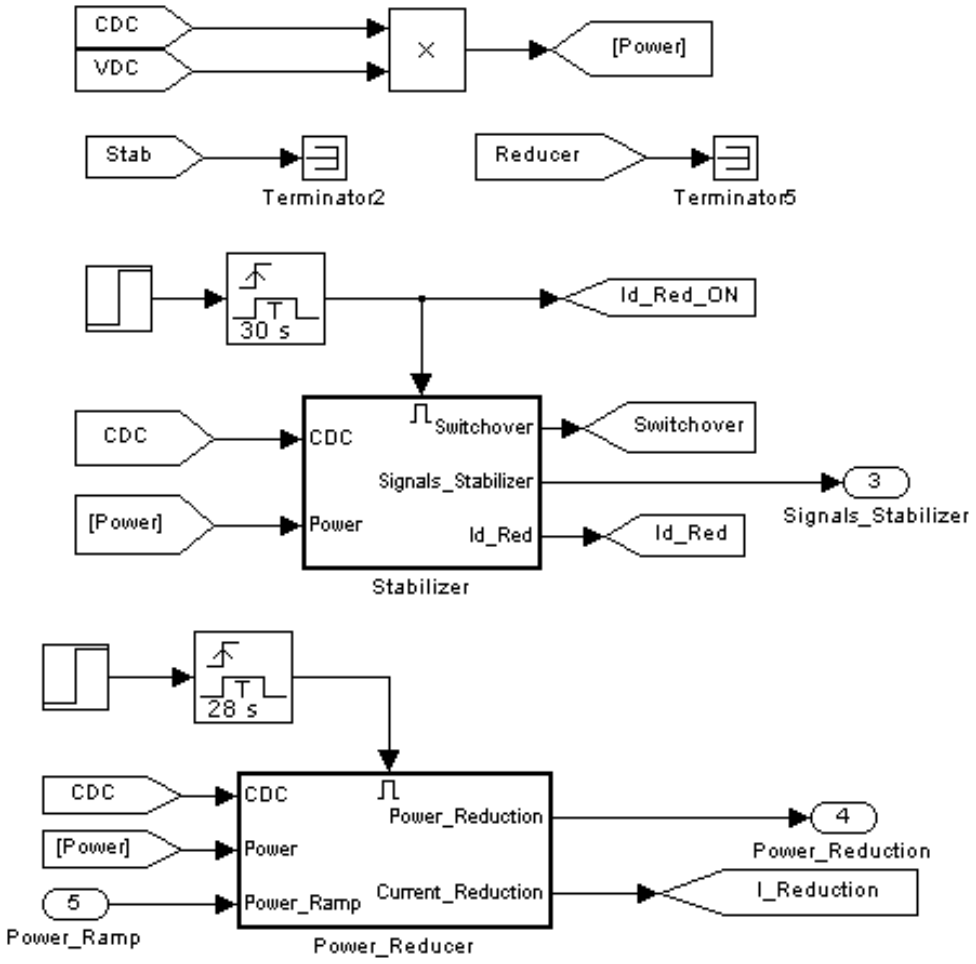


Fig. 62: AVS Implementation

To avoid an operation at the stability boundary with the accompanying swings around the MTP point a power order reduction triggered by the aforementioned “slds” signal is necessary. This feature is also needed when rotating synchronous machines pull the operating point over the MTP point down the lower branch of the PV-curve. Then the revolving automatism around the MTP point is hardly to maintain as parallel investigations performed at the same at FH Frankfurt have shown.

In parallel to the reduction of the power order a signal decreasing the DC current has to be issued: Without such a negative current pulse power order reduction would cause the operating point even more to slide down the lower PV-curve. This principle of a current reduction, to ensure a safe operation around the MTP-Point, is already mentioned and explained in chapter 2.2.1.6.

Fig. 63 shows the detailed working principle of the AVS. Also illustrated, the Id_Red command derived from the occurrence of the stability limit detection signal. On the basis of Fig. 60, you can see the discretized differentiators with discrete 2nd order low-pass filters with a damping factor of $\mathrm{Z} = 0.707$, responding to the following equation: $Q = {}^{1}/_{2 * \mathrm{Z}}$

Data that is not especially mentioned here remains at the same values as previously described in the PSCAD model.

The OpWriteFile subsystem, (Fig. 60, Data_Stab) is a special real time computation element, which is not part of the default SimPowerSystem Toolbox. But it is used here, to write the data of defined parts of the system into a file to allow a later observation of it.

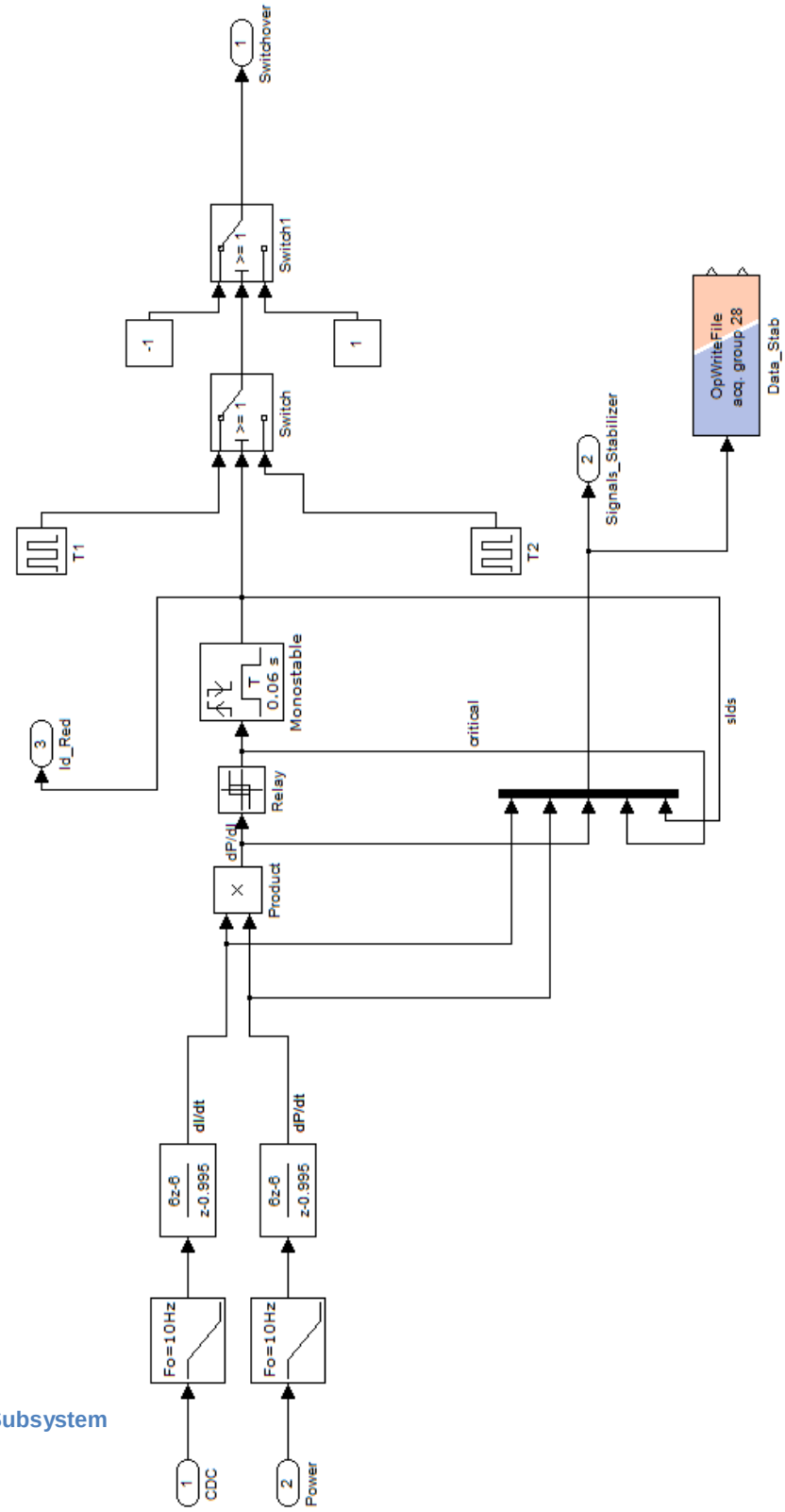


Fig. 63: AVS Subsystem

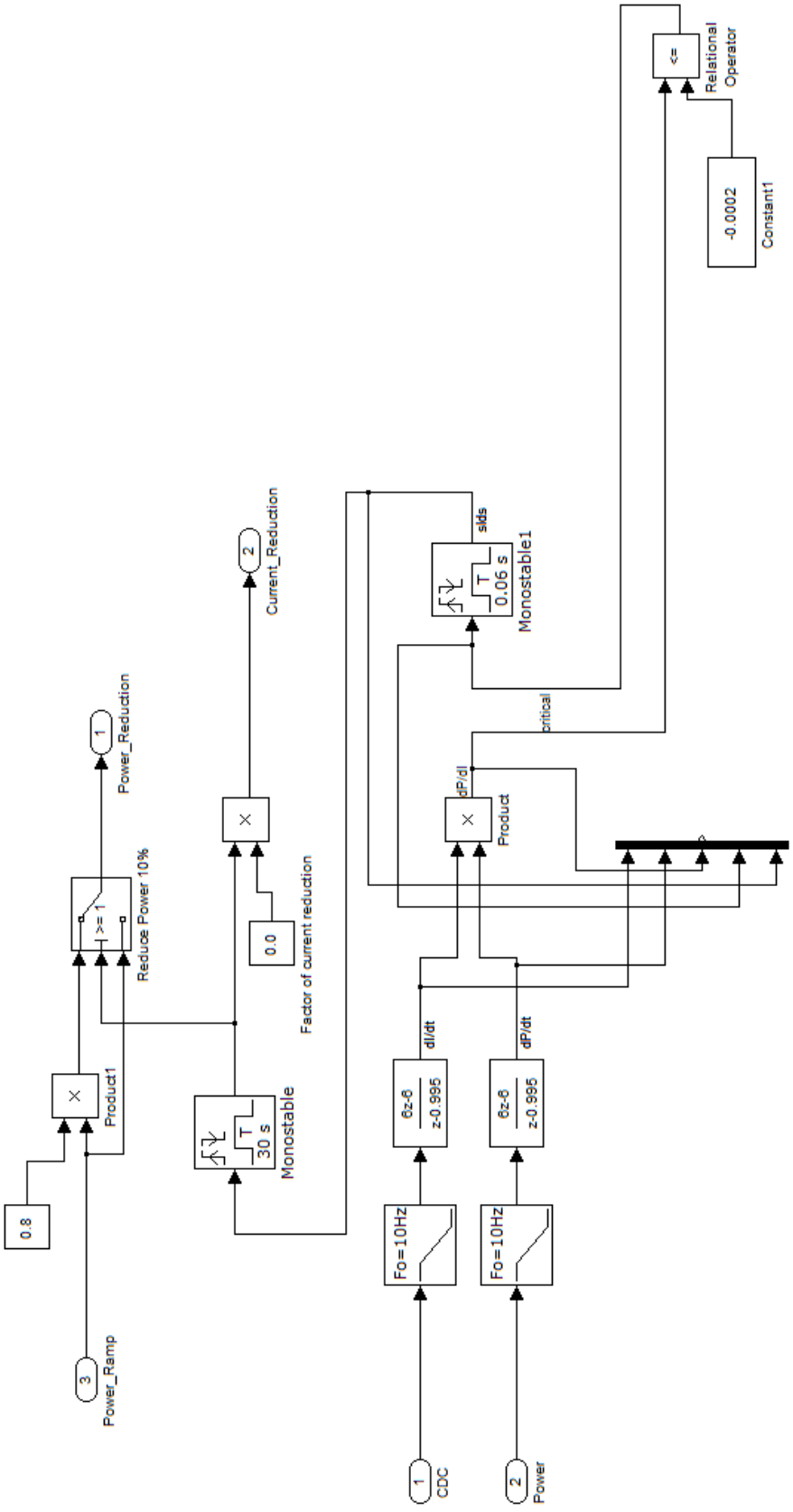
Some problems occurred while testing the automatic power reduction (Fig. 64). It appeared that a transmission with the “GoTo” and “From” blocks from the Simulink library over more than one subsystem can lead to a data loss, but it also depends on how these systems are interlaced into each other. But no further investigation on that had been done; instead some new circuit designs was implemented. The system loses a bit its clarity, but it is working fine with the modification.

The next challenge occurred, while trying to find the right settings for the power reduction.

After switching off the stabilizer to test the behavior of automatic power reduction and switch that device on a sudden trigger impulse of the relay that is triggering the monoflop occurs and automatic power reduction was initiated. This is caused through an undefined state of the relay we are using in the AVS. While running on nominal conditions the factor $\frac{\partial P}{\partial I_d}$ is around zero, which means that it is in between the switching conditions of the hysteresis block. So a value of x that is [0.0001 > x < -0.0002] means an undefined state, and the output can be true or false, with no predetermination. This effect of not having a defined state does, however, not occur when the system just starts with AVS being active since then the output of the hysteresis switch will always be positive and not undefined.

Regarding the function principle of the automatic power reduction mechanism, which means, that after surpassing the MTP point, an automatic power reduction should be initiated without an oscillation around the MTP point. The cause of no switch back point, when on the upper branch of the PV curve, due to a non-oscillating behavior, leads to the following variation of the automatic power reduction principle, compared with the one in PSCAD.

Comparing to the circumstance that this never occurred, within the simulation that was done with PSCAD, further investigations on that become necessary. Due to tight time constraints regarding the schedule of this project, no further analysis is performed at this point.


Relational Operator
<=
-0.0002
Constant1
slds
0.06 s
Monostable1
critical
dP/dt
Product
2
Current_Reduction
1
Power_Reduction
>= 1
Reduce Power 10%
0.0
Factor of current reduction
Product1
0.8
30 s
Monostable
3
Power_Ramp
dI/dt
dP/dt
6z-6
z-0.995
Fo=10Hz
1
CDC
2
Power

Subsystem

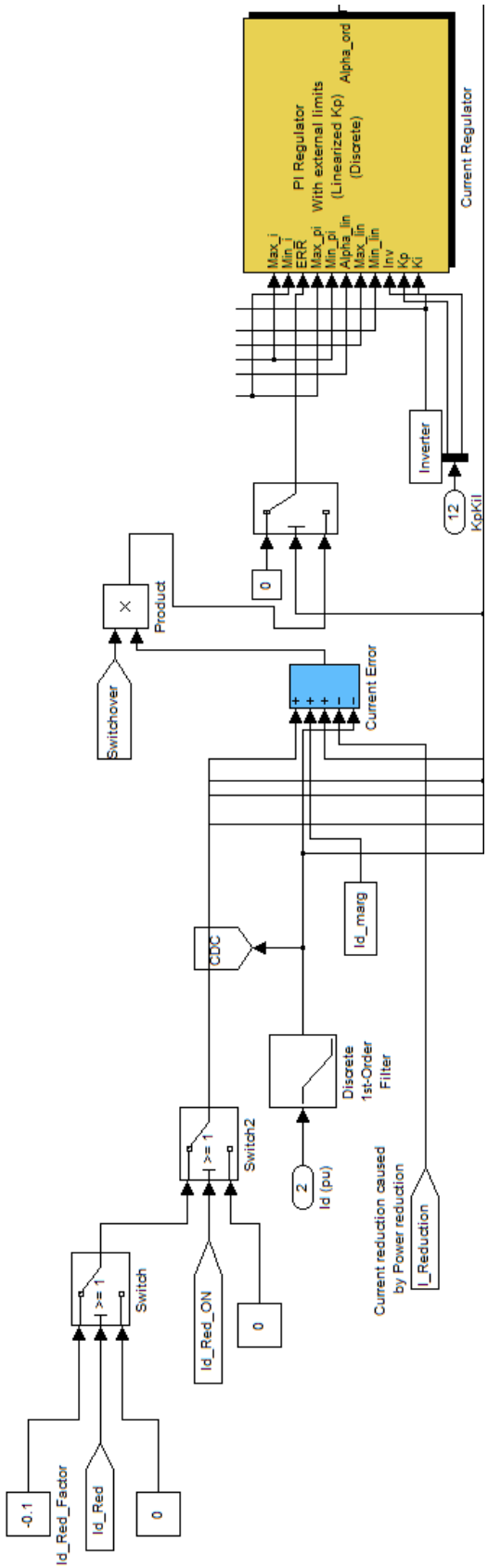


Fig. 64: Control Signals of AVS inside Inverter Control

Fig. 65 illustrates how the control signals (the output signals of the AVS and Power_Reducer subsystem, Fig. 62) are acting inside the inverter control shown in Fig. 61.

Display in Fig. 65 is just a brief cut-out of the whole subsystem inside the inverter control mask, to illustrate how the generated signals from the AVS act in the closed loop control circuit of the inverter. The detailed, complete circuit is attached to the appendix.

2.2.2.7 Scoping Data Problematic / Building Test Scenarios

The previously mentioned disadvantage of a massive time lag between the simulation and the console subsystem used to scope the signal leads to rethink about the manual controls that were implemented in the circuit in order to perform tests on the behavior of the AVS.

Precast functions that perform an “in-the-loop” change of parameters or values needed to be implemented and the former embedded manual functions were switched inactive. Therefore at this point it is just mentioned that there is the option to manually adjust values of the system, but without the possibility to watch an on time respond of the system. Due to that fact the manual controls are still embedded in the system, to maybe allow acting with them when a solution for the scoping challenge is found.

To perform a highly detailed real time data acquisition, the “OpWriteFile” block from the special OPAL-RT library is used. Due to a more time intensive appendance, at that point it seems to be the only feasible way of handling the circumstances with the simulator.

It is not an “in-the-loop” scoping of the signals, but at least the high resolution, true data that is computed inside the simulator.

A method of adjusting some parameters for testing purposes is shown in Fig. 66.
The Parameter Control, as a function of the RT-Lab software surface.

This still does not allow an “in-the-loop” change of the parameters while the simulation is running, but at least the systems does not need to be built again after a change of a parameter or an adjustment of some value.
At least, this fact gains some more time while running test cycles on the simulator.

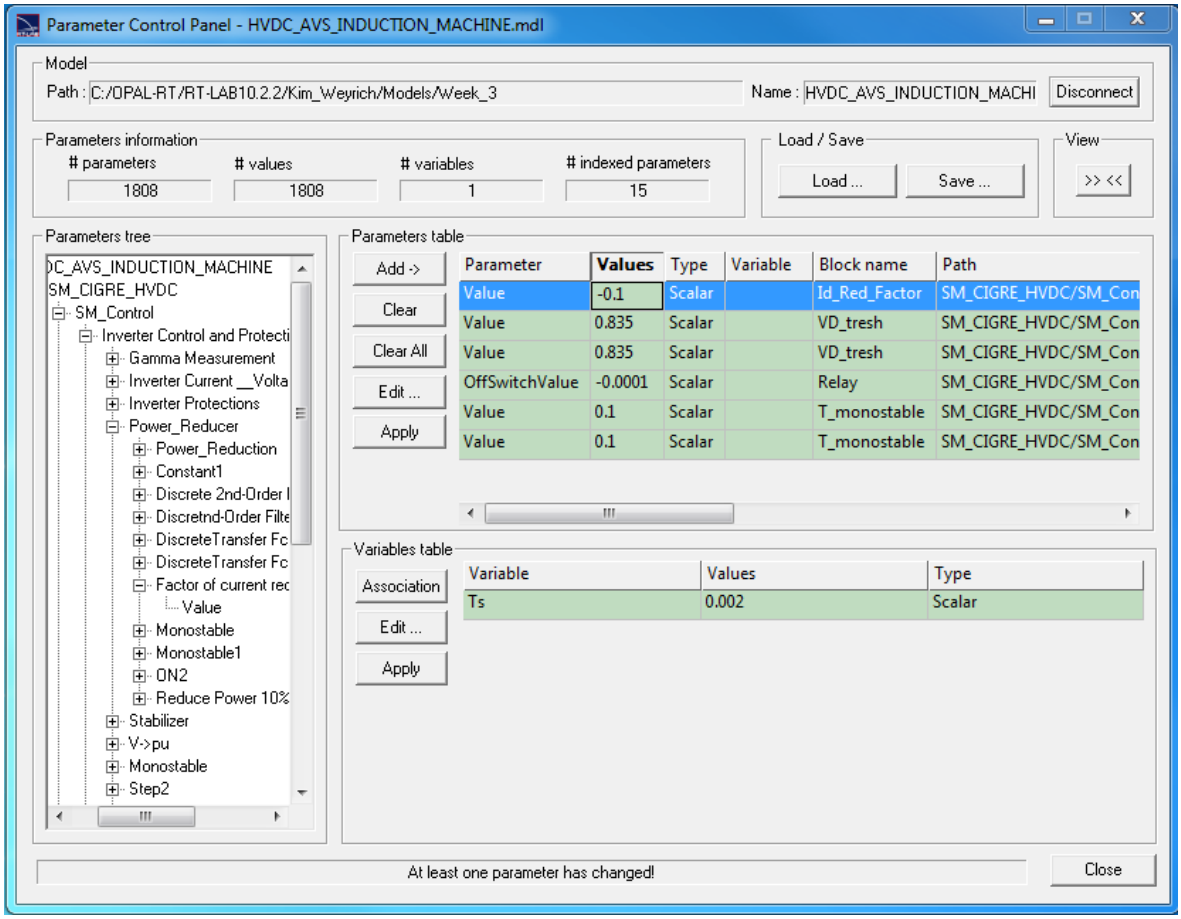


Fig. 65: Parameter Control Panel

2.2.2.8 Implementation of Asynchronous Machine

Regarding task #2, an Implementation of an Asynchronous Machine should be performed to test the performance of the AVS for consumer equipment which is known to have the potential to pull the voltage further down.

For our case a standard squirrel cage induction machine was modeled. Shown below, the equivalent circuit diagram for the d and q axis. SimPowerSystem uses this mathematical description to model a squirrel cage induction machine in its environment

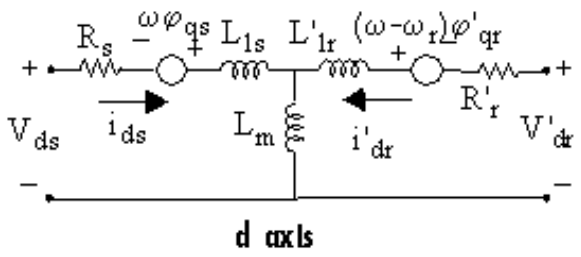


Fig. 66: d Axis Asynchronous Machine

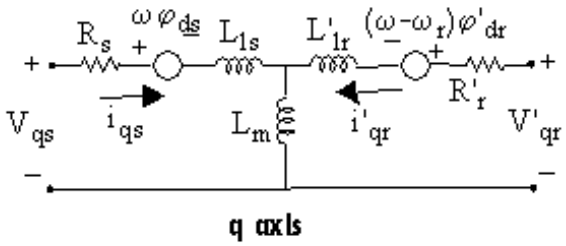


Fig. 67: q Axis Asynchronous Machine

$$V_{qs} = R_s i_{qs} + d\varphi_{qs}/dt + \omega\varphi_{ds}$$
$$V_{ds} = R_s i_{ds} + d\varphi_{ds}/dt - \omega\varphi_{qs}$$
$$V'_{qr} = R'_r i'_{qr} + d\varphi'_{qr}/dt + (\omega - \omega_r)\varphi'_{dr}$$
$$V'_{dr} = R'_r i'_{dr} + d\varphi'_{dr}/dt - (\omega - \omega_r)\varphi'_{qr}$$
$$T_e = 1.5p(\varphi_{ds} i_{qs} - \varphi_{qs} i_{ds})$$

where

$$\varphi_{qs} = L_s i_{qs} + L_m i'_{qr}$$
$$\varphi_{ds} = L_s i_{ds} + L_m i'_{dr}$$
$$\varphi'_{qr} = L'_r i'_{qr} + L_m i_{qs}$$
$$\varphi'_{dr} = L'_r i'_{dr} + L_m i_{ds}$$
$$L_s = L_{ls} + L_m$$
$$L'_r = L'_{lr} + L_m$$

Fig. 68: Equivalents Asynchronous Machine[XIII]

Regarding our German identifiers, it requires some explanation.

$L_{ls} = Inductance_{leakage\_stator}$

$L_{lr} = Inductance_{leakage\_rotor}$

$L_m = Magnatizing\ Inductance$

The asynchronous machine also called induction machine, has the following rating:

$S = \sqrt{3} * I_{Line} * U_{Line}$

$S = 1.73 * 15.9kA * 13.804kV$

$S = 380\ MVA$

The detailed data can be found in the appendix. The values for line current and line voltage depend on the reference PSCAD Model "with_motor_and_red_ld_110630.psx".[XV]

[XIII] Information provided by Matlab Help Library
[XV] Model designed by Prof.Dr.Walter Kuehn

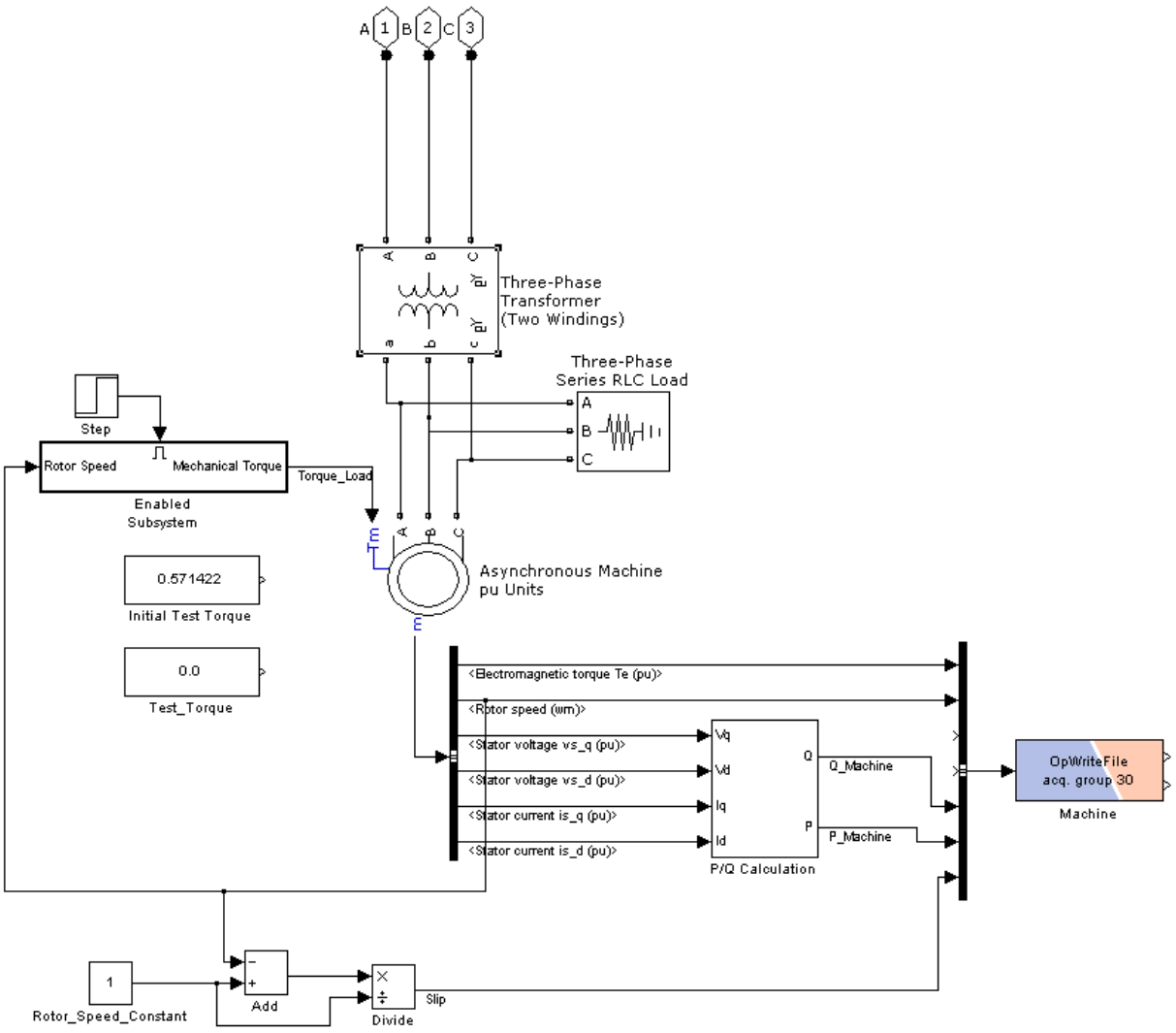


Fig. 69: Implementation of Asynchronous Machine

Fig. 70 shows the principle implementation of the asynchronous machine in the rectifier subsystems. The three-phase transformer (Fig. 70, connections A, B, and C) is connected to the rectifier bus, which can be found in the detailed model description in the appendix.

The bottom of Fig. 70 shows the calculation of the slip, in order to judge whether the machine has exceed its break-over point or not.

The P/Q Calculation became necessary to allow a judgment of the results that were obtained with the present circuit. The exact method of their calculation is illustrated in Fig. 71. With the given Stator Data of the d-axis and q-axis, regarding the current and voltage, real and reactive power are calculated.

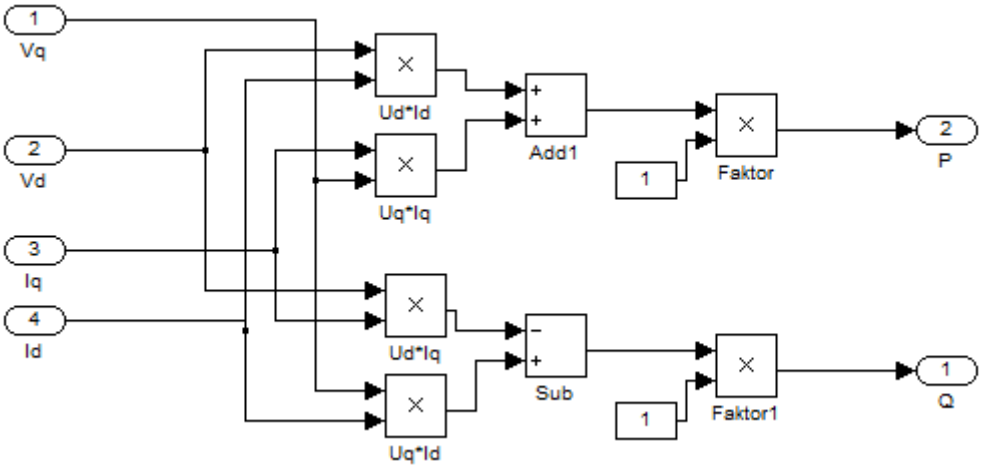


Fig. 70: P/Q Calculation

Another big difference of the already discussed differences of those two simulation tools is the fact that a block, modeled as a current source, cannot be connected in series with the inductive element of the second block.

Adding a high-value resistance in parallel with one of the two blocks is necessary. You can also specify high-value resistive snubbers if the blocks have a snubber device.

Fig. 72 shows a solution to that characteristic SimPowerSystem issue. A Three-Phase Series RLC Load is added to solve not only this specific problem, it's also mandatory to enable a further load-flow calculation by the solver. An active power load of 10kW is adjusted in the RLC Load and allows the simulation a right computation. Also this load should not affect our test scenarios in a negative way.

At least, it should be mentioned that the Nominal power of the transformer is chosen to be about 6 times higher than the rating of the induction machine. This is mandatory to permit the machine a re-raise of the electro mechanical torque after decreasing and increasing it, with a various internal grid voltage.

The enabled subsystem in Fig. 70, to generate the mechanical load torque, is illustrated in Fig. 72. As an aim to shown the differences of VDCOL, AVS and the automatic power reducer, you should able to recognize their working method in one single diagram.

Therefore it has become necessary to push the induction machine back to nominal conditions, which means to reduce the load torque after the machine has surpassed the breakdown torque, to get it back.

To have a better appreciation of this mechanism, Fig. 73 shows the load torque function in order to serve our test scenario demands.

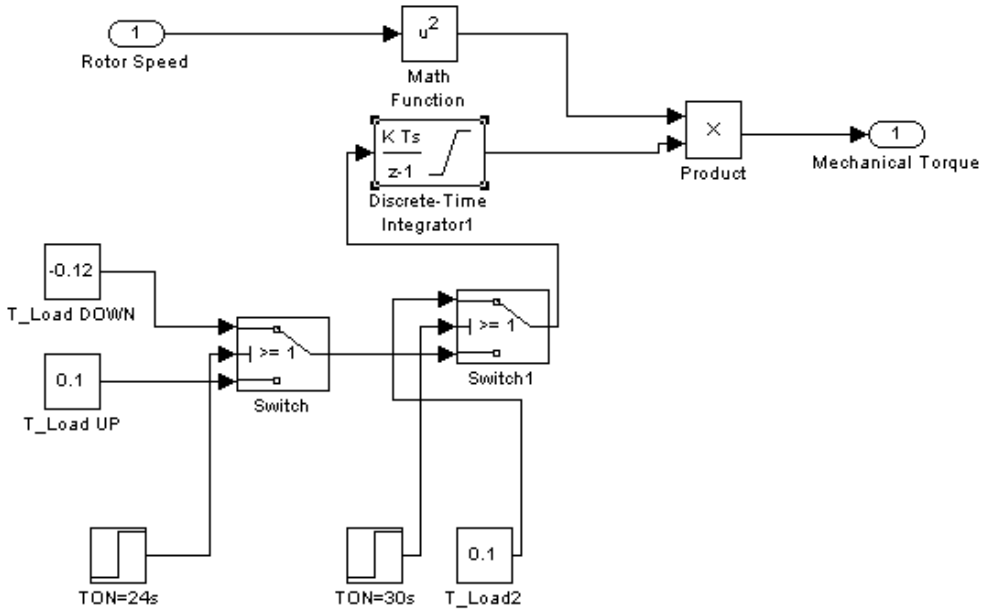


Fig. 71: Torque Reference Calculation

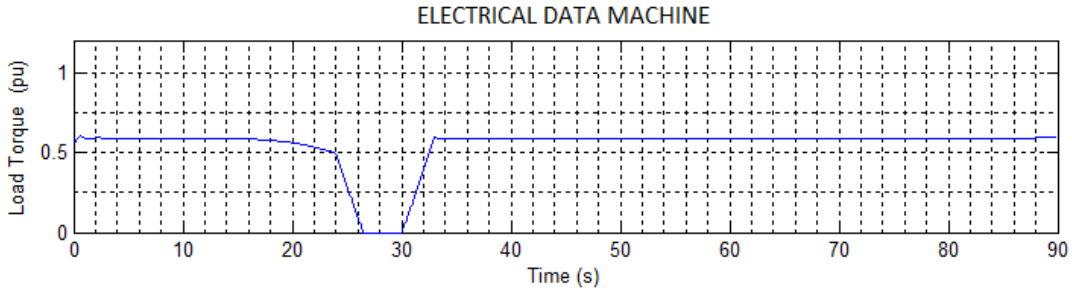


Fig. 72: Load Torque Function

2.2.2.9 Implementation of Synchronous Generator

This stage of the project is not completed yet, and requires further investigation. But as a part of this project, and work on it is already done, it should be mentioned here.

As it has been shown in the attempt of implementing a synchronous generator instead of a static grid source, the SimPowerSystem environment is not the smartest tool to design highly complex power systems straight from the scratch. The Load Flow problematic and some software disadvantages complicated this task in a way that a feasible solution was not found in the constraints of the schedule.

For the sake of completeness all the attempts with different approaches are attached to the appendix. Even some working models with a synchronous generator serving a static source, to a static load even to a dynamic load can be found in the appendix, and should be the starting point for a further investigation in order to complete this project in the future.

2.2.3 Differences between PSCAD and RT Implementation

As it becomes evident from the former chapter, there are a lot of differences between the two application development systems. Too many to mention all, but a few fundamental differences should definitely be illustrated.

Fig. 74 depicts the different approaches to describe hardware within the system. While SimPowerSystem uses a more mathematical, physical way of describing their components, the PSCAD environment uses a more a practical specification (data sheet) related method of modeling individual components.

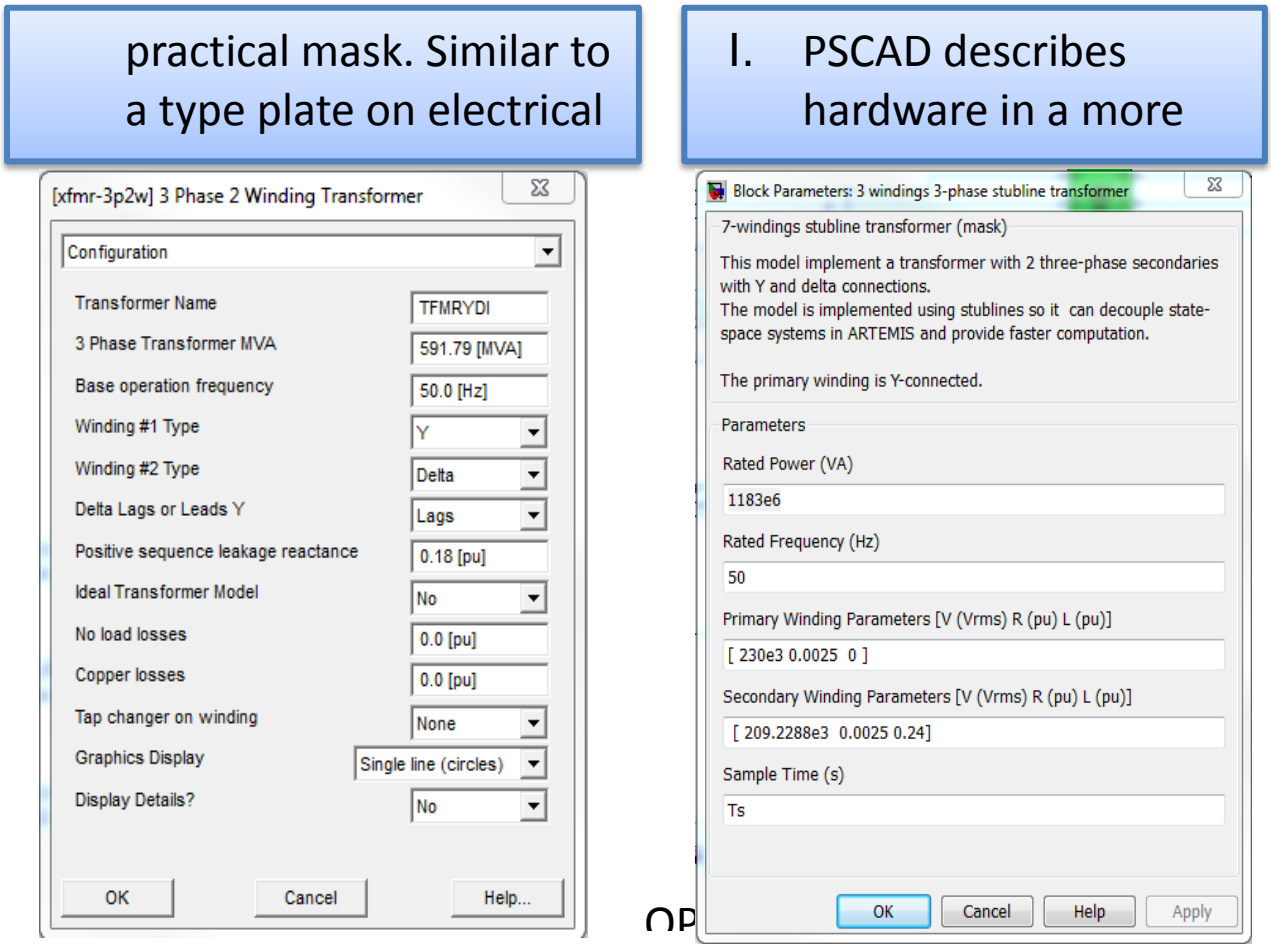


Fig. 74: Different Masks of Hardware Description

The fact the PSCAD uses sometimes phase voltages and sometimes line voltages (sometimes crest values, sometimes rms-values) while SimPowerSystem is requiring line voltages has to be carefully treated. A manual conversion of the values used in previously realized PSCAD simulation, is indispensable.

Fig. 75-77 show this problematic for the previously mentioned induction machine.

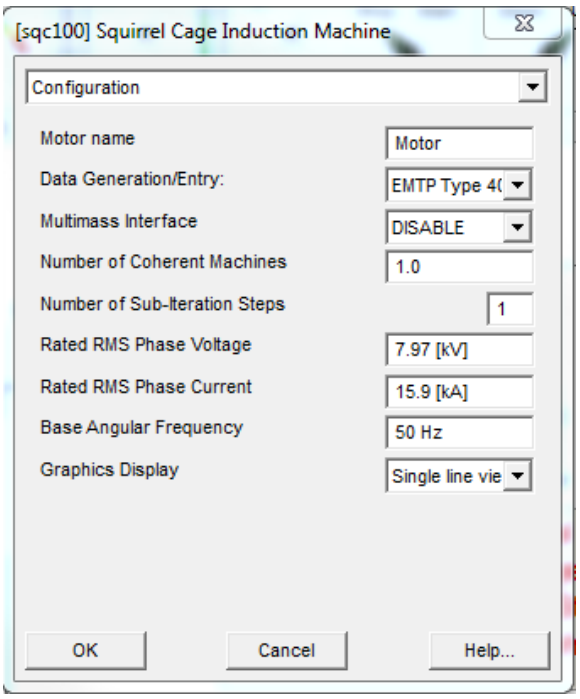


Fig. 75: PSCAD Induction Machine Mask 1

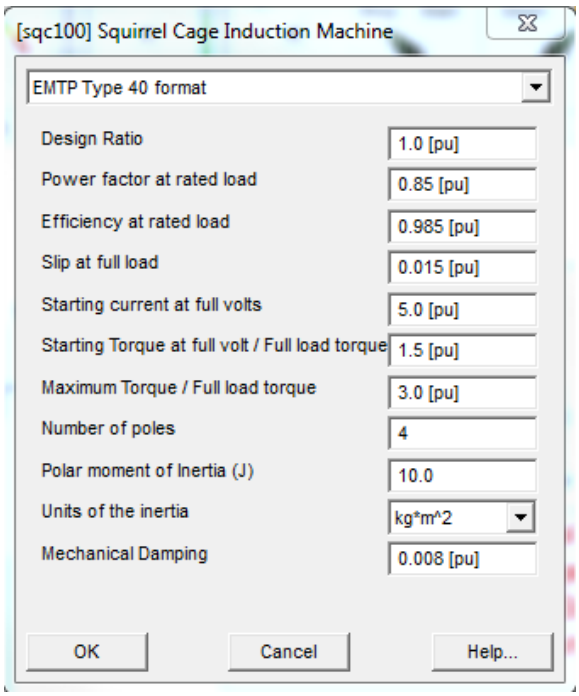


Fig. 76: PSCAD Induction Machine Mask 2

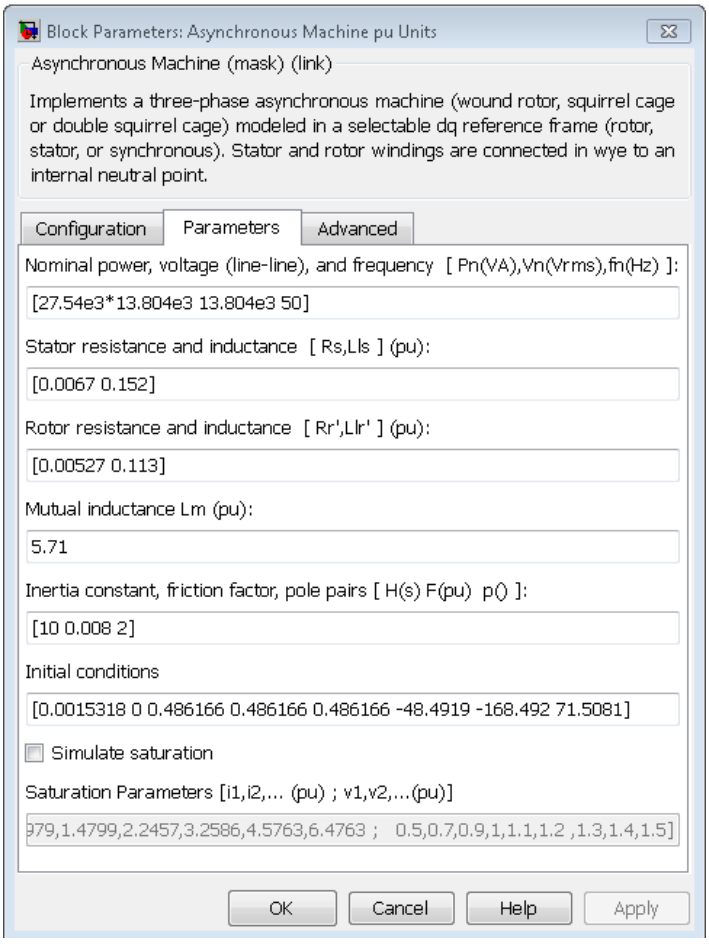


Fig. 77: SimPowerSystem Induction Machine

Comparison Chart

• PSCAD uses easy to handle drop-down menu to parameterize the components. → Easy intuitive method, but limited in its options	• OPAL RT uses subsystems interlaced into each other → Difficult to read, but almost without constraints regarding adjustment options
• PSCAD with "signals on wire" → Makes analyzing and trouble-shooting less time intensive	• OPAL RT without that possibility → Scope and display embedding causes time delay
• No good solution regarding test scenarios → Wired and hardly readable switching construction can occur	• Graphic user interfaces, with the ability to use object-oriented advanced language → Clearly arranged controls on the windows surface
• PSCAD with no support to compute highly complicated algorithms needed for complex system models. → Leads to manual computing in a foreign software environment	• OPAL RT with the ability to solve those challenges easily with MATLAB environment in background. → Basic possibility of data exchange between SimPowerSystem and MATLAB

Conclusion PSCAD vs. SimPowerSystem (OPAL RT)

PSCAD:

- PSCAD is the faster tool to obtain the first results.
- Easy and intuitive way to design models.
- Basic components such as switched, sliders, etc. allow fast access to a manual variation of essential values while simulating.

SimPowerSystem:

- OPAL RT is not that intuitive and a longer time range is needed to setup a model.

- Almost without constrains regarding the variation of the components.
- Due to the complete Simulink library, abundant of different components.
- Wrong parameterize can lead to system collapse, reset of value without function. Reload of whole system indispensable.

Conversion of PSCAD models into SimPowerSystem (OPAL RT)

- The different appendages of parameterize the model of both application development systems, make a one-to-one conversion almost impossible.
- Requires a lot of manual conversion of components.
- The problem is the different approach of both systems in modeling their components.

3 Simulations

This represents the final chapter and also the final outcome of this project.

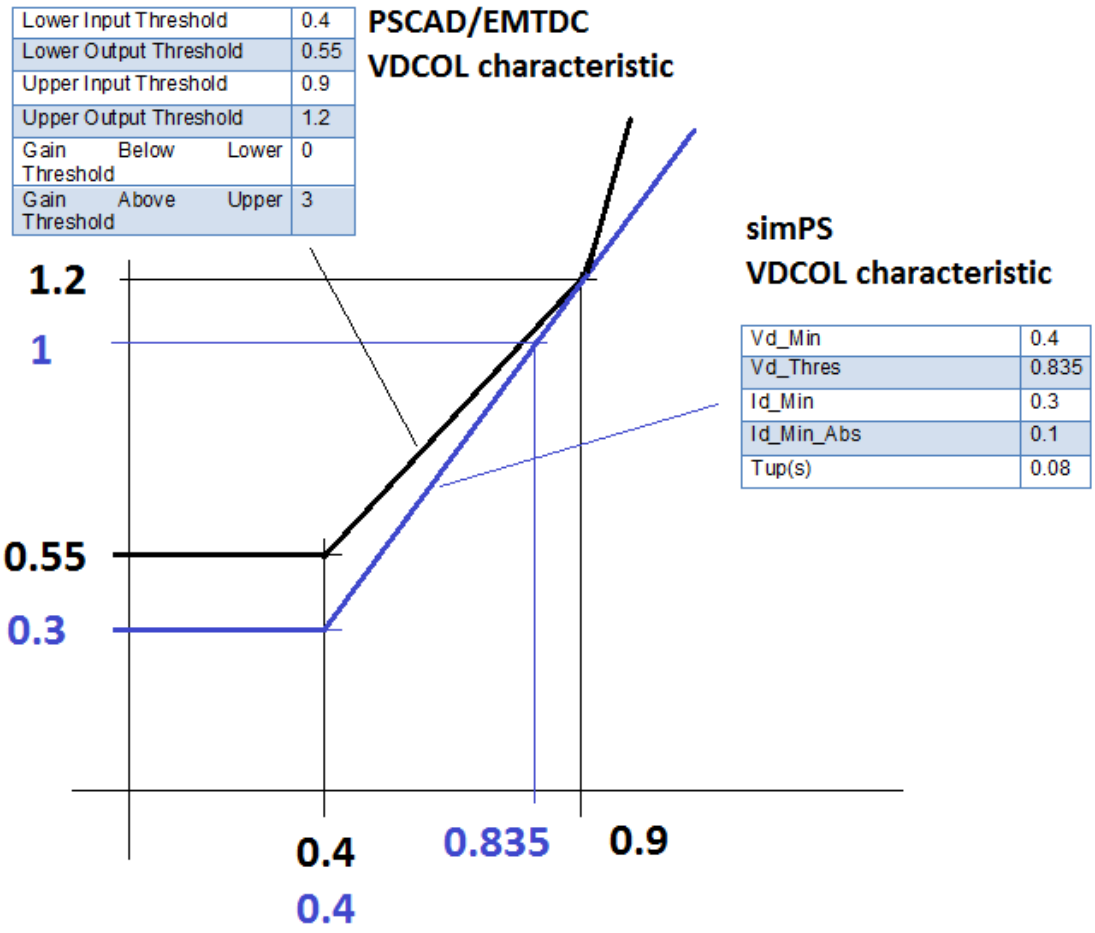
It allows a not only for a judgment on some important capabilities of the two simulation systems but it also shows the performance of the AVS and its benefits in comparison to VDCOL.

3.1 Case A – Weak Grid

Weak grid means that the internal reactance of the rectifier side AC grid was set to a value resulting in a short circuit power ratio of 1.9 at an internal AC grid voltage of 380 kV. It is assumed that this SCR value results from a structural change with a SCR value of 3.33 before this change. For the calibration of the VDCOL characteristic the normally existing SCR value of 3.33 was taken to show the effect of inappropriate calibration.

The characteristic permits DC current overload of 1.2 at 0.9 p.u. AC voltage. This is either a temporary overload or can even be continuous overload depending on the prevailing ambient temperature. Looking at Blackwater with continuous control of the 60-kV-filter bus voltage and discrete control of the 345 kV terminal voltage via the on-load tap changer of the converter transformer this is a realistic assumption. But even if the characteristic would be changed such that the upper input threshold is 0.95 the forthcoming results don’t lose their validity.

Looking at the table values given below it appears that the VDCOL calibration differs considerably between PSCAC/EMTDC and SimPS (appendix sec. 5.4). But the graphs show that this is not true.



Calibration of PSCAD/EMTDC VDCOL characteristic

Lower Input Threshold	0.4
Lower Output Threshold	0.55
Upper Input Threshold	0.9
Upper Output Threshold	1.2
Gain Below Lower Threshold	0
Gain Above Upper Threshold	3

Calibration of SimPowerSystem VDCOL characteristic

Vd_Min	0.4
Vd_Thres	0.835
Id_Min	0.3
Id_Min_Abs	0.1
Tup(s)	0.08

Fig.78 shows the automatic variation of the internal grid voltage, in order to test the behavior of the VDCOL, AVS and the AVS with automatic power reduction in the listed order. This function simulates the effect of internal grid changes which can be fast and slow and large or small. Here only one form is used to limit the case number and to focus on the essential point of comparing VDCOL and AVS.

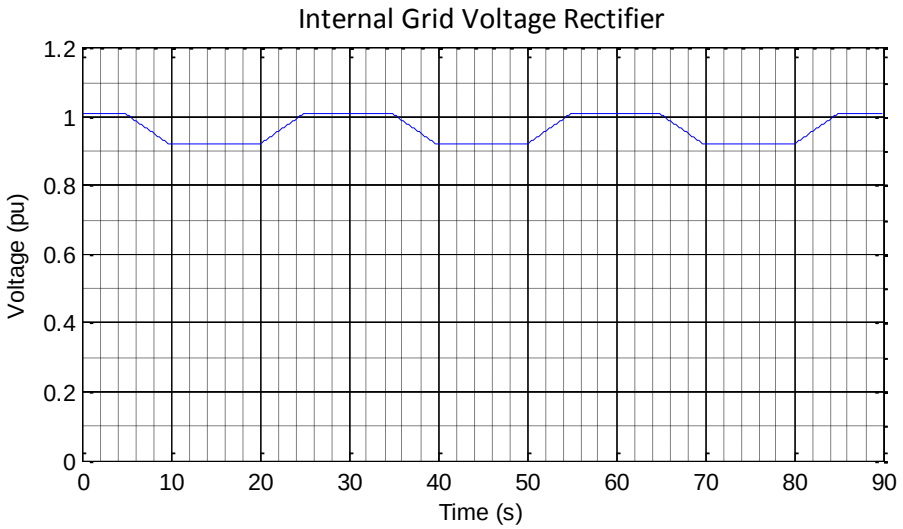


Fig. 78: Internal Grid Voltage for SimPowerSystem Test

In the PSCAD simulation the variation of the internal grid voltage can be accomplished manually or via an automatic ramp. As previously mentioned manual ramping was not possible with SimPS due to the massive time lagging console subsystem to apply manual changes.

3.1.1 Weak Grid on Rectifier Side

At Rectifier: $SCR = 1.9 \;\widehat{=}\; L = 0.2\,H$ but calibration for $SCR = 3.33$

At Inverter: $SCR = 1.9$

Fig. 79 shows the response of the AC terminal voltage of the rectifier as a result of a variation of the internal grid voltage shown in Fig.78.

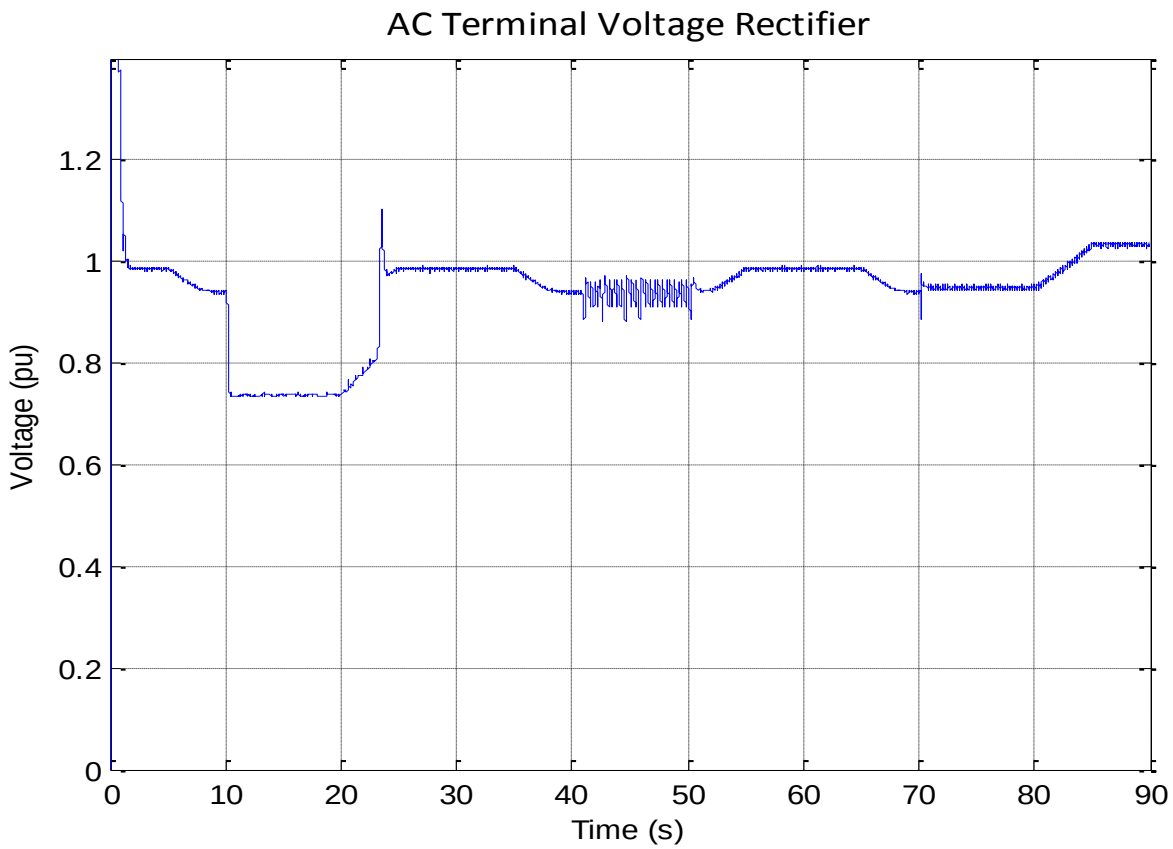


Fig. 79: AC Terminal Voltage Rectifier

From approximately 10 to 20 seconds it is solely VDCOL being active which results in a massive voltage drop under 0.8 p.u. to almost 0.7 p.u..

A remedy provides the AVS with the revolving operating point, as seen from approx. 40 to 50 seconds, where the voltage does not drop below 0.9 p.u..

The last mechanism tested is the AVS with automatic power reduction ($t \approx 70 - 80s$).

Fig. 80 shows the recorded data of the rectifier that corresponds to the results in Fig. 79. Illustrated is here the steep drop of the DC voltage caused by VDCOL resulting in DC current increase in order to serve the power demand. The power transferred is low due to the limited DC current which is also shown in the gap between the current reference value (green line) and the actual value (blue line).

The displayed low DC voltage is unacceptable for long distance transmission.

When the AVS intervenes, a stable oscillation around the MTP-Point occurs, which results in no DC voltage drop, and the maximum power is transferred at AC grid voltage.

AVS with automatic power reduction can ensures safe operation of the system without a revolving operating point.

For the sake of completeness the inverter related oscillograms are displayed in Fig. 81 and 82.

The values of the DC voltage (low) and the DC current (high) holding for VDCOL operation and the comparison with the respective values of the AVS are a clear proof that the operating point at VDCOL operation slides to the lower branch of the PV-curve. Connected to this not only inefficiency of operation but many other disadvantages as they were already listed under in chapter 1.

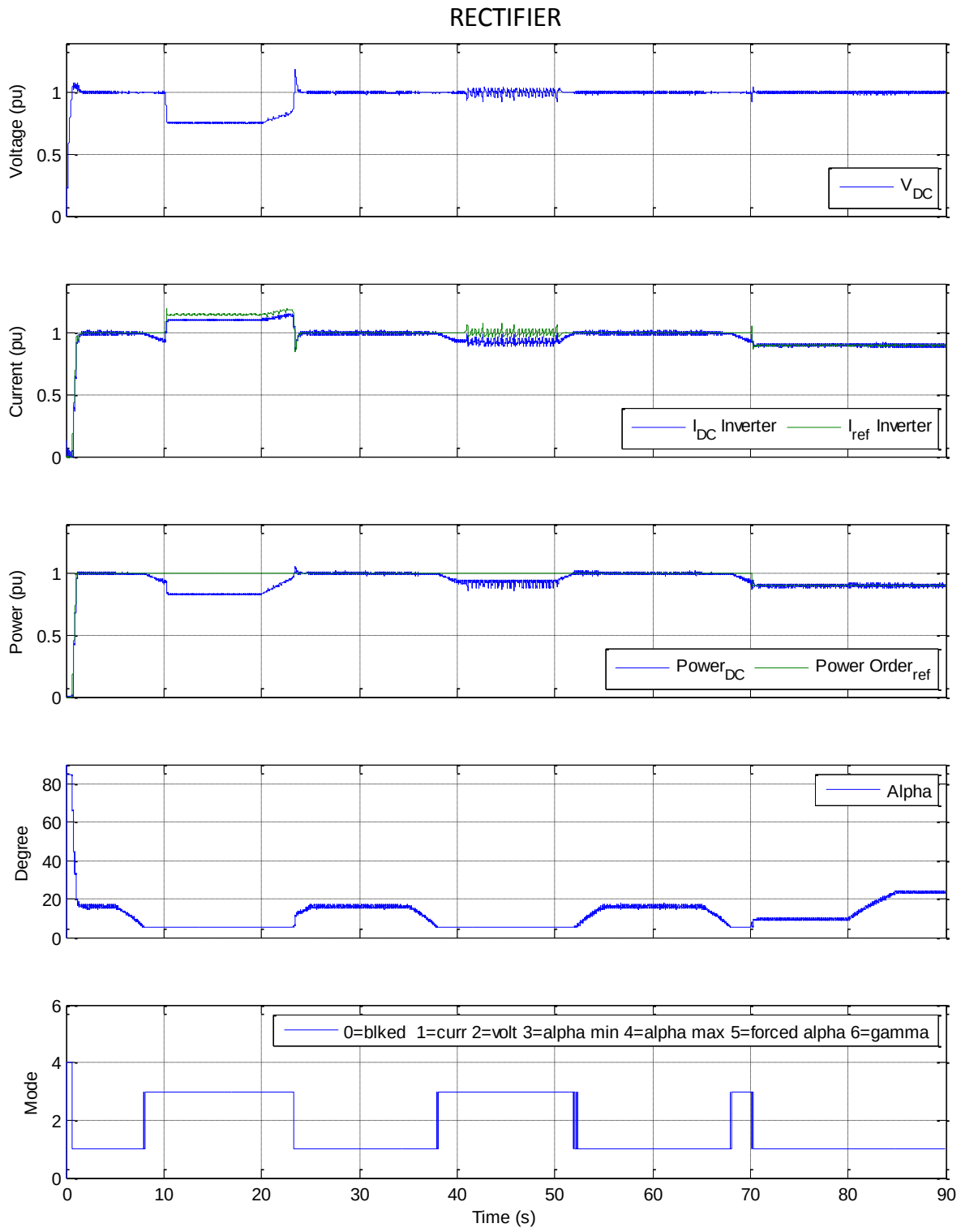


Fig. 80: Rectifier Oscillograms

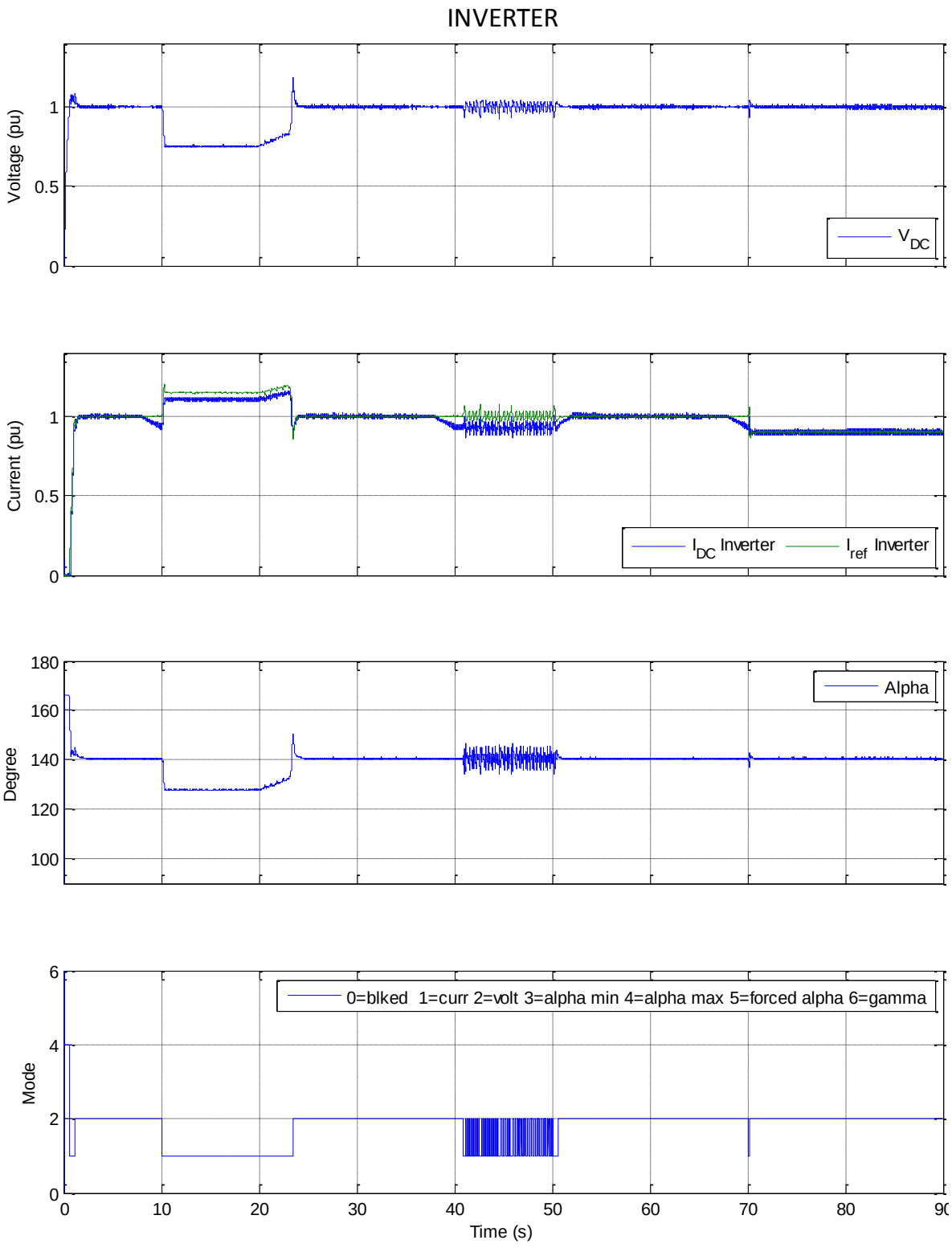


Fig. 81: Inverter Oscillograms

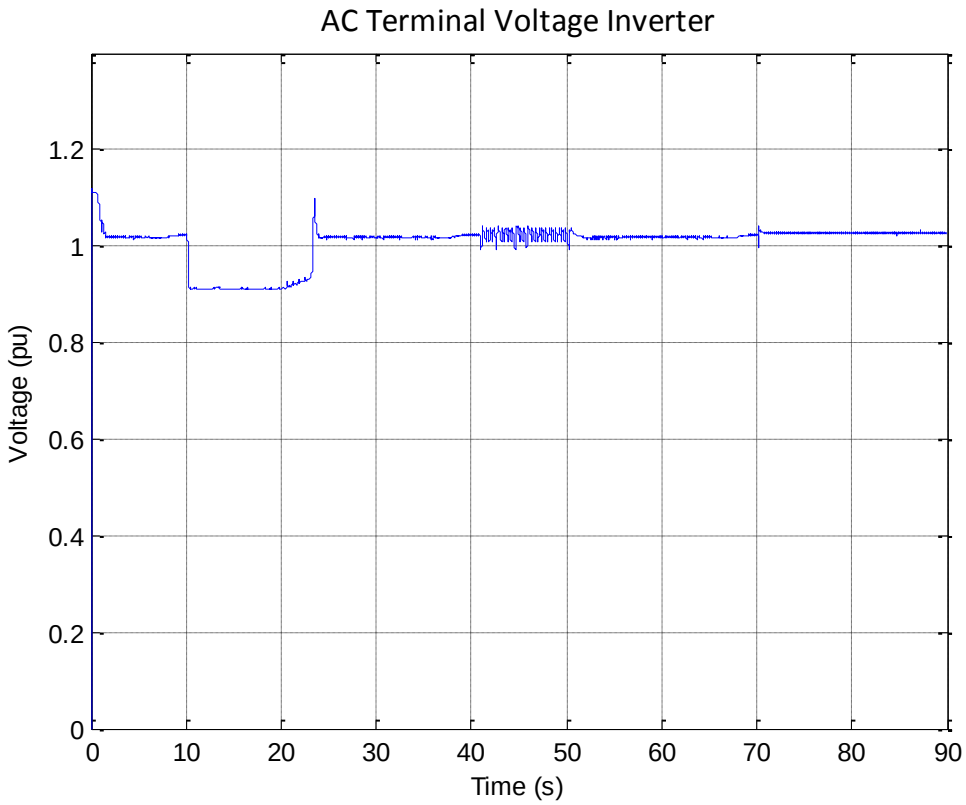


Fig. 82: AC Terminal Voltage Inverter

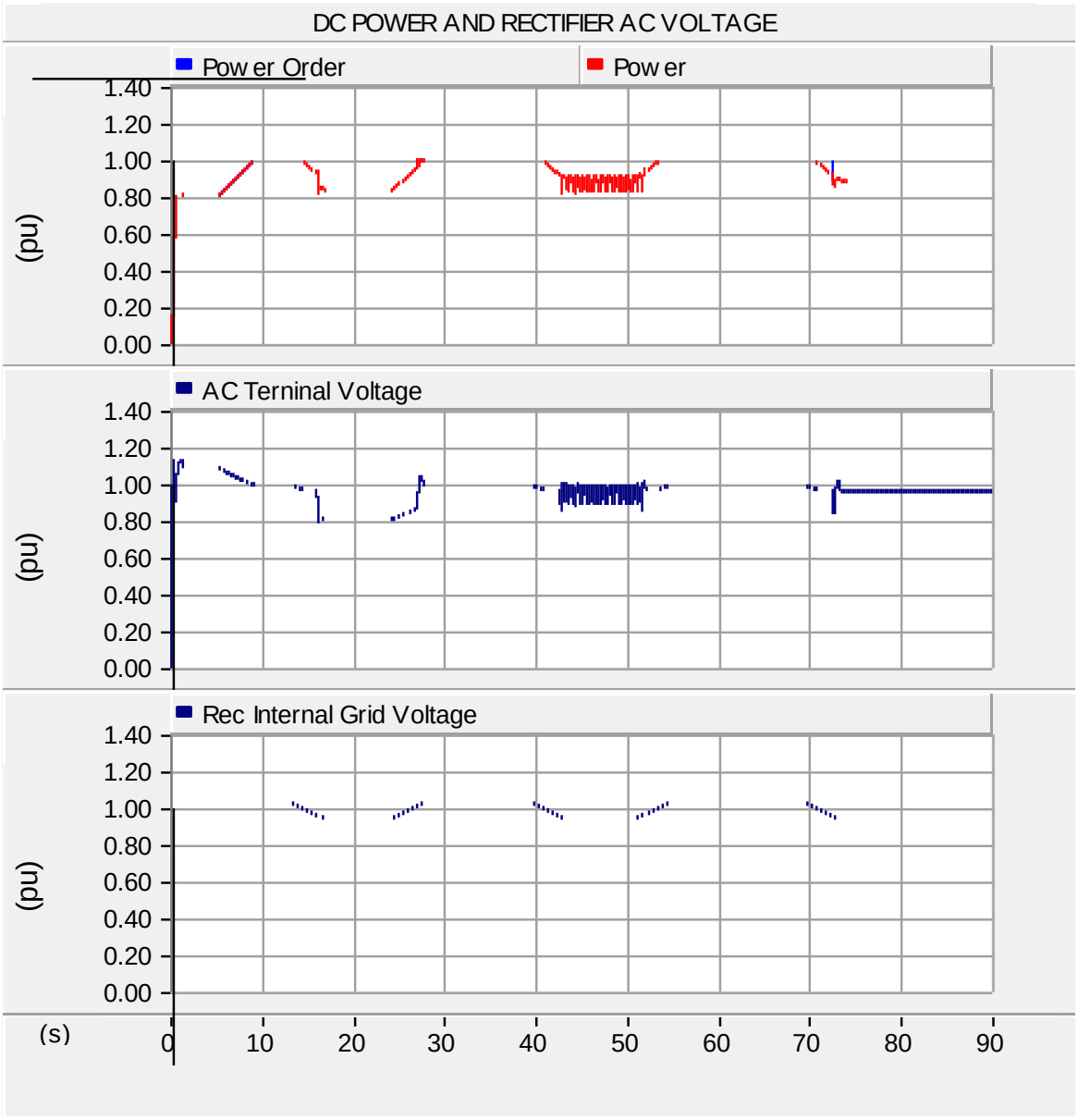


Fig. 83: DC Power and Rectifier AC Voltage

Fig. 83 and 84 illustrate the previously results achieved with the PSCAD simulation system. One difference is the manually applied change in the internal grid voltage, which leads to some small shifts regarding the time axis, but as displayed in the oscillograms, both simulations show the same working principle of the AVS.

In the PSCAD Scenario the simulation starts with a power order of 0.8 p.u. and is ramped to 1 p.u. and nominal conditions are achieved at about $t \approx 10s$. After that, the same order of the specific mechanisms is tested, which means first solely VDCOL, AVS and last the AVS with automatic power order.

For the sake of completeness it should be mentioned, that the internal grid voltage remains low in the PSCAD simulation which results in a small difference of the AC terminal voltage at the end of the simulation, which can, however, be neglected.

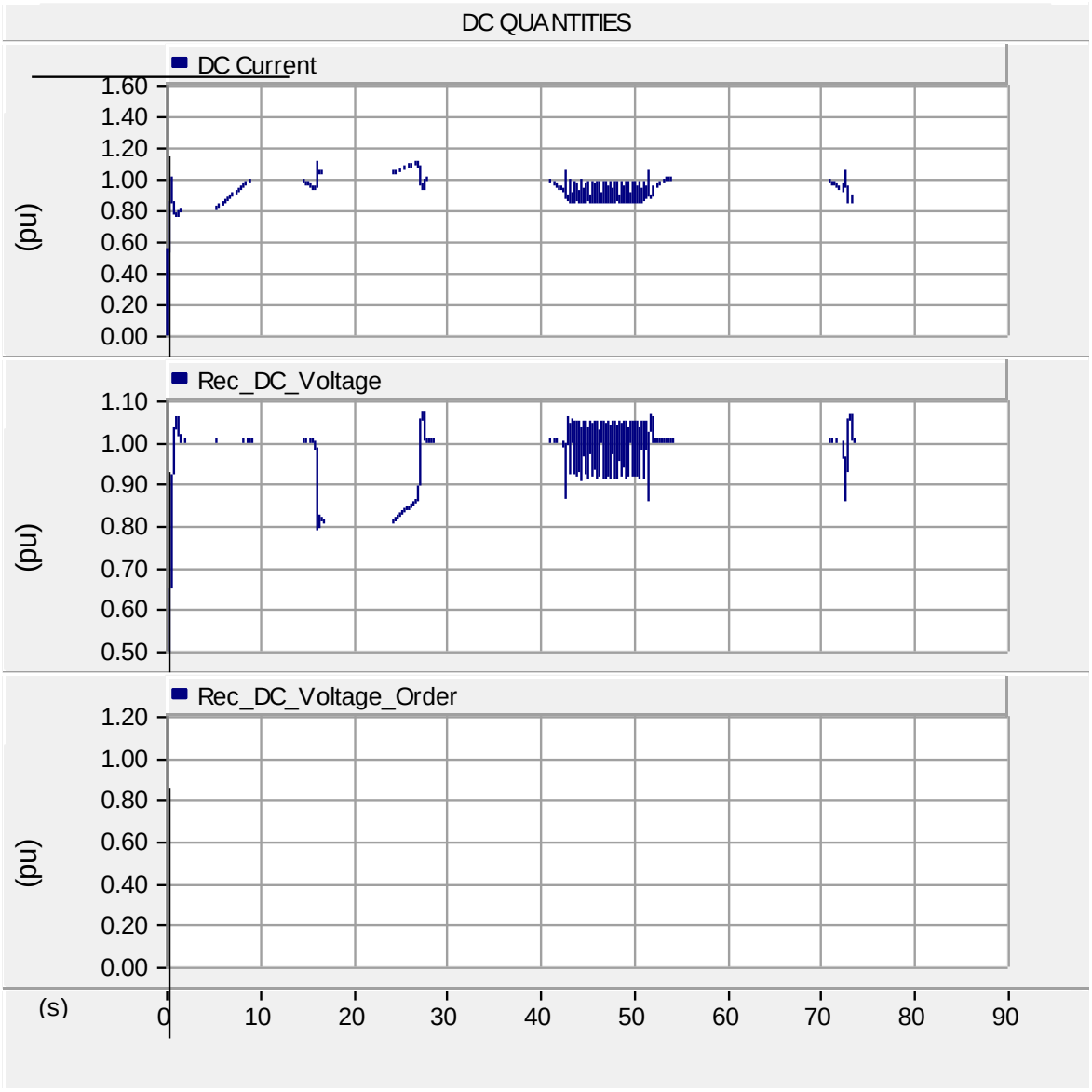


Fig. 84: DC Quantities

3.1.2 Weak Grid on Inverter Side

At Rectifier: $SCR = 2.5 \;\widehat{=}\; L = 0.15\,H$ but calibration for $SCR = 3.33$

At Inverter: $SCR = 2 \;\widehat{=}\; L_{series} = 0.47\,H$

The test the system behavior on a weak AC grid on the inverter side, the internal grid voltage of the AC Grid on the rectifier side is kept constant.

The same function as shown in Fig.78 is this time applied as internal grid voltage at the inverter.

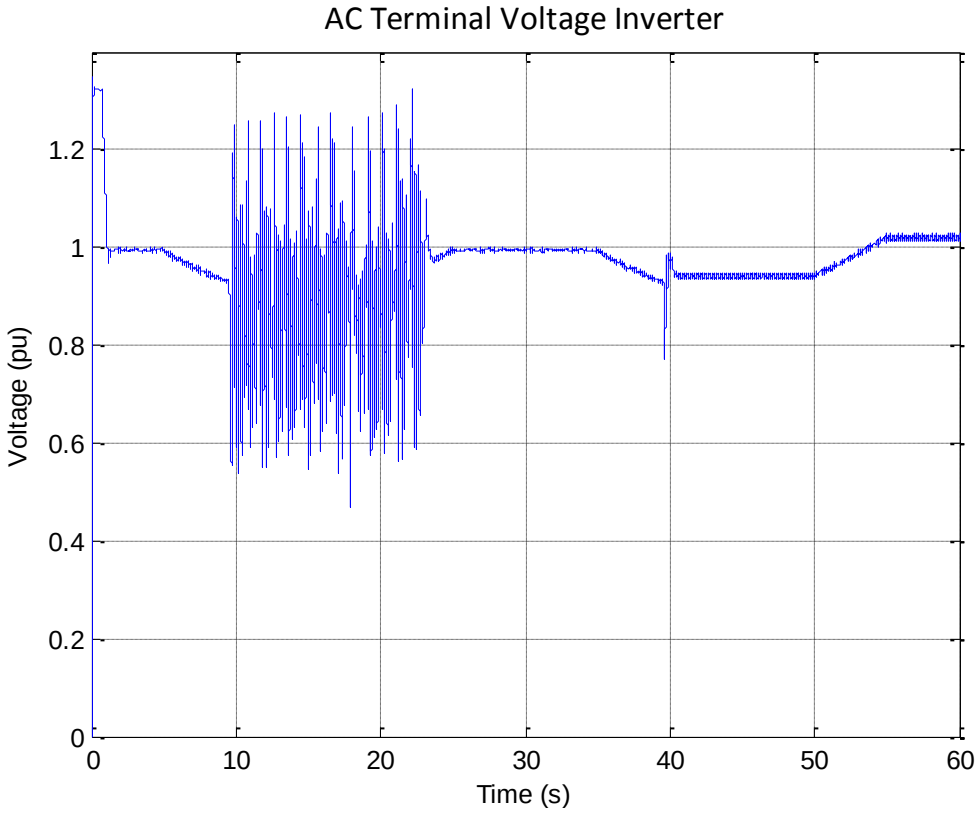


Fig. 85: AC Terminal Voltage Inverter

In this scenario only VDCOL and AVS with automatic power reduction is tested, therefore a reduction of the run time down to 60 seconds was made.

From approx. 10 to 20 seconds, with solely VDCOL, the serious problem of commutation failures occurs (Fig. 85 and 86).

In contrast to VDCOL the AVS method ($t \approx 40 - 50s$) shows just a short dip in the respective quantities, and no commutation failure occurs (Fig.86).

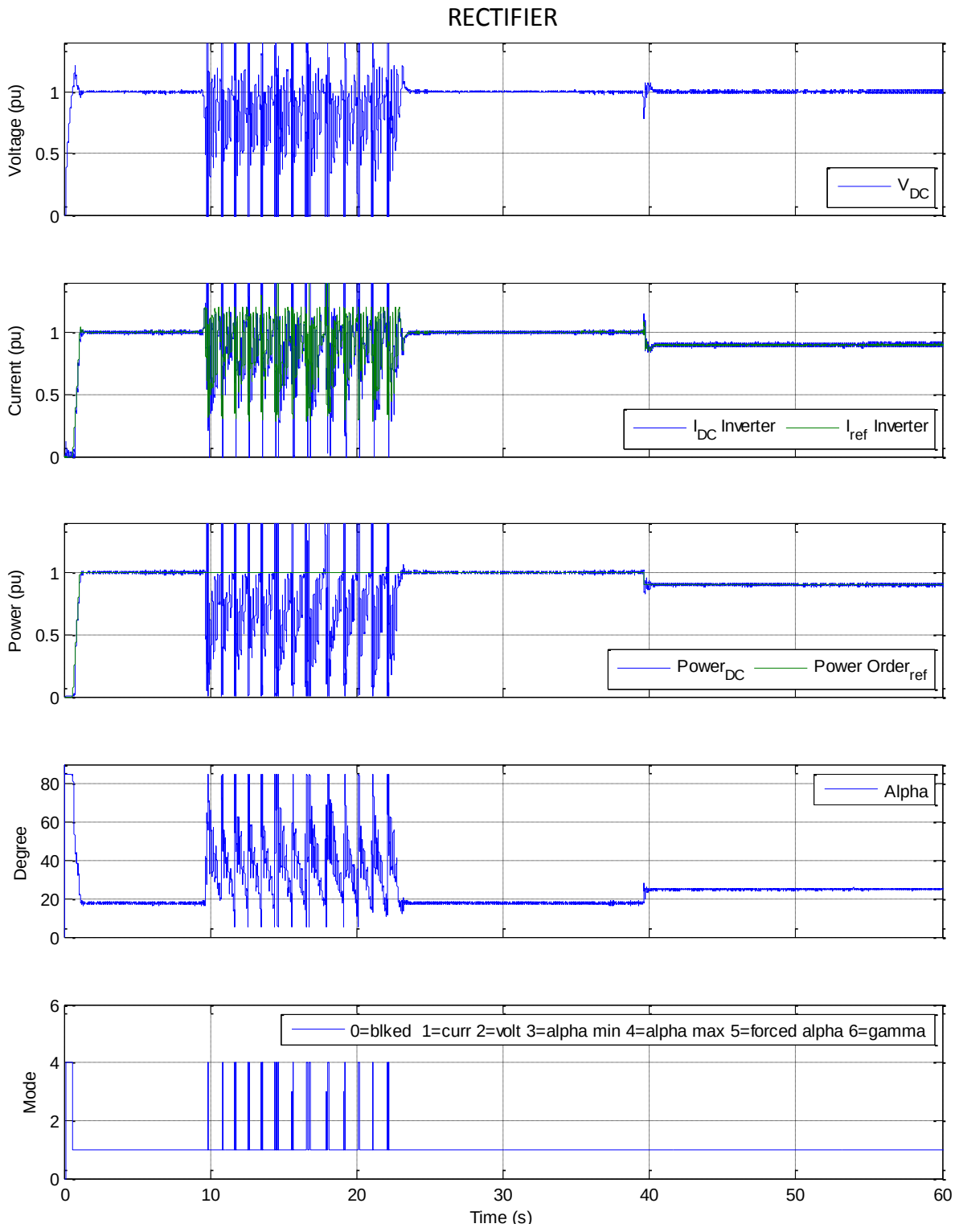


Fig. 86: Rectifier Oscillograms

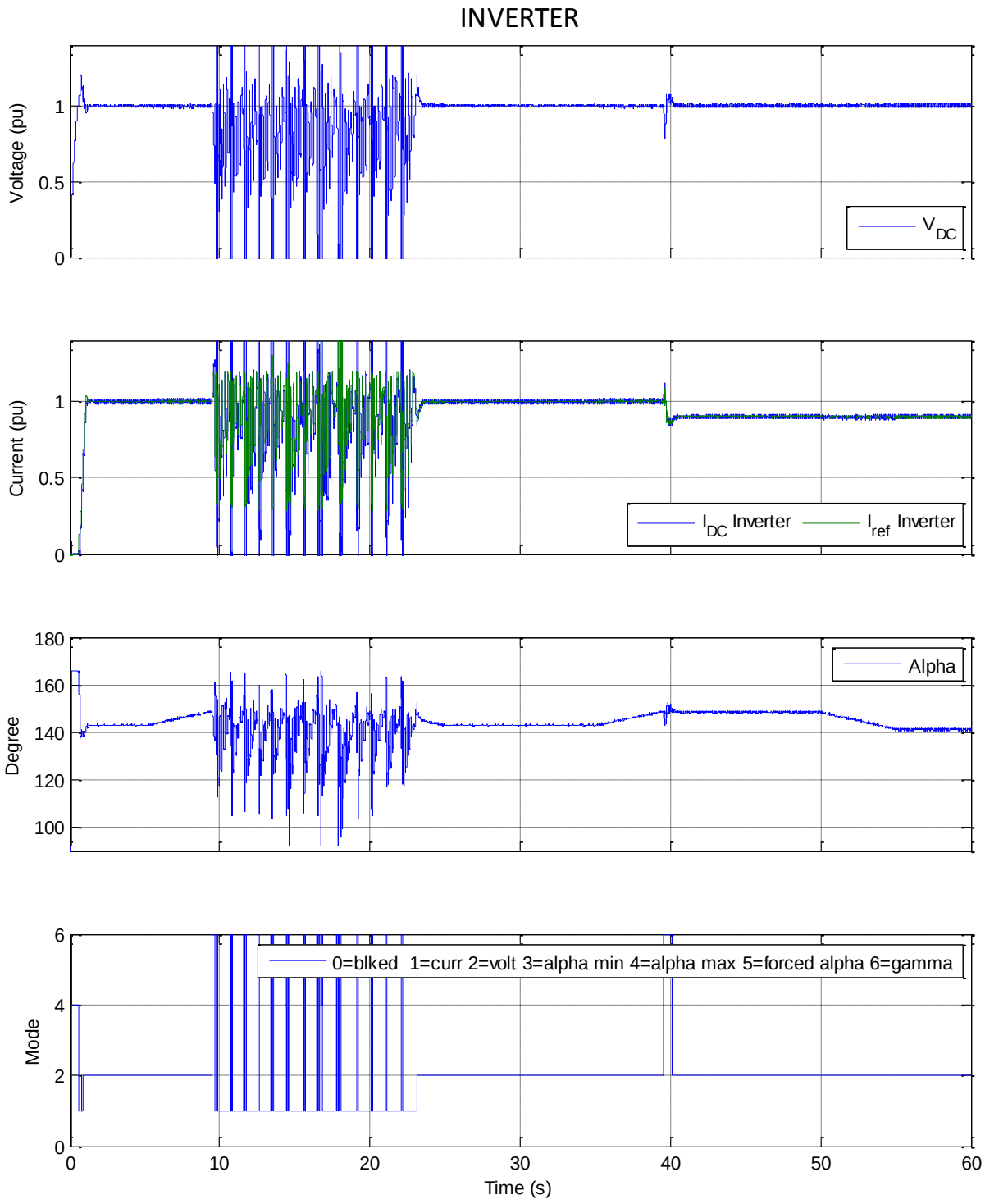


Fig. 87: Inverter Oscillograms

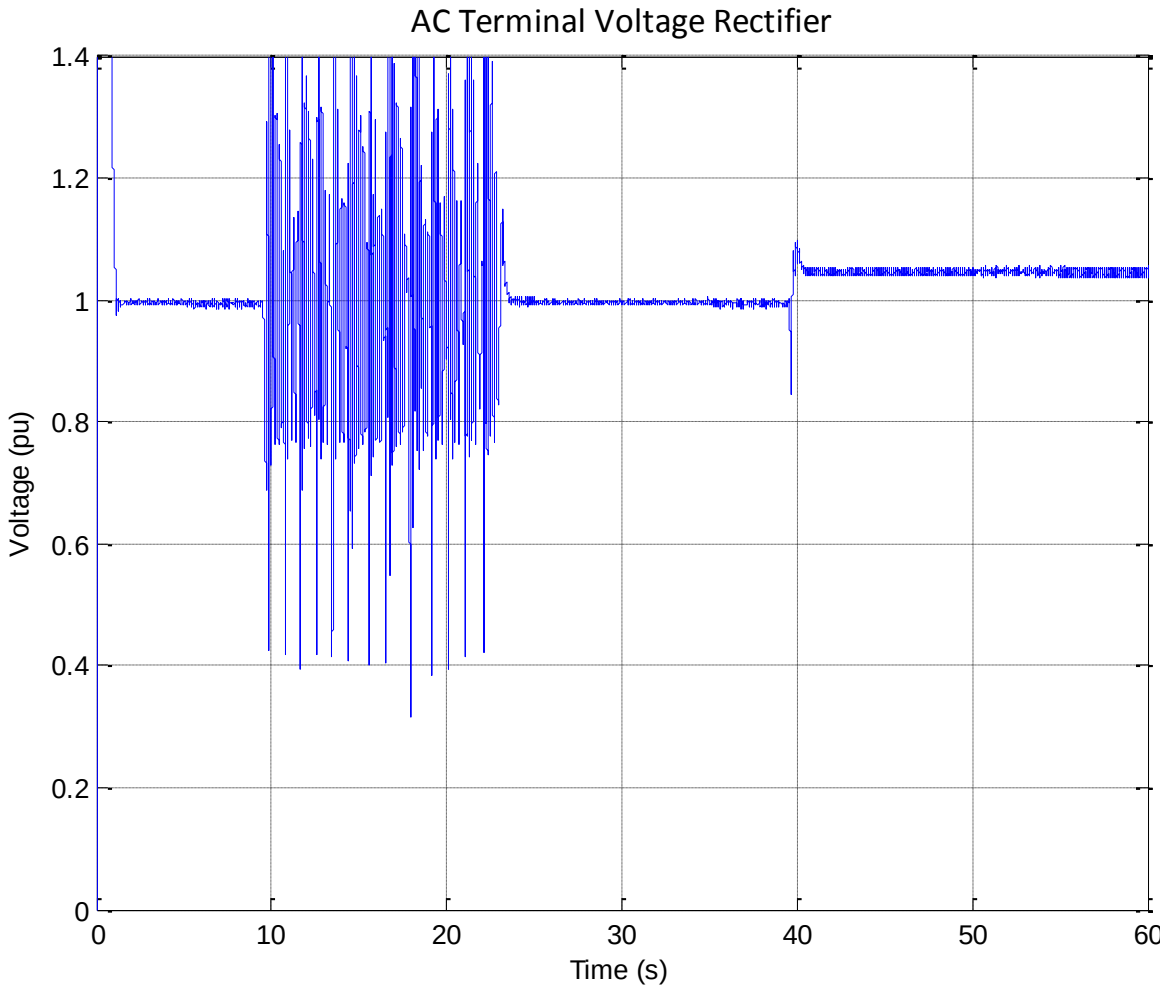
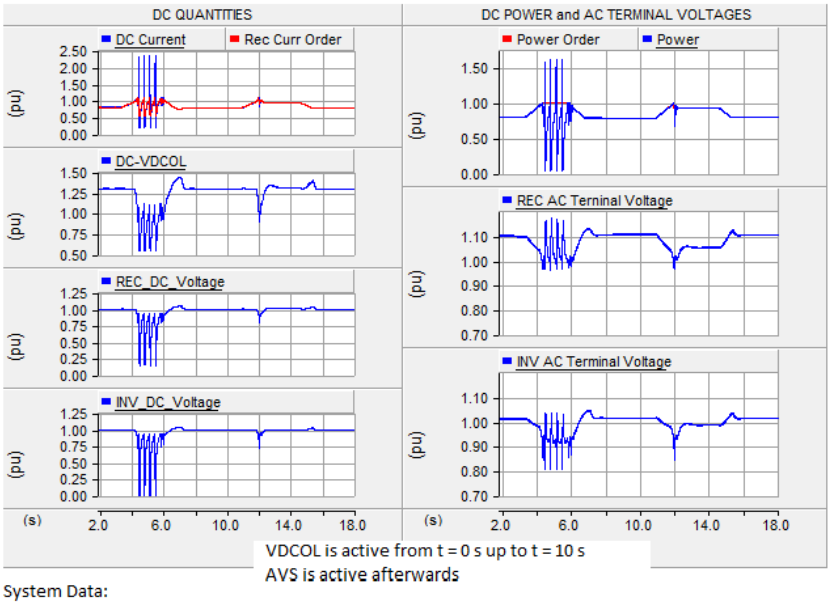


Fig. 88: AC Terminal Voltage Rectifier

An equal behavior is obtained with using PSCAD/EMTDC (Fig.89). Here not the internal grid voltage at the inverter is ramped up and down but the power order. Also the time frame chosen is somewhat different. With VDCOL the sliding of the operating point to the lower branch of the PV-curve cannot prevented. AVS keeps the operating point on the upper branch after only transiently moving to the lower branch.

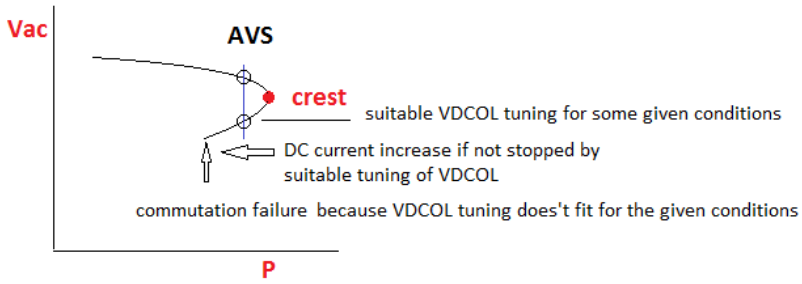
By good luck it can be that VDCOL prevents commutation failures, however, even then the operating point is not desirable (Fig. 90). It lies on the lower branch of the PV-curve. The PV-diagram and the text below the figure describes this situation.

CASE_1: Comparison of the effects of VDCOL and AVS - CASE_1_tuning
Inverter operating on very weak AC grid
using the Cigré Bench Mark Model for HVDC Controls
augmented by the Automatic Voltage Stabilizer



VDCOL is active from t = 0 s up to t = 10 s
AVS is active afterwards

System Data:
nominal DC voltage: 500 kV
nominal DC current: 2 kA
SCR rectifier grid: 3.33
SCR inverter grid: 2
internal ac grid voltage at rectifier: 390 kV
internal ac grid voltage at inverter: 210 kV



The conditions here are such that commutation failures occur when ramping up the power while only VDCOL is active (from t = 0 s up to t = 10 s).
Whether commutation failures occur depends on various factors which are the controls and its parameters but also main circuit parameters as the DC line capacitance.

Here it is clearly shown that commutation failures occur after the power order has reached the maximum transferable power level. The crest is surpassed and since current increase is not stopped by VDCOL - due to the given calibration - commutation failures are not prevented. See figure at the bottom of this page.

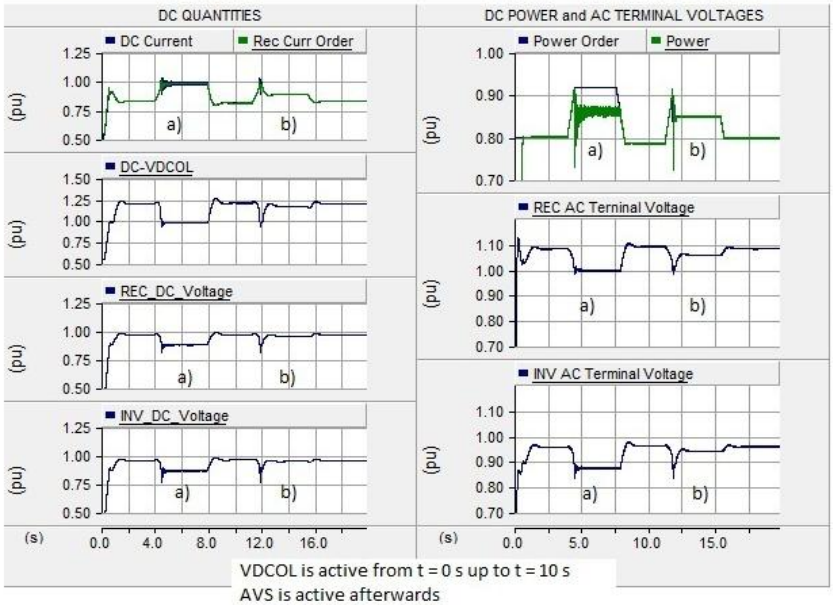
Calibration would only fit accidently as in CASE_2.
Since the beta angle is shifted towards 90 degrees - called forced retard - a commutation failure vanishs but re-occurs because the power order was not vet reduced. This was done after the forth occurence of the commutation failure. Of course this can also be done earlier.
The big difference makes here the AVS. No commutation failure occur. The power transfer is not disturbed very much and the voltage shows only one dip and then operation continues on an adaptively set new power level.

Kuehn, Feb. 25, 2011

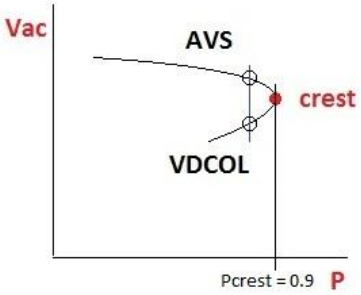
Fig. 89: Relevant Quantities for Case_1_Tuning[XVI]

[XVI] PSCAD/EMTDC Simulation by Kuehn, W.

CASE_2: Comparison of the effects of VDCOL and AVS - CASE_2_tuning
Inverter operating on very weak AC grid
using the Cigré Bench Mark Model for HVDC Controls
augmented by the Automatic Voltage Stabilizer



System Data:
nominal DC voltage: 500 kV
nominal DC current: 2 kA
SCR rectifier grid: 3.33
SCR inverter grid: 2
internal ac grid voltage at rectifier: 390 kV
internal ac grid voltage at inverter: 190 kV



The power ramp starts at t = 4 s from the steady state value of 0.8 pu. VDCOL is on. The actual power transfer cannot exceed the maximum transferable power level of the transmission system which at the given conditions is 0.9 pu.
However, the power controller drives the operating point over the crest to the lower branch of the PV-curve before VDCOL limits the current. This causes a steep voltage decline and a corresponding decrease of maximum transferable power of about 0.85 pu.
When ramping down the power order the operating point returns to the upper branch. Then to test the AVS the power order is ramped up again. Also here maximum transferable power is reached and AVS brings the power down to a safe value providing a certain margin.

That with VDCOL being active the operating point shifts to the lower branch of the PV-characteristic (see figure at the bottom) can be detected from the fact that at about the same power level the voltages are much lower for VDCOL than for AVS and accordingly the dc current is much higher for VDCOL than for AVS. Compare the levels at a) and b) in the figures on the left.
That the current is limited before commutation failures occur is only good luck.
If the internal ac grid voltage at the inverter is, e.g., set at 210 kV, then commutation failures show up.
See oscillograms of CASE_1.

Conclusion: VDCOL is very diffently acting for different conditions. This outcome shows that VDCOL is not a reliable method and even when limiting the dc current it does it with a very high probability only on the lower PV-branch with the already described disadvantages.

Kuehn, Feb. 25, 2011

Fig. 90: Relevant Quantities for Case_2_Tuning[XVII]

[XVII] Simulation by Kühn, W.

3.2 Case B – Test Performance with embedded Asynchronous Machine

At Rectifier: $SCR = 1.9 \;\widehat{=}\; L = 0.2\,H$ but calibration for $SCR = 3.33$

At Inverter: $SCR = 3.3 \;\widehat{=}\; L_{series} = 0.15\,H$

The function in Fig.78 is used again to test the behavior of the system. Also the running order of the specific systems tested remains the same as the one in the previous test runs.

But in contrast to former scenarios the DC power order is decreased to 0.8 p.u. taking into account the demand by the asynchronous machine. In this way the total power transfer on the AC line is about the same as before when starting the test.

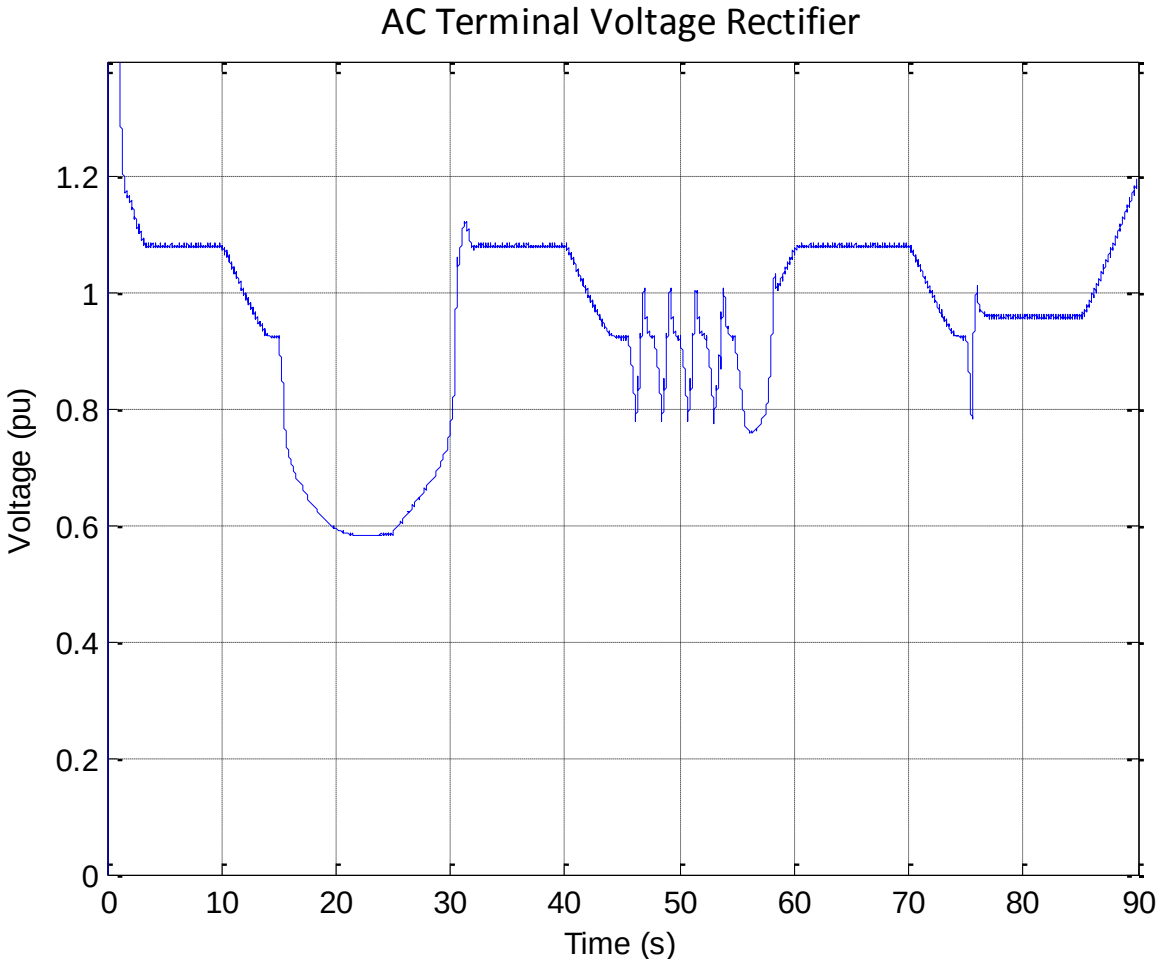


Fig. 90: AC Terminal Voltage Rectifier

The AC terminal voltage of the rectifier shows a massive steep depression with solely VDCOL taking part in the test run (Fig.91, $t \approx 10 - 30s$), down to 0.6 p.u.. This is an unacceptable low value, caused by the reactive power consumption of the asynchronous machine that is pulling further down the AC voltage.

Fig. 92 shows that DC power decreases despite increasing DC current which is a clear indication that the maximum transferable power point is surpassed.

Again a remedy is provided by the AVS $(t \approx 40 - 60s)$, and the AVS with automatic power reduction$(t \approx 70 - 90s)$.

The results confirm our previously made assumption that asynchronous machines pull the voltage further down once the HVDC system causes a voltage decline.

AVS prevents the collapse of the system.

Corresponding oscillograms of the inverter are displayed in Fig. 93 and 94.

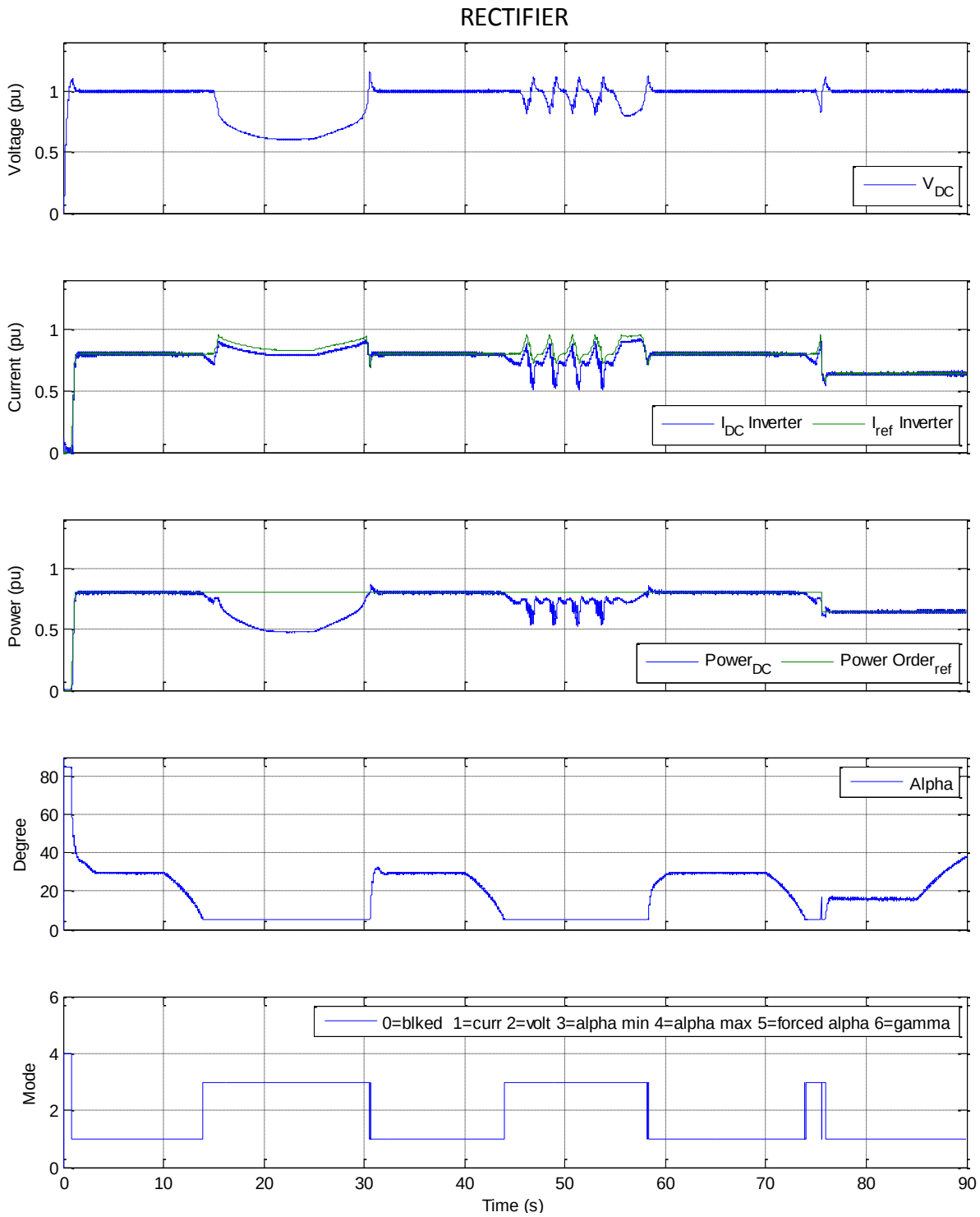


Fig. 91: Rectifier Oscillograms

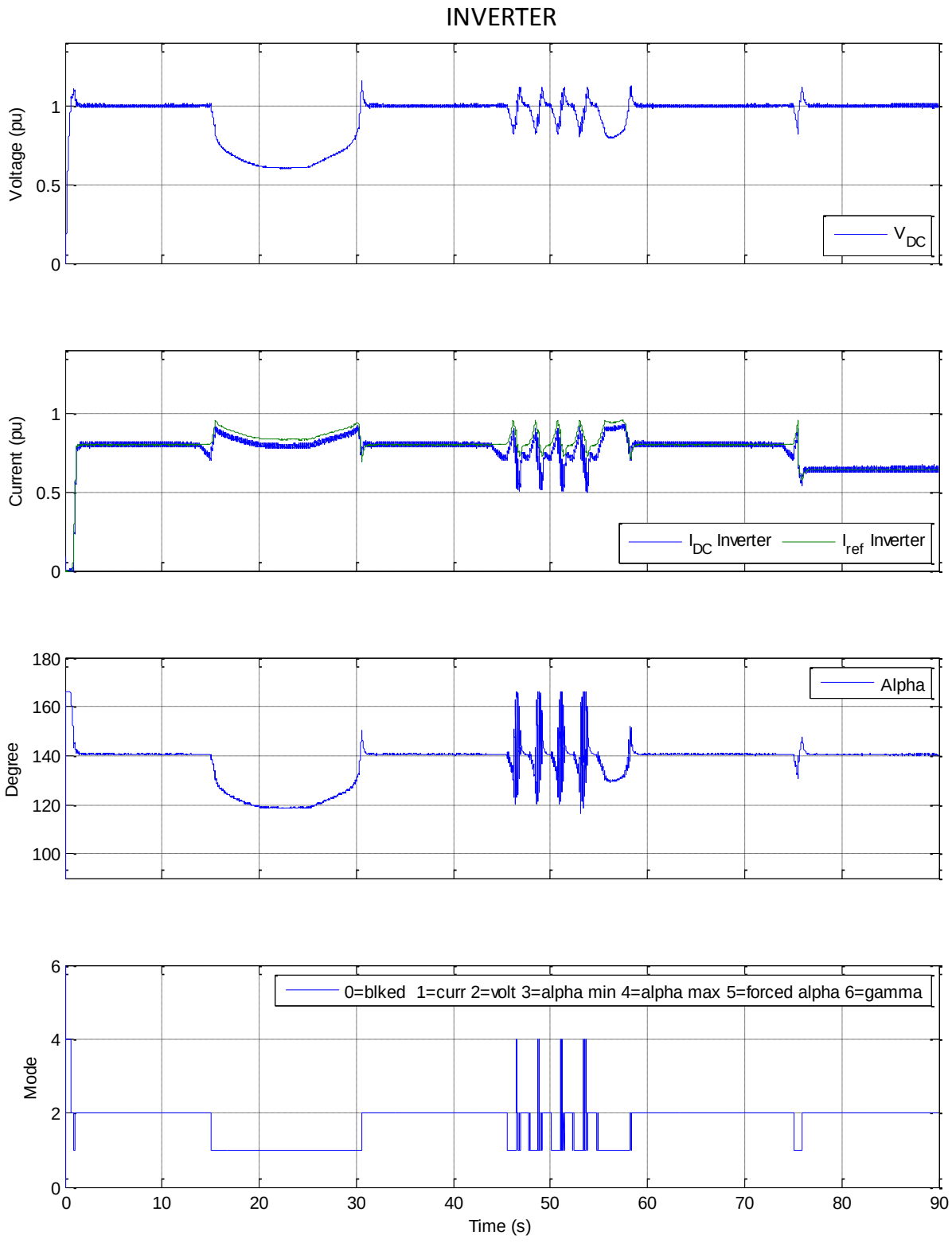


Fig. 92: Rectifier Oscillograms

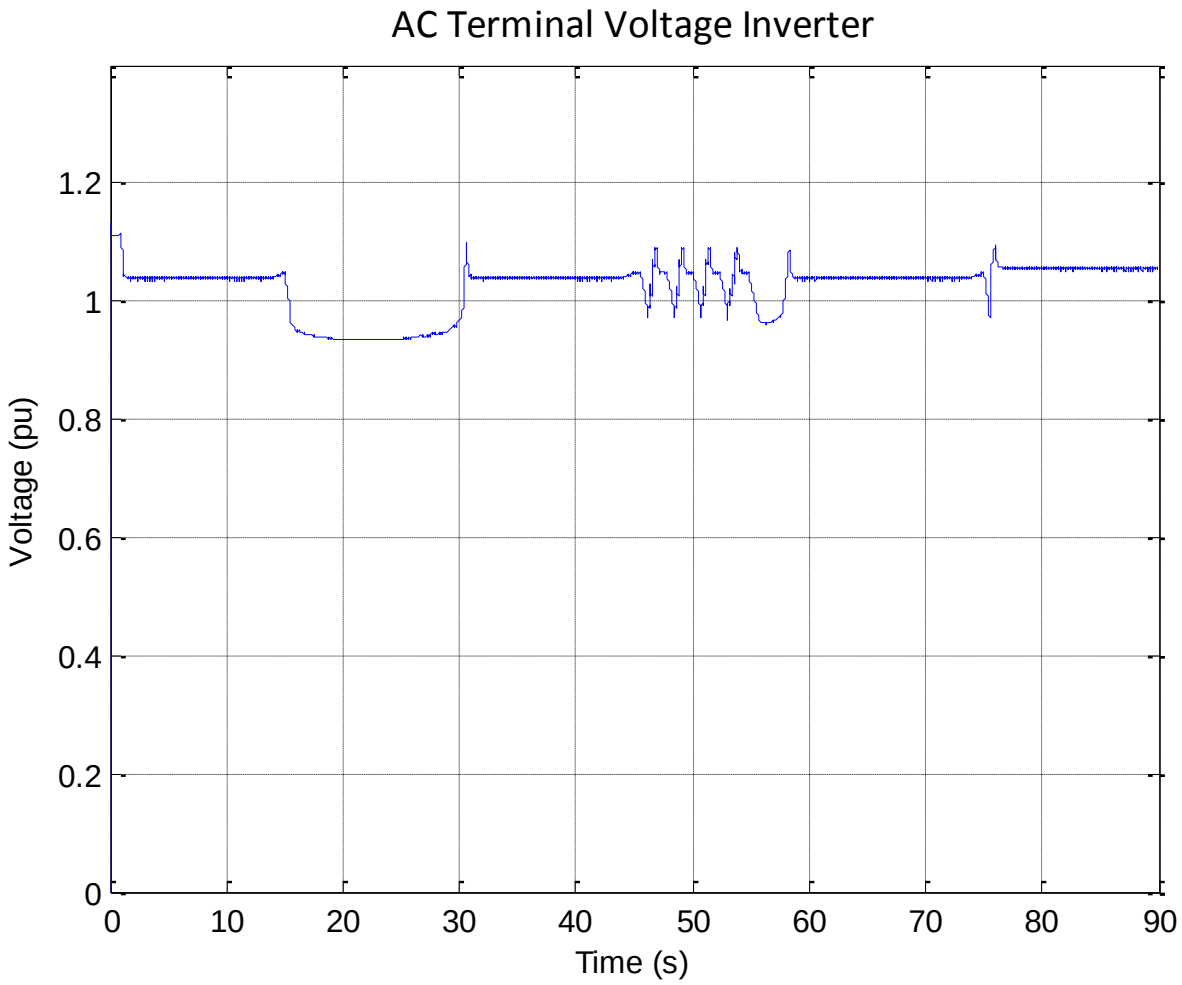


Fig. 93: AC Terminal Voltage Inverter

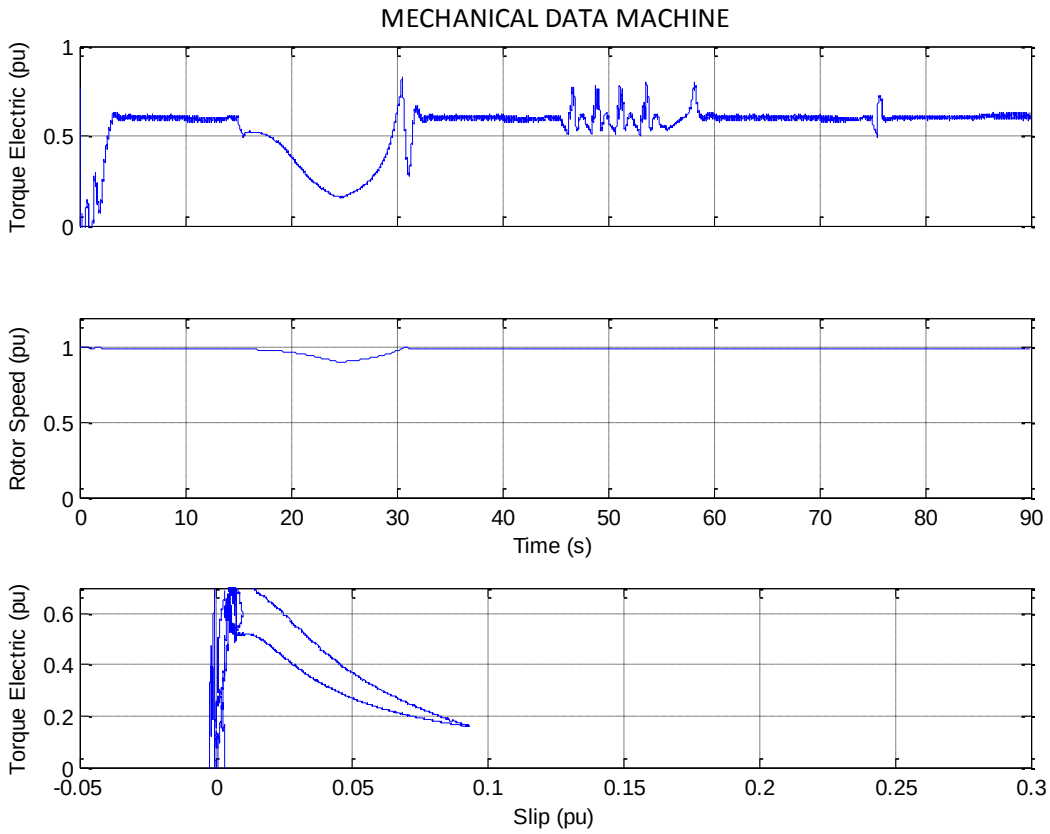


Fig. 94: Mechanical Oscillograms Asynchronous Machine

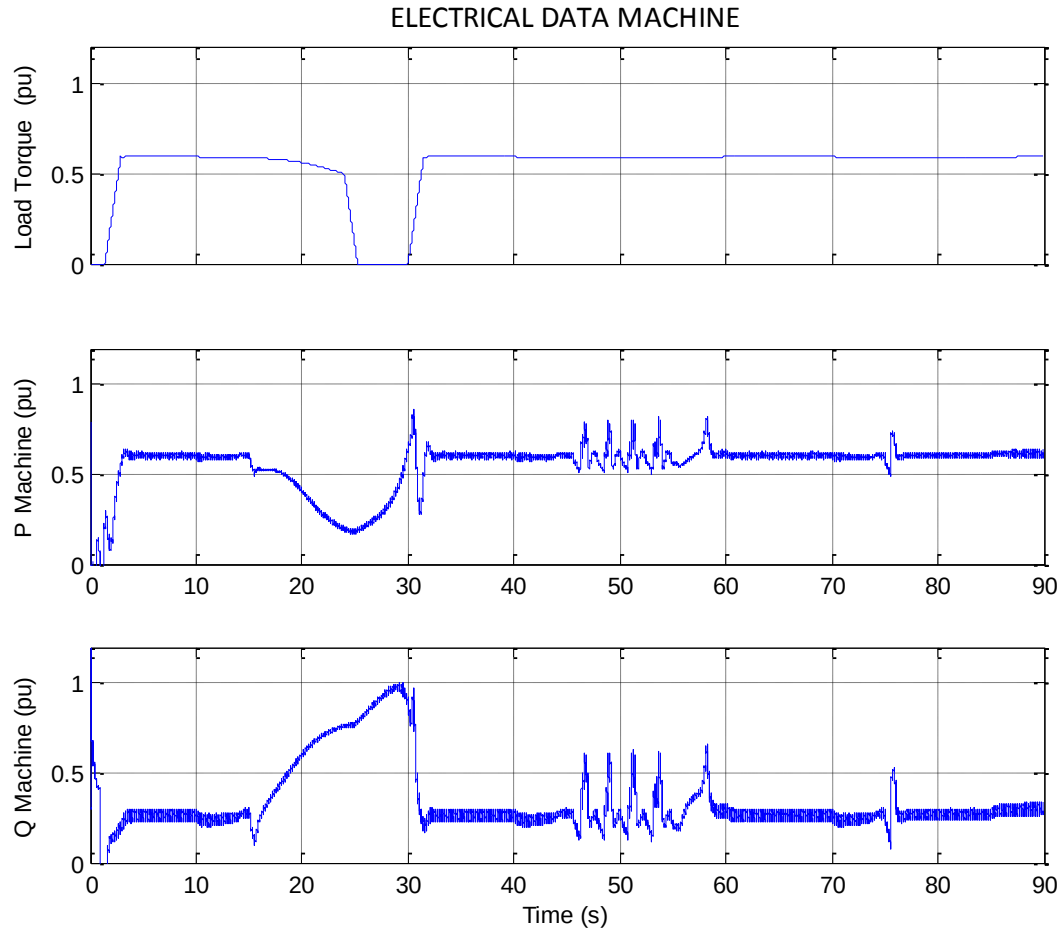


Fig. 95: Electrical Oscillograms Asynchronous Machine

An interesting aspect illustrates Fig.95 that displays the mechanical operation inside the machine. It shows a stalling of the machine that can be prevented by the AVS. Fig.96 shows the decrease of reactive power consumption while the machine is stalling.

Fig. 97 to 100 hold for PSCAD/EMTDC simulations. The results are in accordance with those obtained by real time simulation.

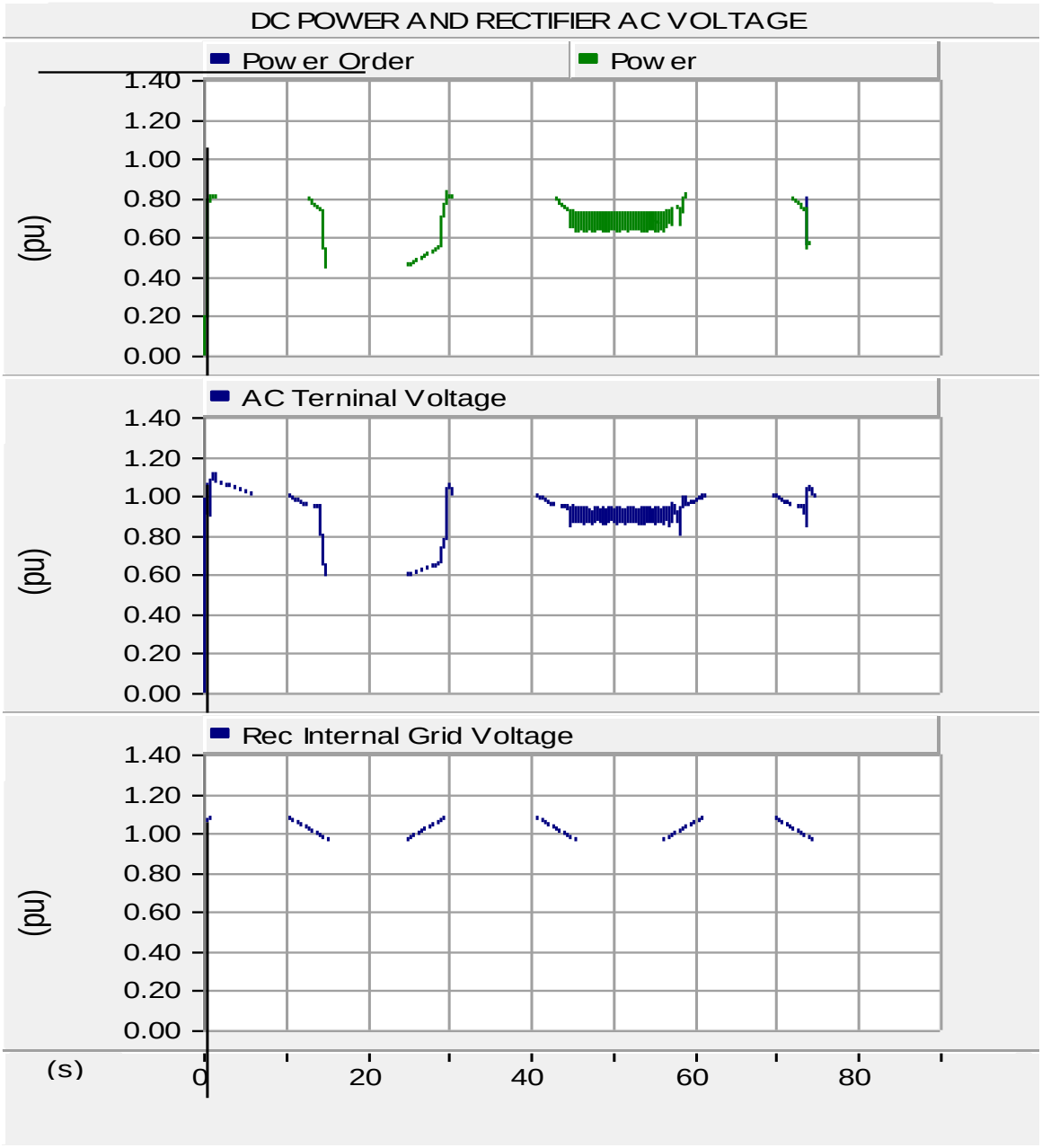


Fig. 96: DC Power and Rectifier AC Voltage

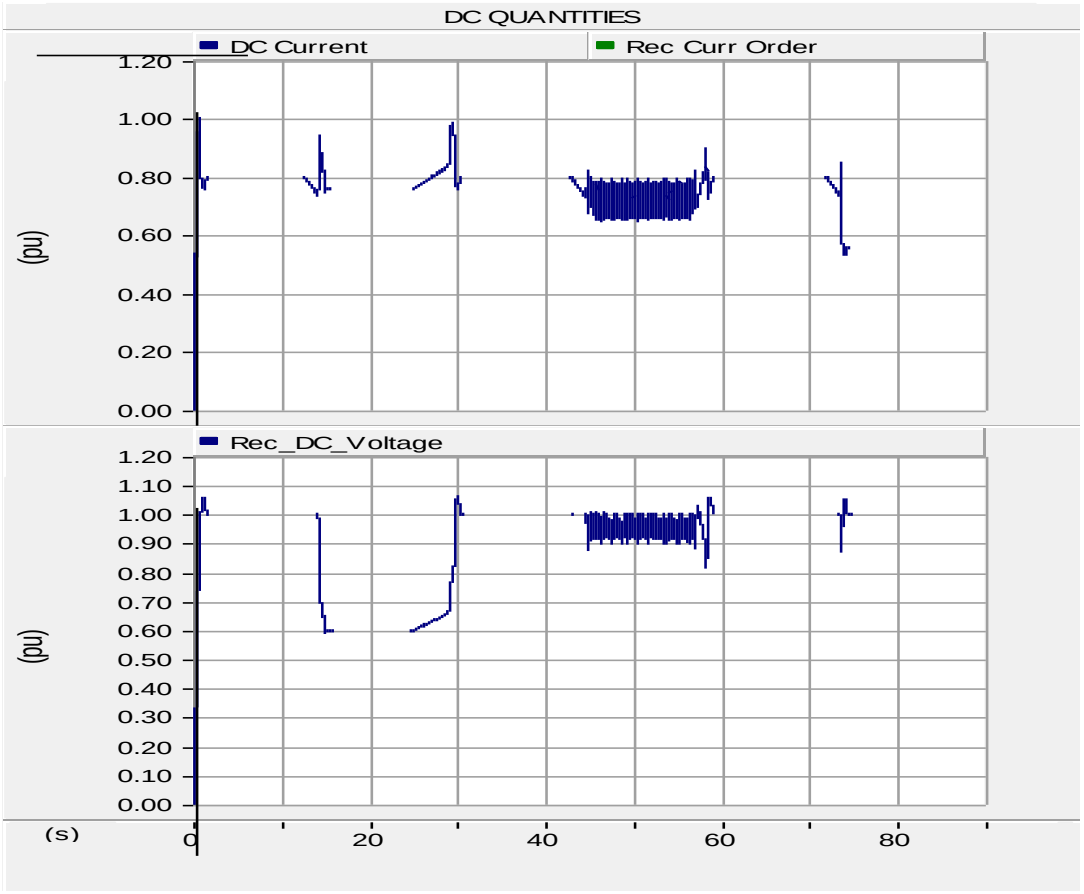


Fig. 97: DC Quantities

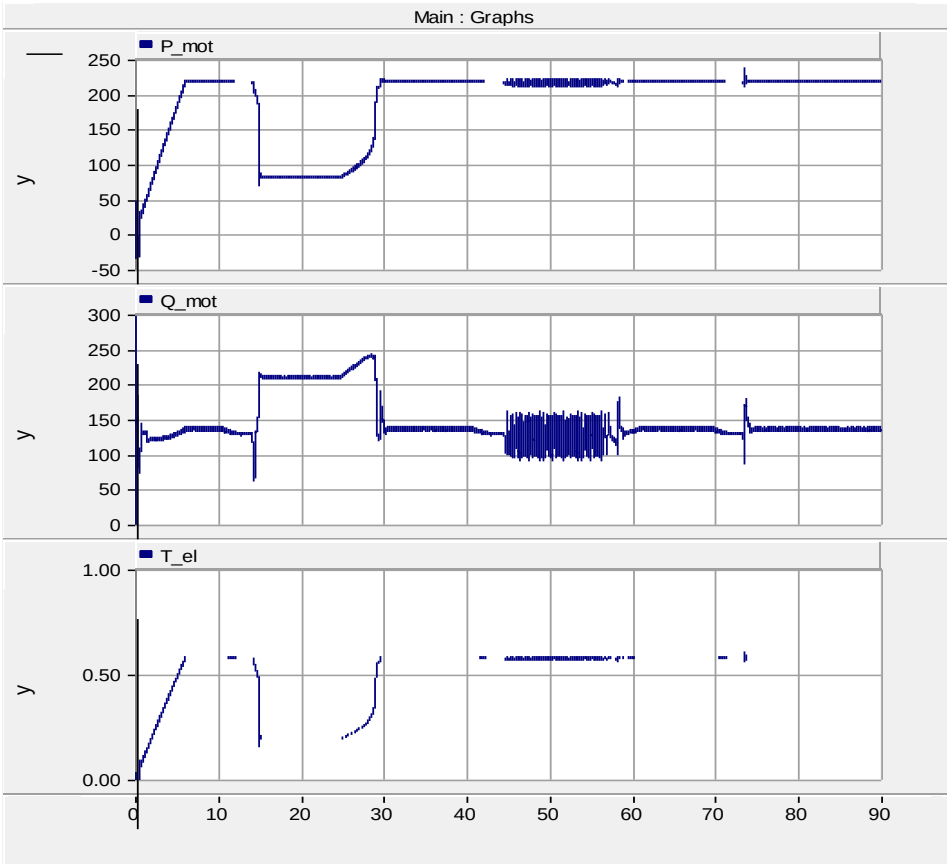


Fig. 98: PSCAD Oscillograms Asynchronous Machine

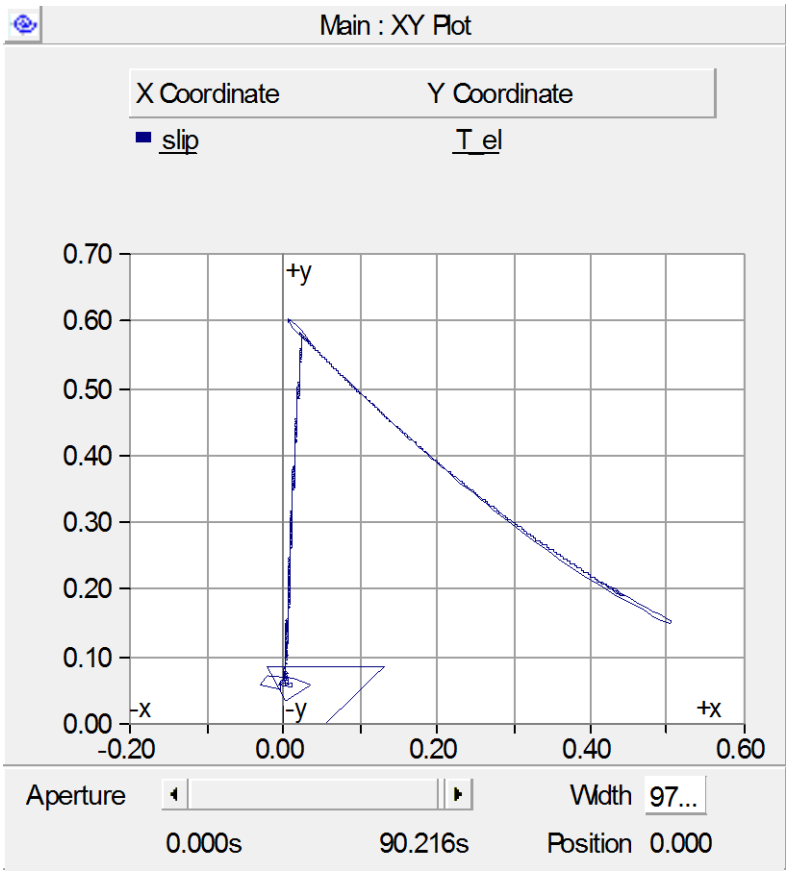


Fig. 99: Slip Asynchronous Machine

4 Further Work

- Prevention of Generation's "free-run" by the AVS and comparison with VDCOL
  - Without Speed-governor (constant mechanical power)
  - With Speed-governor
- Real-Time Stability Margin determination and adaptive power setting
- Performance of the AVS as compared to VDCOL control in multi-machine power system

These studies shall be based on already available material[XVIII] generated by PSCAD/EMTDC simulations. The following is an expert of this.

[XVIII] Kuehn, W., Internal Reports

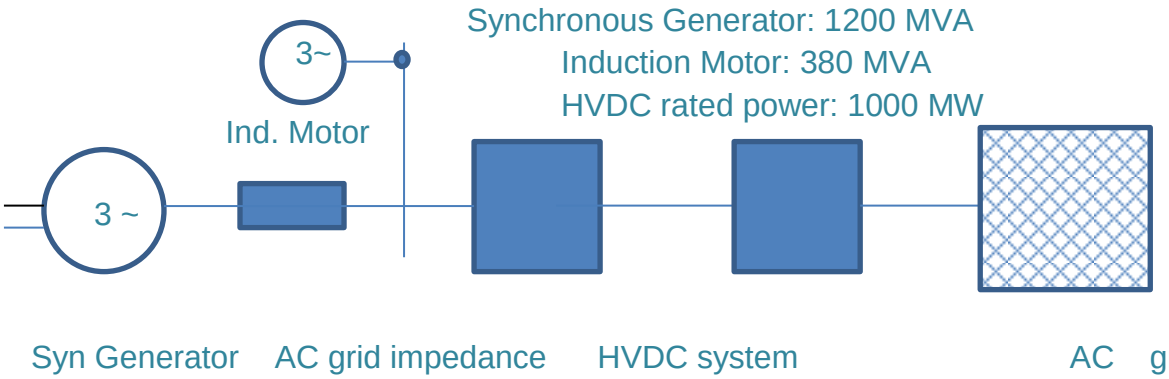
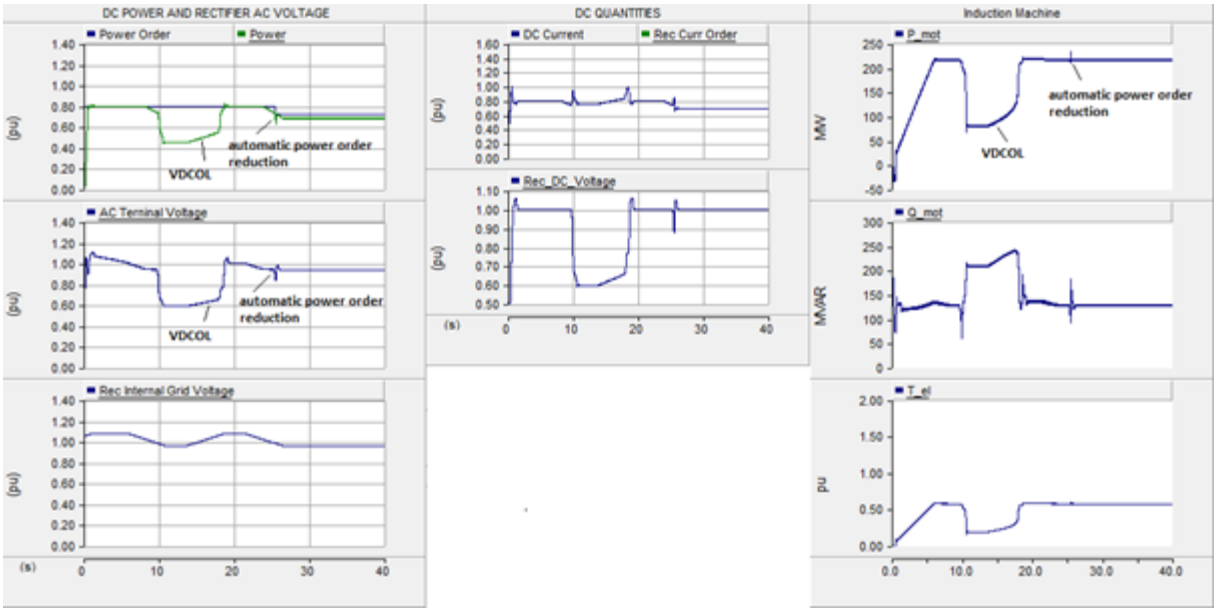


Fig. 1: Synchronous Generator replacing the static voltage source and Induction Motor connected to one HVDC terminal

VDCOL limits the DC current but does not prevent voltage collapse at decreasing AC grid voltage (internal voltage is decreased and increased testwise).

Automatic power order reduction, however, prevents voltage collapse.

It is not the converter alone pulling the voltage down but also the asynchronous machinery. VDCOL with whatever calibration can hardly take into account this machinery on a secure basis.



The figures below hold for a two-area AC transmission system where one area is connected to HVDC transmission and induction machines. Operation with VDCOL is not stable when decreasing the internal grid voltage and reaching the steady state stability limit. The system shows electromechanical swings with negative damping while the automatic voltage stabilizer achieves stability. These results are unique, cannot yet be found in connection with VDCOL anywhere in literature and are worth to be reviewed by ABB.

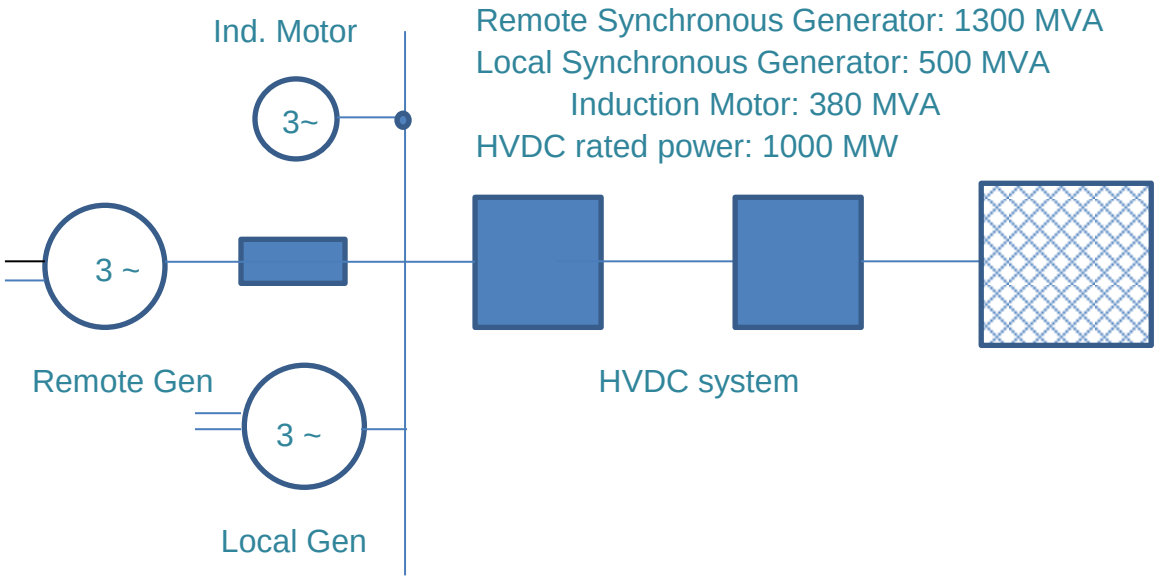
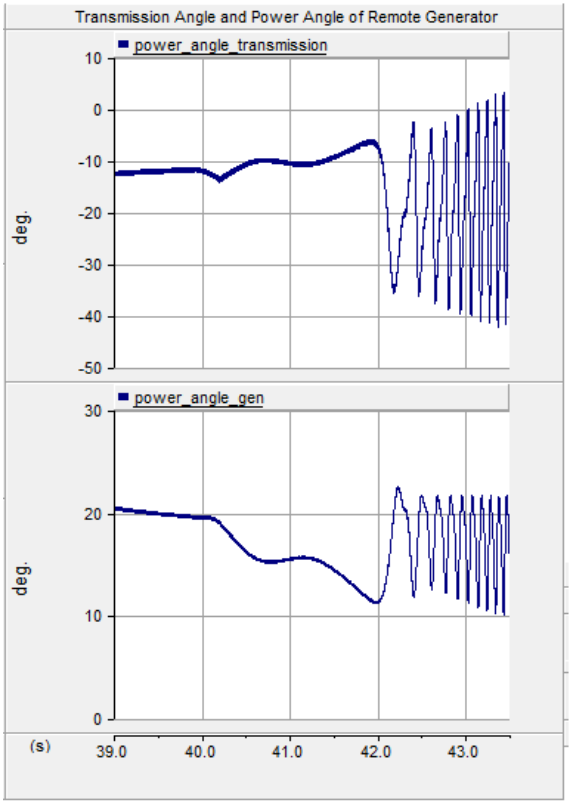
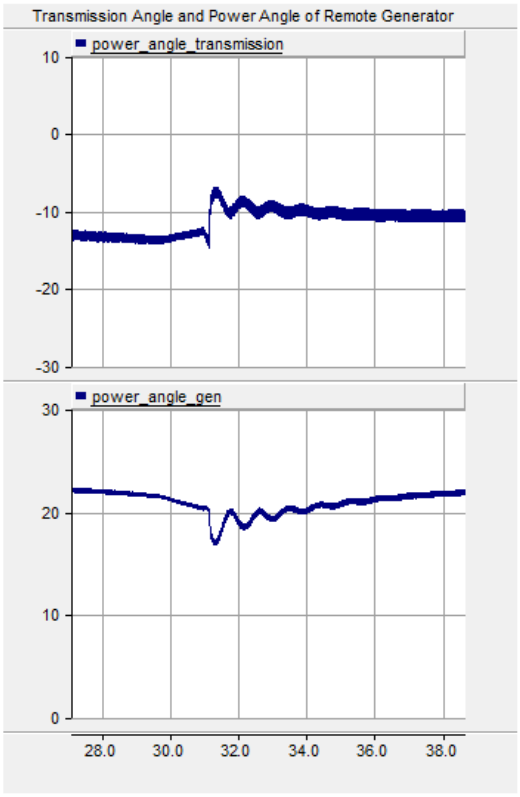


Fig. 2: Two-area system



VDCOL: Unstable electromechanical swings



AVS: Stable at the stability boundary

5 Appendix

Most of the Appendix will only be viewable in the digital version of this thesis which is attached as a DVD to this work. The problem is the large complexity of the real time model and all the data that is used.

5.1 Adjusted Values of the SimPowerSystem Models

Rectifier Regulator Data:

Firing angle α limits	max = 85 deg min = 5 deg
Current Regulator [deg/pu]	Kp = 90 Ki = 1800 Alpha init = 90 deg
Id Meas. Filter H(s)=1/(1+Ts)	T = 0.0012s
VDCOL	See 3.1 VDCOL
Constant alpha mode	Alpha = 166 deg +Rate limit = inf [deg/s] -Rate limit = -inf [deg/s]
Sample Time	Tctrl = Ts = 0.00005s

Inverter Regulator Data:

Firing angle α limits	max = 166 deg min = 92 deg
Voltage Regulator [deg/pu]	Kp = 100 Ki = 700 Alpha init = 90 deg
Current Regulator [deg/pu]	Kp = 90 Ki = 1800 Alpha init = 90 deg
Gamma Regulator [deg/pu]	Kp = 1 Ki = 20 Gamma init = 90 deg
Vd Meas. Filter 2nd Order Low Pass	f0 = 15 Zeta = 0.707
Id Meas. Filter H(s)=1/(1+Ts)	T = 0.0012s
VDCOL	See 3.1 VDCOL
Current Margin	0.042
Voltage Margin	0.02
Constant alpha mode	Alpha = 92 deg +Rate limit = inf [deg/s] -Rate limit = -1000[deg/s]
Sample Time	Tctrl = Ts = 0.00005s

Asynchronous Machine Data:

Machine Type	Squirrel Cage
Nominal Power [VA]	27.54e3*13.804e3
Nominal Voltage [Vrms]	13.804e3 @ 50Hz
Stator Resistance [pu]	Rs = 0.0067
Stator Inductance [pu]	Lls = 0.152
Rotor Resistance [pu]	Rr' = 0.00527
Rotor Inductance [pu]	Llr' = 0.113
Mutual Inductance [pu]	5.71
Inertia Constant H(s)	10
Friction Factor F(pu)	0.008
Pole pairs	2
Initial Conditions	Calculated by Load Flow tool

Transformer for Asynchronous Machine Data:

At least, the Nominal power of the transformer is chosen to be about 6 times higher than the rating of the induction machine.

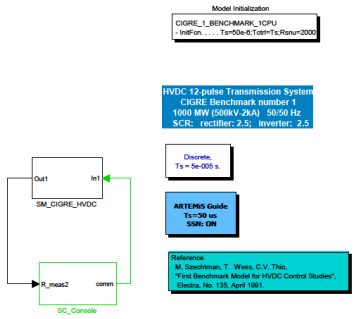
This is mandatory to permit the machine a re-raise of the electro mechanical torque after decreasing and increasing it, with a various internal grid voltage.

Winding 1	Y (Grounded)
Winding 2	Y (Grounded)
Nominal Power [VA]	2400e6 @ 50Hz
Winding 1 parameters	V1 = 400e3 [Ph-Ph voltage] R1 = 0.002 [pu] L1 = 0.08 [pu]
Winding 2 parameters	V1 = 13.804e3 [Ph-Ph voltage] R1 = 0.002 [pu] L1 = 0.08 [pu]
Magnetization Resistance [pu]	Rm = 500
Magnetization Inductance [pu]	Lm = 500
Initial Fluxes	Calculated by Load Flow tool

[XIX]

[XIX] Based on Calculation by Kuehn, W.

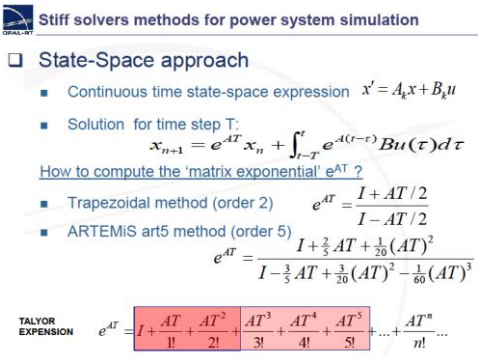
5.2 Description of Opal Cigré Benchmark in SimPowerSystems



Object 1 Cigré Benchmark Description in RT Environment [XX]

"Double-click" to open

5.3 KTH & ABB Workshop



Object 2 Artemis Solver and SSN method [XXI]

[XX] Software description by OPAL-RT TECHNOLOGIES Montreal, Quebec, Canada
[XXI] Dr. Lugi Vanfretti

5.4 VDCOL Function Used In SimPowerSystem Model

Voltage Dependant Current Order Limiter (VDCOL)

"The Voltage Dependant Current Order Limiter (VDCOL) block is used with both the rectifier and the inverter regulators. According to a given DC voltage – DC current profile, this function adapts the current reference sent to the regulators. When significant voltage drops occur at the AC system(s) or faults on the DC link cause DC voltage drops, the current reference is limited according to a linear profile determined by the function's internal parameters. The VDCOL automatically reduces the reference current (Id_ref) set point when VdL decreases. The current-voltage characteristic of the VDCOL is illustrated in Fig.101.

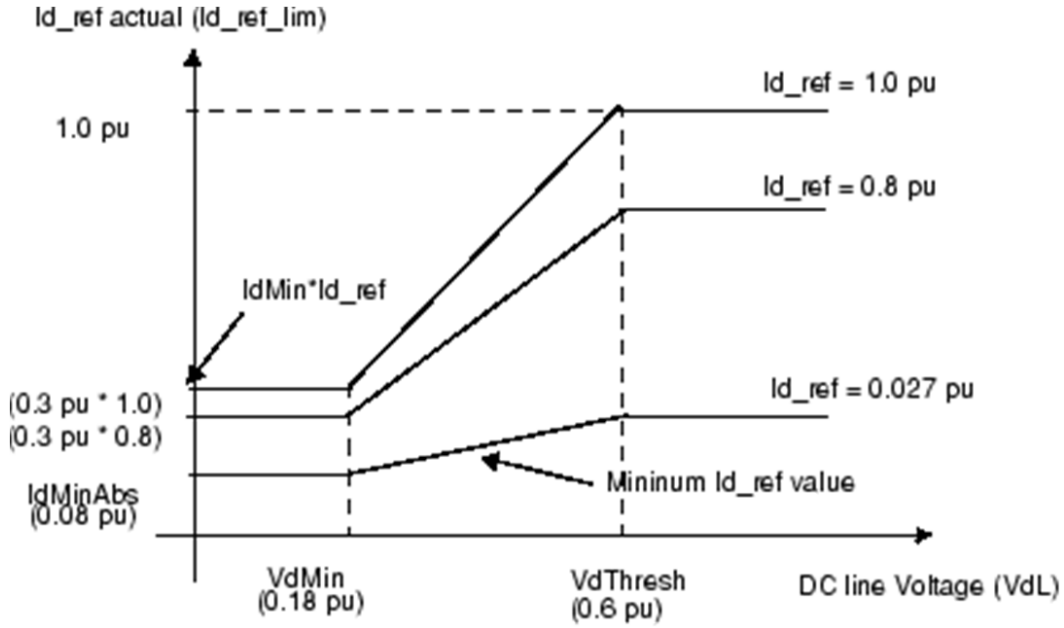


Fig. 100 VDCOL Current-Voltage Characteristic

The Id_ref value starts to decrease when the Vd line voltage falls below a threshold value VdThresh (0.6 pu by default). The actual reference current used by the controllers is named Id_ref_lim. IdMinAbs is the absolute minimum Id_ref value, set at 0.08 pu. When the DC line voltage falls below the VdThresh value, the VDCOL drops instantaneously to Id_ref. However, when the DC voltage recovers, the VDCOL limits the Id_ref rise time with a time constant defined by the parameter Tup (80 ms by default)."[XXII] [XXIII]

In the "own" generic model in section 2.2.1.3 AC voltage DC current order reduction was implemented which should in general be preferred. However, as already mentioned before the performance of VDCOL does not differ much between AC voltage dependent and DC voltage dependent DC current order limitation if the grid is considerably weak, that if the SCR value is around two.

[XXII] SimPowerSystems v4.6, The Mathworks. HVDC demo: "HVDC Transmission System (Thyristor-Based)" by S.Casoria (Hydro-Quebec)
[XXIII] Real-Time Simulation of HVDC Systems with eMEGAsim by OPAL-RT TECHNOLOGIES Montreal, Quebec, Canada; Jean-Nicolas Paquin,Wei Li, Jean Bélanger

5.5 Symbols and Units

Description	Symbol	SI-Unit	Unit Symbol
Direct Voltage	V_{DC}	Volt	V
Direct Current	I_{DC}	Ampere	A
Firing Angle	$alpha$	Degree	$^{\circ}$
AC Grid Voltage Inverter	$V_{AC\_Inverter}$	Volt	V
AC Grid Voltage Rectifier	$V_{AC\_Rectifier}$	Volt	V
AC Grid Voltage (Line-to-Ground, Peak Value)	V_{AC_Extern}	Volt	V
DC Voltage Rectifier	$V_{Rectifier}$	Volt	V
DC Voltage Inverter	$V_{Inverter}$	Volt	V
Resistance DC Line	$Resistance_{Line}$	Ohm	Ω
Current Margin Value	Id_{margin}	Current	A
Short Circuit Ratio	SCR		
Internal Inductance of AC Grid	L_{grid}	Henry	H
Ideal No-Load Direct Voltage	U_{di0}	Volt	V
Rated Direct Voltage	U_{dn}	Volt	V
Apparent Power Converter Transformer	$S_{Transformer}$	VA	VA
Direct Current on Line	I_{dn}	Current	A
Valve Side Voltage Transformer	$U_{l,Bridge}$	Volt	V
Voltage Drop on DC Line	$U_{\Delta,DCLink}$	Volt	V
Real Power	P	W	W
Apparent Power	S	VA	VA
Reactive Power	Q	var	var

5.6 PSCAD Models

Own Developments:

Classic_tier_1.pscx	Classic_tier_2.pscx	Classic_tier_3.pscx
Classic_tier_4.pscx	Classic_tier_5.pscx	

Compatible with PSCAD X4

Pre-designed Models:[XXIV]

CMP_AVS_VDCOL_(WeakRectifierGrid).psc	CMP_AVS_VDCOL_(Weak InverterGrid).psc
CMP_REC_110612.psc	CMP_REC_110612_red_Id_110630.psc
with_motor_110629.psc	with_motor_and_red_Id_110630.psc
syngen_indmotor_110710.psc	2syngen_indmotor_110711.psc

Compatible with PSCAD V4.2.1

5.7 SimPowerSystem Models

All following models require Matlab/Simulink 2010b + OPAL RT Environment.

Case 1 – Weak Grid Investigations:

HVDC_AVS.mdl	
HVDC_AVS_edit2_Rectifier_weak.mdl	HVDC_AVS_edit2_Inverter_weak.mdl

[XXIV] Designed by Kuehn, W.

Case 2 – Performance Test With Asynchronous Machine:

HVDC_AVS_INDUCTION_MACHINE.mdl
HVDC_AVS_INDUCTION_MACHINE_V2.mdl
HVDC_AVS_INDUCTION_MACHINE_V3_new_master_crl.mdl

Case 3 – Performance Test With Synchronous Generator:

HVDC_AVS_SYN_GENERATOR.mdl	SYN_GENERATOR_1200MVA_STATIC_SOURCE.mdl
HVDC_AVS_SYN_GENERATOR_edit.mdl	SYN_GENERATOR_1200MVA_STAB.mdl
HVDC_AVS_SYN_GENERATOR_edit_2.mdl	SYN_GENERATOR_1200MVA_ONLOAD.mdl
HVDC_AVS_SYN_GENERATOR_edit_3.mdl	SYN_GENERATOR_1200MVA_ONLOAD_V2.mdl
HVDC_AVS_SYN_GENERATOR_edit_4.mdl	SYN_GENERATOR_1200MVA_DYNAMICLOAD.mdl
HVDC_AVS_SYN_GENERATOR_edit_5.mdl	
HVDC_AVS_SYN_GENERATOR_edit_6.mdl	

5.8 Matlab Code for Data Plotting and Arrangement

 Plot.m	 Plot_SYN.m
 Data_arrangement.m	 Data_arrangement_SYN.m

It should be mentioned, that the real-time data structures are needed to display any of the SimPowerSystem Data. These are delivered separately on DVD.