Spin-Transfer Torque Magnetoresistive Content Addressable Memory (CAM) Cell Structure Design with Enhanced Search Noise Margin

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***Abstract*— This paper presents a new memory cell structure for content addressable memory (CAM) based on magnetic tunneling junction (MTJ). Each CAM cell uses a pair of differential MTJs as basic storage element and incorporates transistors to greatly improve the cell search noise margin at low sensing current. Using the same design principle, we further develop an area-efficient cell structure for ternary CAM (TCAM), which occupies about 25% less area compared with directly using two CAM cells to form one TCAM cell. The effectiveness of the proposed CAM and TCAM cell structures has been demonstrated by circuit simulation at 0.18μm CMOS technology.**

I. Introduction

As the second-generation magnetoresistive memory, spin-transfer torque (STT) writing type memory recently attracted much attention [1]–[3] and is being considered as one promising candidate for future universal low-power and high-speed nonvolatile digital memory. The basic building block in magnetoresistive memory is magnetic tunneling junction (MTJ), and the data storage is realized by configuring the resistance of MTJs into one of two possible states (i.e., high-resistance state and low-resistance state). STT magnetoresistive memory configures the MTJ resistance through spin-transfer torque switching, which can more easily support technology scaling and reduce the write current compared with traditional magnetoresistive memories [2].

This work is interested in the design of STT magnetoresistive content addressable memory (CAM). Accessed by its content other than address, CAM is ideally suited for any systems that require a large amount of data search, e.g, Ethernet address lookup, cache tags, and data compression, etc. In current practice, CAM uses SRAM-based data storage cells [4]. Being nonvolatile, MTJ-based CAM clearly can be advantageous in many applications. Intuitively, to realize an MTJ-based CAM cell, we may simply use two MTJs that are always complementarily configured to store 1 bit, and the differential MTJ pair forms a voltage divider. Given input voltages corresponding to present input search bit, the voltage divider in each cell delivers either a low or high output voltage, indicating a match or mismatch between the present input search bit and the bit stored in the cell. In fact, such differential 2-MTJ cell structure has been proposed in [5], [6] to improve the sensing speed in magnetoresistive random access memory (RAM). However, as explained later, such a straightforward scheme cannot deliver a large enough search noise margin to realize high-speed and reliable operation in STT magnetoresistive memory.

To address this problem, we develop a new STT magnetoresistive CAM cell structure by integrating MOS transistors into the MTJ-based voltage divider in each cell to greatly improve the search noise margin. It can realize high-speed and reliable CAM operations while maintaining low sensing current through MTJs. Using the same design principle, we further develop an area-efficient cell structure for ternary CAM (TCAM) that stores three values in each cell (i.e., "0", "1", and "don't care"). It can reduce about 25% area compared with a straightforward TCAM cell structure consisting of two CAM cells. We designed match-lines of 32 CAM cells and 32 TCAM cells at 0.18μm CMOS technology. The worst-case search time is about 3.3ns for CAM at sensing current of 45μA and 5ns for TCAM at sensing current of 75μA, where the search noise margin is over 500mV.

II. Background

A. MTJ Basics

One MTJ has two ferromagnetic layers and one oxide barrier layer. The resistance of MTJ depends on the relative magnetization directions of the two ferromagnetic layers, i.e., when the magnetization is parallel (or anti-parallel) as illustrated in Fig. 1, MTJ is in low (or high) resistance state. In STT magnetoresistive memory, parallel and anti-parallel

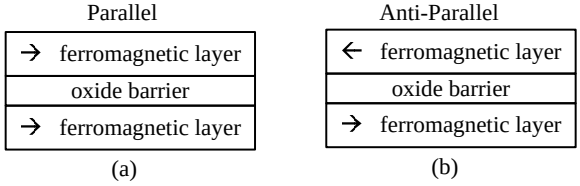

Fig. 1. Two configurations of MTJ: (a) parallel (low resistance) and (b) anti-parallel (high resistance).

magnetization are realized by steering a write current, which must be larger than a threshold, directly through MTJs along two different directions. In current practice, the write current threshold in STT magnetoresistive memory is as low as few hundred μA [2], [3], which directly enables a significant reduction of memory write energy compared with traditional magnetoresistive memories. Let R_h and R_l denote the high

and low MTJ resistance, respectively, we define tunneling magneto-resistance ratio (TMR) as $(R_h - R_l)/R_l$. A large TMR makes it easier to distinguish the two resistance states and hence is highly desirable. As shown in [2], for an MTJ with MgO barrier layer and a dimension of 125nm $\times$ 220nm, the high and low resistance are about 5.5kΩ and 2.5kΩ, respectively, leading to a typical TMR of 155%. Since both write and read are current driven, the sensing current has to be (much) lower than the write current threshold (e.g., 100μA and below) in order to avoid unintentional write during read operation.

B. CAM and TCAM Basics

CAM compares input search word against its own content in parallel, and returns the address of the stored word that matches (i.e., equals to) the input search word. Each stored word associates with an individual match-line (ML) that reports the comparison result (i.e., match or mismatch). As illustrated in Fig. 2(a), CAM typically uses SRAM cell for bit storage. For the purpose of simplification, the figure does not include the access transistors and bit-lines which are used to read and write the SRAM cell. After the match-line is first charged to a high voltage, the search bit is loaded onto the global differential search-line (SL and $\overline{SL}$) and compared with the CAM cells in parallel. A mismatch between the search bit and the stored bit turns on one pulldown path, which will discharge the match-line; while a match turns off both pulldown paths. TCAM is a special type of CAM, in which each cell can store three values, including logic 0, logic 1, and don't care (denoted as X). During a search operation, a cell that stores X always reports a match regardless to whether the input search bit is logic 0 or 1. Typically two CAM cells are used to implement one TCAM cell.

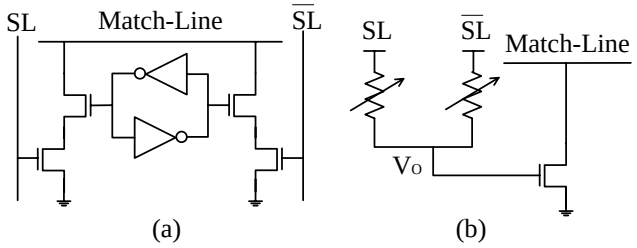

Fig. 2. Structure of (a) a typical SRAM-based CAM cell and (b) a straightforward MTJ-based CAM cell. For the purpose of simplicity, we omit the transistors and control lines for writing/reading the cell in both (a) and (b).

C. A Straightforward MTJ-Based CAM Cell Structure

Fig. 2(b) presents a possible straightforward MTJ-based nonvolatile CAM cell structure consisting of two differential MTJs (i.e., one MTJ has high resistance and another has low resistance). Driven by the input differential search-line, the two MTJs form a voltage divider with the output voltage V_o. Let V_h and V_l denote the high and low voltages on the differential search-line. Recall that R_h and R_l represent the high and low resistance of MTJs, and $TMR = (R_h - R_l)/R_l$. Hence the output voltage V_o can be either $V_o^{(h)} = V_h + (V_l - V_h)/(2 + TMR)$ or $V_o^{(l)} = V_l + (V_h - V_l)/(2 + TMR)$, where $V_o^{(h)} > V_o^{(l)}$. Clearly, to make such simple MTJ-based CAM cell functional, $V_o^{(h)}$ and $V_o^{(l)}$ should be able to turn on and off the nMOS transistor on the pulldown path, and the search noise margin $V_o^{(h)} - V_o^{(l)} = (V_h - V_l)/(1 + 2/TMR)$ should be sufficiently large to ensure operation reliability and achieve high search speed. However, since $V_h - V_l$ cannot be too large in order to avoid unintentional write, such simple CAM cell structure may not be able to have sufficient search noise margin. For example, let us consider MTJs whose R_h and R_l fall into the range of 5$\sim$6kΩ and 2$\sim$3kΩ, respectively. If the current through MTJs is set to be 60μA during the search operation, the worst-case noise margin of V_o is only about 120mV, which may result in unsatisfactory reliability and speed performance.

III. Proposed MTJ-Based CAM/TCAM Cell Structures with Enhanced Search Noise Margin

This section first presents a simple design principle to improve the noise margin by inserting transistors into the differential resistor pair, then applies this design principle to design cell structures of MTJ-based CAM and TCAM.

A. Basic Design Principle

The underlying basic principle of this work is to insert transistors into the differential MTJ voltage divider to amplify the search noise margin. It is illustrated in Fig. 3. Let

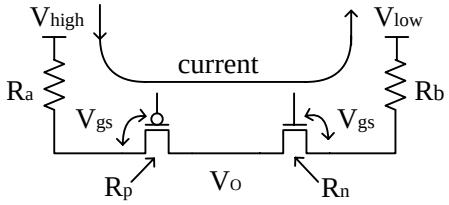

Fig. 3. The basic principle of the proposed sensing circuit.

R_n and R_p represent the ON resistance of the nMOS and pMOS transistors, respectively, which are modulated by the gate-source voltage V_{gs}. Such resistance-voltage dependency can potentially improve the search noise margin, which is intuitively explained as follows: If $R_a = R_l < R_b = R_h$, the noise margin is determined by $(R_h + R_n)/(R_l + R_p)$. Due to the relatively large voltage drop across R_b, V_{gs} of the nMOS transistor is relatively small and makes R_n relatively large. Meanwhile, due to the small voltage drop across R_a, V_{gs} of the pMOS transistor is relatively large and makes R_p relatively small. Hence the ratio $(R_h + R_n)/(R_l + R_p)$ tend to be relatively large, leading to an improved search noise margin. Similarly, if $R_a = R_h > R_b = R_l$, the noise margin may also improve due to the same resistance-voltage dependency.

The effectiveness of this basic design principle is demonstrated using the following example. Again, consider MTJs whose R_h and R_l fall into the range of 5$\sim$6kΩ and 2$\sim$3kΩ, respectively. Using Cadence tool set with 0.18μm CMOS

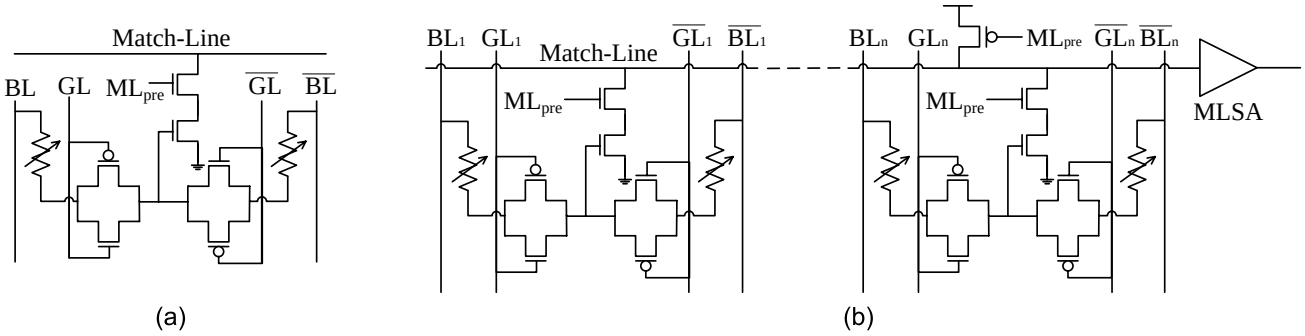

Fig. 4. (a) Proposed CAM cell structure, and (b) a match-line with n cells. For the purpose of simplicity, we omit the transistors and control lines for writing/reading each CAM cell.

technology design kit, we designed the circuit shown in Fig. 3 and obtained the results listed in Table I. We set V_{high} as 1.6V and V_{low} as -0.1V, and set the gate voltages of the nMOS and pMOS transistors as 1.05V and 0V, respectively. A noise margin of over 500mV is achieved with less than 50μA sensing current. In comparison, under the same sensing current, only about 90mV noise margin can be achieved without inserting the transistors into the MTJ pair.

TABLE I
SIMULATION RESULTS TO DEMONSTRATE THE BASIC DESIGN PRINCIPLE.

R_a (KΩ)	R_b (KΩ)	V_o (mV)	current (μA)
3	5	857.0	42.66
5	3	323.5	43.83

B. CAM Cell Structure Design

Applying the above basic design principle, we develop a CAM cell structure as illustrated in Fig. 4(a), where two pairs of nMOS and pMOS transistors are inserted between the two differential MTJs. The gate of each pair of nMOS and pMOS transistors is driven by one gate-line (i.e., GL and $\overline{GL}$). During the search operation, the differential gate-line always turns off one pMOS transistor in one pair and one nMOS transistor in another pair, hence the cell circuit is always equivalent to the one shown in Fig. 3. The voltages of the differential bit-line and differential gate-line should be appropriately determined so that the output of the voltage divider can turn on or off the nMOS transistor on the pulldown path. Let $V_o^{(h)}$ and $V_o^{(l)}$ denote the high and low output of the voltage divider, ideally we should make $(V_o^{(h)}+V_o^{(l)})/2$ equals to the threshold voltage of the nMOS transistor on the pulldown path.

As illustrated in Fig. 4(b), all the CAM cells in the same word share one match-line. The search operation of the MTJ-based CAM has two phases: first all the match-lines are pre-charged to the supply voltage by setting ML_{pre} to 0, then we set the voltages of each pair of differential bit-line and differential gate-line according to the search bit and set ML_{pre} to 1. Only when the entire word matches the input search word, its match-line can remain a high voltage, otherwise at least one cell will turn on the pulldown path to discharge the match-line. A match-line sense amplifier (MLSA) can be used to speed up the search operation.

A match-line with 32-bit CAM cells is designed using 0.18μm CMOS technology. R_h and R_l of MTJs fall into the range of 5$\sim$6kΩ and 2$\sim$3kΩ, and the voltages of the bit-line and gate-line keep the same with the above design example. Fig. 5 shows the simulated worst-case search operation waveform, i.e., there is only 1-bit mismatch and the differential MTJs in the mismatch cell have the resistance of 3kΩ and 5kΩ. Results suggest that the worst-case search delay of 3.3ns can be achieved, leading to over 250MHz search frequency.

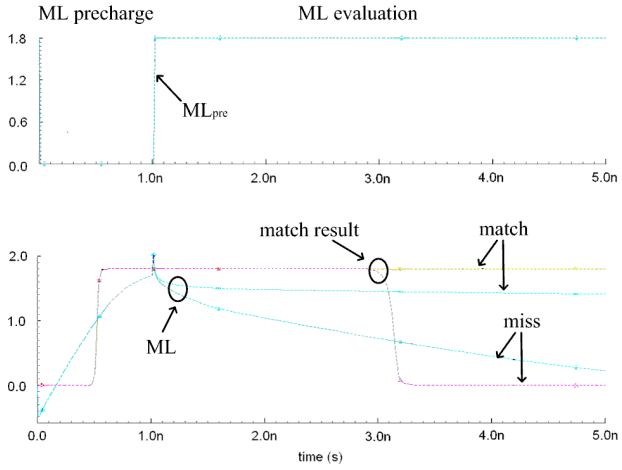

Fig. 5. Simulated worst-case CAM search operation waveform.

C. TCAM Cell Structure Design

It may be intuitive that we can directly use the above MTJ-based CAM cell as a TCAM cell, where don't care X can be represented by configuring the two MTJs into the same resistance state. Recall that the operation of the MTJ-based CAM cell depends on the resistance difference between the two MTJs. Even though the two MTJs are in the same resistance state, their resistance may still have significant difference due to the process variation, e.g., as shown in the above design example, the high resistance may vary between 5kΩ and 6kΩ and the low resistance may vary between 2kΩ

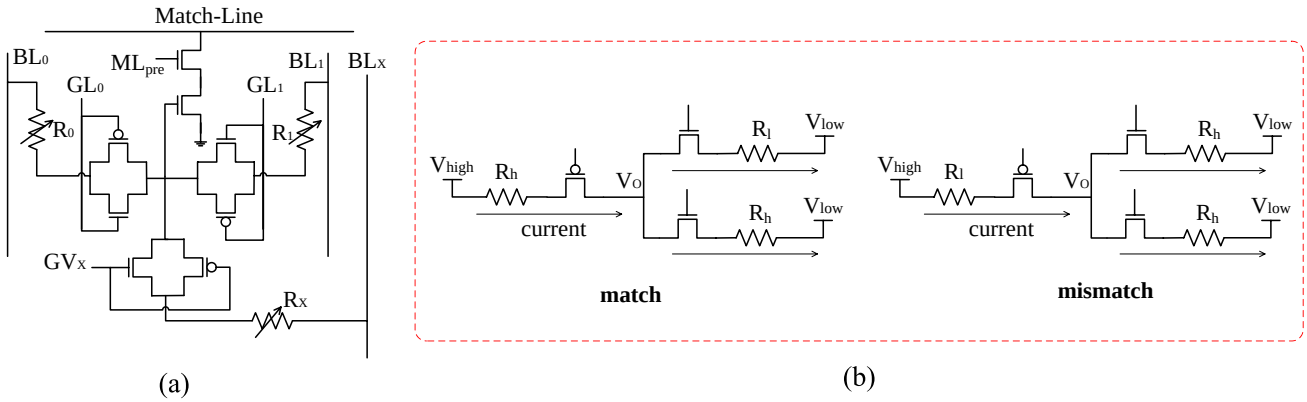

Fig. 6. (a) Proposed TCAM cell structure and (b) simplified equivalent circuits during search operation corresponding to match (i.e., output voltage V_o is low and cannot turn on the nMOS transistor on the pulldown path) and mismatch (i.e., output voltage V_o is high and can turn on the nMOS transistor on the pulldown path).

and 3kΩ. Such resistance variation will largely degrade the search noise margin and even result in malfunction, hence we cannot build a TCAM cell using only one CAM cell.

Instead of using two CAM cells to build a TCAM cell, we develop an area-efficient TCAM cell structure that contains three MTJs, as illustrated in Fig. 6(a). The three MTJs (i.e., R_0, R_1, and R_x) are configured based on one-cold coding scheme that configures only one MTJ to low resistance state, i.e., $\{R_0, R_1, R_x\}$ is $\{R_l, R_h, R_h\}$ for logic 1, $\{R_h, R_l, R_h\}$ for logic 0, and $\{R_h, R_h, R_l\}$ for don't care X. During the search operation, the bit-line BL_x always has a low voltage while the differential bit-lines BL_0 and BL_1 are set according to the input search bit. Fig. 6(b) shows the simplified equivalent circuit when the TCAM cell matches or mismatch the input search bit.

With the same setup as in the above CAM design example, we designed a math-line with 32 TCAM cells. Circuit simulation results show that V_o in each TCAM cell is below 371.9mV in case of match and above 877.8mV in case of mismatch, leading to a search noise margin of 505.9mV. The worst-case sensing current through one MTJ is about 75μA. Fig. 7 shows the simulated worst-case TCAM search waveform, which suggests a less than 5ns worst-case search delay.

IV. Conclusions

This paper presents a new MTJ-based CAM cell structure that can achieve large search noise margin at small sensing current. The same design principle is further applied to develop an area-efficient TCAM cell structure that reduces about 25% area compared with directly using two CAM cells to form one TCAM cell. Match-lines with 32 CAM cells and TCAM cells are designed at 0.18μm CMOS technology to demonstrate the proposed design techniques. Assuming the resistance of MTJs may fall into the range of either 5∼6kΩ or 2∼3kΩ, circuit simulations show that both CAM and TCAM cells can achieve over 500mV search noise margin, and the worst-case search time is about 3.3ns in CAM and 5ns in TCAM.

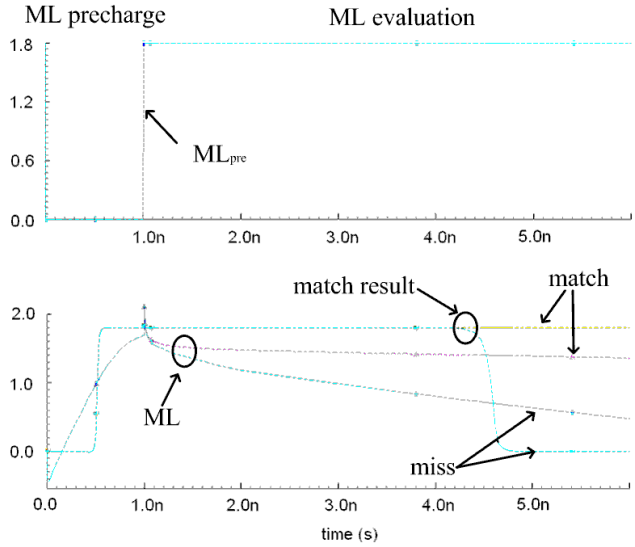

Fig. 7. Simulated worst-case TCAM search operation waveform.

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