

# Use of Parity Checks Inherent in LDPC Codes for Dominant Error Events Detection and $k$ -Constraint Enforcement

Fei Sun and Tong Zhang

**Abstract**—In this paper, we propose to leverage the simple and explicit parity checks inherent in low-density parity-check (LDPC) codes to realize dominant error events detection without code rate penalty. This is enabled by enforcing a very weak constraint on LDPC code parity check matrix structure. Such a constraint can be readily satisfied by most structured LDPC codes ever studied in the open literature such as quasi-cyclic (QC) LDPC codes. Moreover, this zero-redundancy dominant error events detection can be further extended to handle the deliberate bit errors when deliberate bit-flipping is used to enforce  $k$ -constraints. The effectiveness of the proposed methods has been demonstrated through computer simulations.

**Index Terms**—Low-density parity-check (LDPC), dominant error events,  $k$ -constraint

## I. INTRODUCTION

It is well known that, besides error correcting codes (ECC), modern magnetic recording systems typically use two other types of codes, including parity codes and modulation codes, to improve the overall system performance. Parity codes are used to detect the dominant error events at the output of trellis detectors, and once the parity constraints are violated, error event correlations are invoked to locate the most likely dominant error event. The effectiveness of such post-detection processing has been well demonstrated in the open literature [1]–[3]. Modulation codes are used to enforce certain modulation constraints on the bit stream to be stored. The most widely used modulation constraint is the run-length limited (RLL)  $k$ -constraint [4], [5]. The  $k$ -constraint demands that at most  $k$  consecutive 0's may appear in the bit stream, which is essential to facilitate the timing recovery. Such constraints are typically enforced by using standard RLL codes. Since both parity codes and RLL codes inevitably incur code rate penalty, trade-offs between their powerfulness and code rate penalty must be carefully evaluated in practical system design.

Low-density parity-check (LDPC) codes have recently attracted much attention (e.g., see [6]–[9] etc.) because of their potential applications in magnetic recording systems due to their great promise of delivering stronger error correction capabilities over Reed-Solomon codes. This work concerns the realization of dominant error events detection and  $k$ -constraint enforcement for magnetic recording systems using LDPC codes. Since LDPC code decoders demand soft input, soft-output trellis detectors should be used in this context. Well-known soft-output trellis detection algorithms include BCJR algorithm [10] and soft-output Viterbi algorithm (SOVA) [11]

and their variants. Irrelevant to which soft-output detection algorithm is being used, we still can use standard parity codes to detect dominant error events on the hard decisions of the trellis detection soft output. Once the parity constraints are violated, we may use the standard error correlations to locate the most likely dominant error event and erase the corresponding soft output (i.e., set their magnitudes to zero). Clearly, the code rate penalty still exists. In this work, we propose to use the simple parity checks inherent in LDPC codes to detect the dominant error events without code rate penalty. This is enabled by enforcing a very weak constraint on the LDPC code parity check matrix structure. Such a constraint can be easily satisfied by most structured LDPC codes ever studied in the open literature, such as quasi-cyclic (QC) LDPC codes, a family of LDPC codes that have been most widely studied and shown great promise from both error correction performance and efficient VLSI implementation perspectives [12]–[14].

The enforcement of  $k$ -constraint tends to be nontrivial since RLL code decoders typically appear before ECC decoders and only generate hard output. To tackle this issue, researchers have recently developed different approaches that may fall into two categories based on whether RLL codes are explicitly used: (i) RLL codes are still explicitly used and their concatenation with ECC codes that demand soft input are enabled through reverse concatenation and/or soft RLL code decoding [7], [15]–[17]; (ii) Instead of using RLL codes, the  $k$ -constraint is enforced through deliberate bit-flipping [18]–[20]. This work is interested in the second category above. In this context, although code rate penalty is eliminated, the deliberate bit errors may greatly degrade the system performance. Therefore, the critical issue is how to most effectively correct those deliberate bit errors. In [18], [20], the correction of such deliberate bit errors solely depends on ECC, while in [19] deliberate bit errors are handled jointly by post-detection processing and ECC. In this work, motivated by the basic idea in [19], we enhance the above proposed zero-redundancy dominant error events detection scheme to further handle those deliberate bit errors. Notice that in [19] an error-detection code for dominant error event detection explicitly concatenates with the conventional RS code, while in this work we propose to use the parity check constraints inherent in LDPC code structure to perform error event detection.

Based on the above discussion, we may conclude that the key features of this work include (i) we propose to leverage the parity checks inherent in LDPC codes to realize dominant error events detection without code rate penalty, and (ii) we further enhance the zero-redundancy dominant error events detection scheme to detect deliberate bit errors inserted for  $k$ -constraint

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enforcement. For the purpose of evaluation, we considered a magnetic recording read channel that uses SOVA soft-output trellis detection and a length-8136 rate-8/9 regular-(4, 36) QC-LDPC code. Simulation results successfully demonstrate the effectiveness of the proposed methods.

## II. PROPOSED DESIGN METHODS

To detect the dominant error events at the output of trellis detectors, appropriate single or multiple parity codes with short codeword length (e.g., 64 bits) must be formed along the bit stream. In current practice, this is realized by explicitly inserting parity bits into the bit stream, which directly results in code rate penalty. Hence the error detection mechanism being used must be carefully determined subject to the trade-off between its powerfulness and the code rate penalty. Since an LDPC code can be considered as a subcode of a set of very short (e.g., 36 bits) single parity codes, it is reasonable to expect that we may arrange the LDPC code encoding in such a way that a subset of its very short single parity super-codes will explicitly and consecutively appear in each LDPC codeword. Intuitively, this can be directly leveraged to realize the dominant error events detection. Such an arrangement will exist as long as the LDPC code parity check matrix has the following property: The code parity check matrix can always be permuted through column and row permutations so that it contains a row-wise sub-matrix (i.e., this sub-matrix has the same number of columns as the code parity check matrix itself) in which each row contains an all-1's sub-vector and all these sub-vectors are non-overlapped and span over all the columns. This can be further described as follows: for the code parity check matrix  $\mathbf{H}$ , there exists a column/row permutation  $\Pi_D$  so that  $\tilde{\mathbf{H}} = \Pi_D(\mathbf{H}) = [\mathbf{H}_D^T, \mathbf{H}_R^T]^T$ , where the row-wise sub-matrix  $\mathbf{H}_D$  has the structure as shown in Fig. 1. We note that the remaining entries in this row-wise sub-matrix must be zero (i.e., those in the grayed region in Fig. 1) are all zeros.

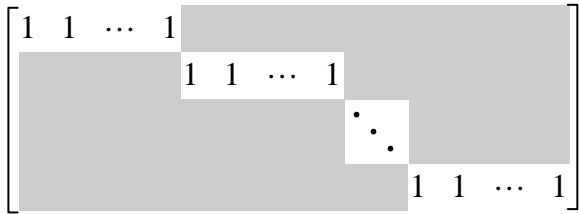


Fig. 1. The structure of the row-wise sub-matrix  $\mathbf{H}_D$  that contains a set of non-overlapped all-1's sub-vectors spanning over all the columns.

If we use  $\tilde{\mathbf{H}}$  for the LDPC code encoding and suppose the sub-matrix  $\mathbf{H}_D$  has  $M_D$  rows, the bits in each LDPC codeword explicitly form  $M_D$  consecutive single parity codewords. These explicit single parity constraints can be used to detect the dominant error events. If multiple parity codes are required to detect the dominant error events, we may interleave multiple single parity codes together, which nevertheless will increase the parity codeword length. The above constraint on LDPC code parity check matrices is very weak and can be readily met by most structured LDPC codes that have been studied in the open literature. For example, for QC-LDPC codes that

are of the most interest to magnetic recording, its parity check matrix has the following form

$$\begin{bmatrix} \mathbf{H}_{1,1} & \mathbf{H}_{1,2} & \cdots & \mathbf{H}_{1,n} \\ \mathbf{H}_{2,1} & \mathbf{H}_{2,2} & \cdots & \mathbf{H}_{2,n} \\ \cdots & \cdots & \ddots & \cdots \\ \mathbf{H}_{m,1} & \mathbf{H}_{m,2} & \cdots & \mathbf{H}_{m,n} \end{bmatrix},$$

where each sub-matrix  $\mathbf{H}_{i,j}$  is a circulant<sup>1</sup>. If there exist a row-wise sub-matrix

$$\begin{bmatrix} \mathbf{H}_{i_1,1} & \mathbf{H}_{i_1,2} & \cdots & \mathbf{H}_{i_1,n} \\ \cdots & \cdots & \ddots & \cdots \\ \mathbf{H}_{i_s,1} & \mathbf{H}_{i_s,2} & \cdots & \mathbf{H}_{i_s,n} \end{bmatrix},$$

in which each column has a single 1, then it is guaranteed that the entire code parity check matrix can be permuted to the desired structure described above.

During the practical operation, when one parity constraint is violated at the output of trellis detectors, error event correlations will be carried out to search the most likely dominant error event among a pre-specified list of dominant error events while assuming a single dominant error event occurs. The most likely dominant error event is defined as

$$\hat{e} = \arg \min_{e \in \mathcal{L}, p(\hat{d}+e)=0} \|h(\hat{d}+e) - r\|^2, \quad (1)$$

where  $\mathcal{L}$  is the pre-specified list of dominant error events,  $\hat{d}$  is the hard decision of trellis detector output,  $p(\hat{d}+e)$  denotes the parity check result,  $h(\cdot)$  denotes the magnetic recording channel function, and  $r$  is the hard decision of trellis detector input. Readers are referred to [1], [2] for a detail description on the realization of error event correlations. Once the most likely dominant error event is identified, we simply set the magnitudes of the corresponding soft output to zero. The pre-specified list of dominant error events is typically determined based on extensive computer simulations.

In the above, we presented the idea of using LDPC codes to realize dominant error events detection. Following the same principle proposed in [19], we may further use such inherent error detection capability to support zero-redundancy  $k$ -constraint enforcement based on deliberate bit-flipping. This leads to an overall system structure as shown in Fig. 2. Deliberate bit-flipping inserts a single 1 or multiple-bit vector that are detectable by the post-detection processing into the bit stream to enforce the  $k$ -constraint. The post-detection processing performs parity check, error event correlations, and soft output erasure. Once the parity constraint is violated, we first search all the possible occurrences of deliberate bit-flipping. If only one is found, we consider the deliberate bit-flipping as one possible error event and add an all-0 entry into the dominant error events list, otherwise we assume the deliberate bit-flipping does not occur and keep the original list of dominant error events. The standard error event correlations and soft-output erasure are subsequently carried out based on present dominant error events list. Fig. 3 illustrates the operation flow of the proposed post-detection processing.

<sup>1</sup>A circulant is a square matrix in which each row is the cyclic shift of the row above it, and the first row is the cyclic shift of the last row.

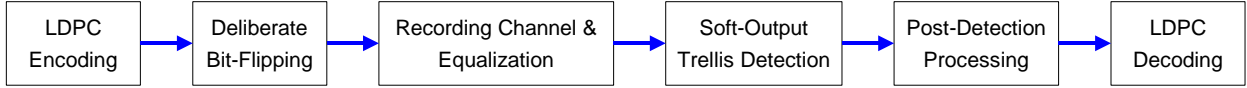


Fig. 2. The overall system structure that uses parity checks inherent in LDPC codes for dominant error detection and  $k$ -constraint enforcement.

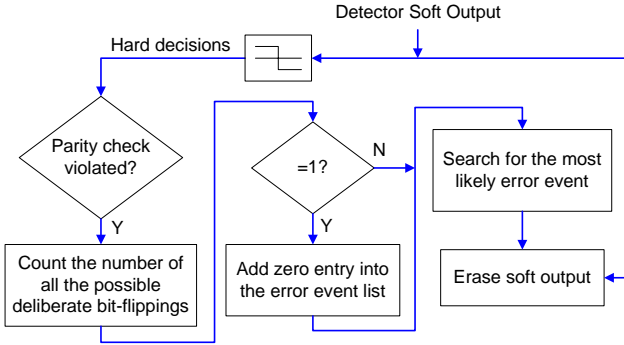


Fig. 3. The overall operation flow of the post-detection processing.

### III. PERFORMANCE EVALUATION

We carried out simulations to evaluate the performance of the above proposed methods. A length-8136 rate-8/9 regular-(4, 36) QC-LDPC code is used. Its parity check matrix contains a  $4 \times 36$  array of circulant matrices, and each circulant matrix has a column weight of 1. Each circulant matrix is randomly constructed subject to the constraint that the overall parity check matrix is 4-cycle free. The read channel equalization target is set as  $4 + 3D - 2D^2 - 3D^3 - 2D^4$ , and the channel is modelled as this ideal equalized channel concatenated with additive white Gaussian noise (AWGN). Our computer simulations show that the error events with 1-bit and 3-bit errors account for over 60% among all the error events. Hence, we simply use the 36-bit single parity check in the LDPC code for dominant error events detection. During the simulation, there is no iterations between the detector and LDPC code decoder, and LDPC code decoder performs up to 20 internal decoding iterations. Fig. 4 shows the simulation results if we only consider the dominant error events detection. For the purpose of comparison, we also show the simulation performance when no post-detection processing is being used. A gain of 0.1dB at the LDPC code decoder output bit error rate (BER) of  $10^{-6}$  is observed.

Fig. 5 shows the simulation results if we further take into account of the  $k$ -constraint enforcement. In this context, we consider the scenarios with  $k=8$  and  $k=9$ . For the purpose of comparison, we also carried out simulations when deliberate bit-flipping is used to enforce  $k$ -constraint without using parity check for error detection. As shown in Fig. 5, more than 0.2dB gain can be achieved at LDPC code decoder output BER of  $10^{-5}$  for  $k=9$ , and the gain increases to over 0.4dB by reducing  $k$  from 9 to 8. This is intuitively justifiable since the performance can greatly degrade as  $k$  reduces if we use deliberate bit-flipping for  $k$ -constraint enforcement without any compensation, while such performance degradation may reduce once we utilize the error event detection capability inherent in LDPC codes. The above simulation results show

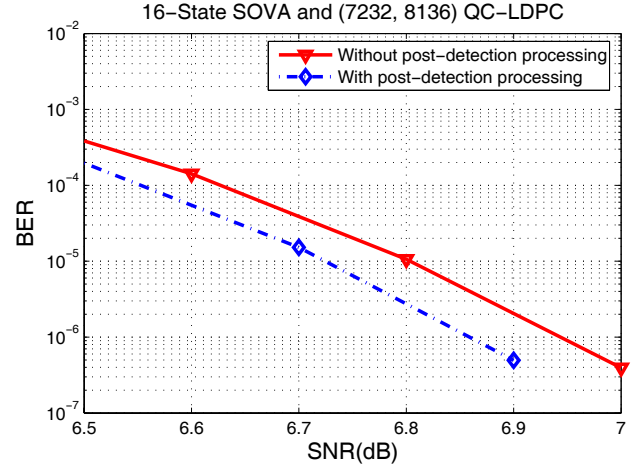


Fig. 4. Performance comparisons of SOVA-LDPC read channel with and without post-detection processing (without considering  $k$ -constraint enforcement).

that the proposed methods may effectively realize dominant error event detection and support the use of deliberate bit-flipping for  $k$ -constraint enforcement at no code rate penalty.

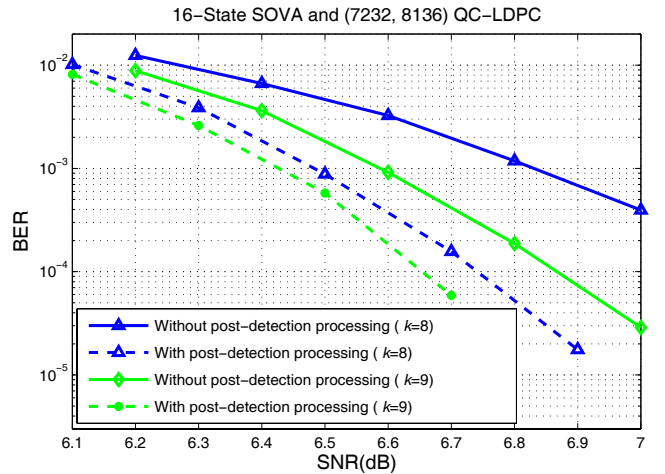


Fig. 5. Performance comparisons of SOVA-LDPC read channel with  $k$ -constraint enforcement.

### IV. CONCLUSION

This paper showed the feasibility and potential of using the simple and explicit parity checks inherent in LDPC codes to realize dominant error events detection at no cost of code rate. Moreover, we pointed out that such zero-redundancy dominant error events detection scheme can be readily used to reduce the performance degradation incurred by deliberate bit-flipping for  $k$ -constraint enforcement. Using a test vehicle of a magnetic

recording channel with the equalization target of  $4 + 3D - 2D^2 - 3D^3 - 2D^4$  and a length-8136 rate-8/9 regular-(4, 36) QC-LDPC code, we carried out simulations to demonstrate the promising potential of the proposed methods.

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