Hybrid Resistor/FET-Logic Demultiplexer Architecture Design for Hybrid CMOS/Nanodevice Circuits

Shu Li and Tong Zhang
Department of Electrical, Computer and Systems Engineering
Rensselaer Polytechnic Institute

Abstract

Hybrid nanoelectronics are emerging as one viable option to sustain the Moore's Law after the CMOS scaling limit is reached. One main design challenge in hybrid nanoelectronics is the interface (named as demux) between the highly dense nanowires in nanodevice crossbars and relatively coarse microwires in CMOS domain. The prior work on demux design use a single type of devices to realize the demultiplexing function, but hardly provides a satisfactory solution. This work proposes to combine resistor with FET to implement the demux, leading to the so-called hybrid resistor/FET-logic demux. Such hybrid demux architecture can make these two types of devices well complement each other to improve the overall demux design effectiveness. Furthermore, the effects of resistor conductance variability are analyzed and evaluated based on computer simulations.

1 Introduction

The past few years have experienced spectacular advances in the fabrication and manipulation of new nanoscale switching devices. Although these new devices show significant future promise, there is a growing consensus [6] that they cannot completely replace CMOS technology. As a result, there is a substantial demand to explore the opportunities for nanoscale CMOS and emerging non-silicon devices to enhance and complement each other to sustain the Moore's Law beyond the CMOS scaling limits. This leads to the paradigm of hybrid CMOS/nano-device circuits [7, 9, 10]. where an array of nanoscale wire ("nanowire") crossbars, with nanowires connected by simple nanodevices at each crosspoint, sits on the top of a CMOS circuit.

One of the main design issues in hybrid nanoelectronic circuits is the interface between highly dense nanowires within nanodevice crossbars and photolithographically defined features of the CMOS subsystem ("microwires"). Several possible solutions have been proposed to tackle this challenge, which may be categorized based on whether the microwire-to-nanowire accessibility is realized through direct mircowire-nanowire ohmic contact [9,11] or a logic circuit called microwire-to-nanowire demultiplexer (demux) [12–16]. All the proposed demux design solutions have a crossbar structure consisting of one layer of parallel nanowires and one layer of parallel microwires. A demux takes the voltages of all the microwires as input to drive the voltage of only one nanowire (called selected nanowire) to a pre-specified value. Meanwhile, in order to ensure good operation reliability, the demux should keep the voltages of all the unselected nanowires well constrained in a safety window far away from that of the selected nanowire or keep all the unselected nanowires floating.

In prior work on demux design, the demultiplexing function is realized by implementing a single type of devices such as resistor [16], diode [12], or field effect transistor (FET) [13–15] at a subset of the microwire-nanowire crosspoints. Because the nonlinear nature of diode's and FET's electrical characteristics can well match the nonlinear nature of the desired demultiplexing function, diode-logic and FET-logic demuxes can, in principle, very well approximate the ideal demultiplexing behavior. However, as pointed out in [16, 17], diode-logic and FET-logic demuxes suffer from significant difficulties of reliable fabrication using current technology. Moreover, FET-logic demuxes tend to suffer from low operational speed because of the serial chains of FETs along the signal path. In contrast, these issues may be much less serious in case of resistor-logic demux. Nevertheless, due to the linear nature of resistor's electrical characteristics, resistor-logic demux inherently cannot well approximate the desired nonlinear demultiplexing behavior. Recent work [16, 17] has applied constant weight codes, a topic in classical coding theory to design resistor-logic demux structure with optimal operation margin, which may relatively better approximate the demultiplexing behavior.

This work proposes a hybrid resistor/FET-logic demux design solution that can much better approach the desired demultiplexing behavior compared with conventional resistor-logic demux, while maintaining the inherent advan-

tages of resistor-logic demux in terms of manufacturability and operational speed. The basic idea is to use a single column of p-type FETs (pFETs) to convert the linear voltage output of a resistor-logic demux core to be nonlinear so that the desired demultiplexing function can be much better approximated. The resistor-logic demux core design can still be optimized using constant weight codes, whereas the optimization constraint on the constant weight code construction is largely relaxed, which will tend to result in a more area efficient demux. Meanwhile, since only one pFET is implemented along each nanowire, the speed degradation can be much less compared with that of an FET-logic demux. Finally, since the resistor-logic demux core no longer directly drives the nanowires within the nanodevice crossbar, the overall system energy consumption will be accordingly reduced.

2 Background

Kuekes et al. [16] presented the architecture of the resistor-logic demux, which provided the feasibility to fabricate the specific resistances at the crosspoint of nanowire and microwire. A resistor-logic demux typically has a microwire-nanowire crossbar structure with identical resistors implemented at certain microwire-nanowire crosspoints. Let N_{micro} and N_{nano} denote the number of microwires and nanowires within the resistor-logic demux crossbar, respectively. All the resistors at the crosspoints form N_{nano} distinct resistor-based linear voltage dividers that share the same N_{micro} input voltages, and each voltage divider drives one individual nanowire. If we use '1' and '0' to represent the presence and absence of a resistor at each crosspoint, each nanowire (and hence each voltage divider) can be represented by an N_{micro}-bit *nanowire characteristic vector*. Accordingly, the entire demux can be represented by an $N_{nano} \times N_{micro}$ *demux characteristic matrix* in which each row is one nanowire characteristic vector.

A demux should drive the voltage of one nanowire to a pre-specified value and keep the voltages of all other nanowires well constrained in a safety window far away from that of the selected nanowire or keep all the unselected nanowires floating. Let V_{sel} denote the desired output voltage of the selected nanowire. We assume that the input voltage on each microwire can be either V_{sel} or V_0, and define an N_{micro}-bit *input vector* in which '1' and '0' represent that the voltage of the corresponding microwire to be V_{sel} and V_0, respectively. Hence, we simply set the input vector of the microwires equal to the characteristic vector of the nanowire to be selected. Given one binary vector $\mathbf{s}$, let $wt(\mathbf{s})$ denote its Hamming weight. Given the input vector $\mathbf{h}$, the output voltage of the nanowire with the characteristic vector $\mathbf{v}$ is

$$\frac{wt(\mathbf{h} \text{ AND } \mathbf{v})}{wt(\mathbf{v})} \cdot (V_{sel} - V_0) + V_0. \quad (1)$$

Let V^m_{wire} denote the minimum value of the voltage differences between one selected nanowire and any unselected nanowires. In general, the objective of resistor-logic demux design is to maximize $V^m_{wire}/(V_{sel} - V_0)$ in order to improve the operational reliability. However, in the context of crossbar nanoelectronic circuits that are of most practical interest, the objective of resistor-logic demux design is beyond mere maximization of $V^m_{wire}/(V_{sel} - V_0)$. For crossbar nanoelectronic circuits, a pair of demuxes is used to drive both the rows and columns of nanowires. The crosspoint of the selected row nanowire and the selected column nanowire lies the selected nanodevice under operation. The magnitude of the voltage drop across the selected nanodevice under operation, denoted as ΔV_{sel}, typically should be greater than that of any other unselected nanodevices. Let $\Delta \mathcal{V}_{unsel}$ denote the set of the magnitudes of voltage drops across any unselected nanodevices. In this context, the main objective is to maximize v_m that is defined as

$$v_m = 1 - \frac{\max(\Delta \mathcal{V}_{unsel})}{\Delta V_{sel}}. \quad (2)$$

We note that v_m represents the normalized margin of the voltages across the selected and unselected nanodevices. Mere maximization of $V^m_{wire}/(V_{sel} - V_0)$ for the individual row or column resistor-logic demux does not necessarily maximize v_m. Since how to design the demux to only maximize V^m_{wire}/V_{sel} is already nontrivial, the design of optimum row and column demuxes for nanodevice crossbar certainly becomes more challenging.

It has been well demonstrated [16, 17] that constant weight codes, a topic in classical coding theory, can be readily leveraged to tackle this challenge. A constant weight code is denoted as (n, M, d_{min}, d_{max}, w), where n is the length of each codeword, M is the number of codewords, d_{min} and d_{max} are the minimum and maximum Hamming distance between any two codewords, and w is the weight of the codewords. To design a resistor-logic demux with N_{micro} microwires and N_{nano} nanowires, we construct a constant weight code (N_{micro}, N_{nano}, d_{min}, d_{max}, w) and assign each N_{micro}-bit codeword as one nanowire characteristic vector. For any two codewords $\mathbf{s}$ and $\mathbf{t}$, we have $wt(\mathbf{s} \text{ AND } \mathbf{t}) = w - dist(\mathbf{s}, \mathbf{t})/2$, where $dist(\mathbf{s}, \mathbf{t})$ denotes the Hamming distance between $\mathbf{s}$ and $\mathbf{t}$. Therefore, (1) can be rewritten as

$$\frac{w - dist(\mathbf{h}, \mathbf{v})/2}{w} \cdot (V_{sel} - V_0) + V_0. \quad (3)$$

With the assumption that the row and column demuxes are identical, it has been proved in [16] that the normalized voltage margin v_m defined in (2) is equal to $2d_{min}/(2d_{max} +$

d_{min}). Therefore, in order to maximize v_m, we should maximize d_{min}/d_{max}. Meanwhile, it is clear from (3) that the maximization of $V^m_{wire}/(V_{sel} - V_0)$ for each demux only requires to maximize d_{min}. Furthermore, it is desirable for the row and column demuxes to use as less number of microwires as possible in order to reduce the area overhead. Therefore, for nanodevice crossbar circuits with N_{nano} nanowires along each direction, the essential demux design challenge is how to construct a constant weight code (N_{micro}, N_{nano}, d_{min}, d_{max}, w) that has a minimum value of N_{micro} and maximum value of d_{min}/d_{max}. Finally, it should be pointed out that the resistor-logic demux output voltage analysis in [16] assumes the impact of the load resistance from the nanodevice crossbar to be negligible. If such impact is not negligible, voltage margin results presented above will be subject to certain degradation.

3 Hybrid Resistor/FET-Logic Demux

This work presents a method to fundamentally improve the design effectiveness of resistor-logic demux. The essential challenge of resistor-logic demux design is due to the conflict between the linear nature of its operation and the desired nonlinear nature of an ideal demux. In this section, we propose to circumvent such linear vs. nolinear conflict by introducing a column of pFETs between the resistor-logic demux and the nanodevice crossbar, as illustrated in Fig. 1. DeHon et al. [8] described the technique to fabricate FETs by controlling the doping profile along the axial dimension of the nanowires. Therefore, it is feasible to form one pFET along each nanowire through appropriate doping and fabrication of dielectric layer, and the feasibility has also been experimentally demonstrated in [13] that reports a design of FET-logic demux. The resulted overall demux is referred to as hybrid resistor/FET-logic demux.

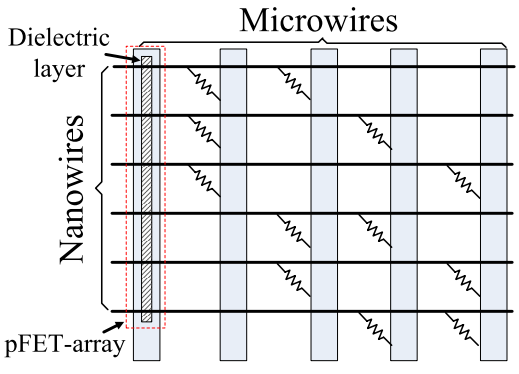

Figure 1. Hybrid resistor/FET-logic demux.

The column of pFETs converts the linear output voltage of the resistor-logic demux core into nonlinear output voltage that can well match the expected nonlinear behavior of an ideal demux. According to (1), within the resistor-logic core, the selected nanowire has a voltage of V_{sel} and the voltages of all the other nanowires fall into the range $[\frac{w-d_{max}/2}{w} \cdot (V_{sel} - V_0) + V_0, \frac{w-d_{min}/2}{w} \cdot (V_{sel} - V_0) + V_0]$. Therefore, the minimal voltage difference between the selected nanowire and any other unselected nanowire, which is denoted as V^m_{wire}, equals to $\frac{d_{min}}{2w}(V_{sel} - V_0)$. Moreover, all the pFETs share the same gate voltage denoted as V_g and we assume that all the pFETs possess identical threshold voltage V_{tp}. Clearly, in order to only turn on the pFET associated with the selected nanowire, the gate voltage V_g and the threshold voltage V_{tp} of the pFETs (notice that $V_{tp} < 0$) must satisfy

$$\begin{cases} V_g - V_{sel} & < & V_{tp} \\ V_g - (V_{sel} - V^m_{wire}) & > & V_{tp} \end{cases} \quad (4)$$

To balance the operational margin, we set $V_g - V_{tp} = V_{sel} - V^m_{wire}/2$. This hybrid resistor/FET-logic demux has the same function as the pure FET-based demux solutions proposed in [13–15]. Due to the regularity of the pFETs array, it is reasonable to expect that the fabrication of pFET can be relatively easy. The desired voltage drops across the selected nanodevice can be easily realized by applying the appropriate gate voltages and input microwire voltages to both row and column demuxes. It is clear that, in order to improve the demux operational reliability, we increase the value of d_{min} of the constant weight codes, which can be more efficient (in terms of the required microwire numbers) compared with increasing d_{min}/d_{max}.

Compared with the conventional resistor-logic demux design, this proposed hybrid resistor/FET-logic demux design has the following main advantages, including (i) Only the selected nanowire will be driven to the desired voltage while all the other unselected nanowires will keep floating. This obviates the concern of the operational voltage margin for the nanodevice operation within the nandevice crossbar. (ii) The demux design objective becomes the maximization of d_{min} instead of d_{min}/d_{max}, which will facilitate the construction of constant weight codes and reduce the number of required microwires. (iii) The nanodevice crossbar can be much less sensitive to the operational variability of the resistor-logic core incurred by environmental and process variations. (iv) The power consumption may be reduced since only one voltage divider needs to drive the load from the nanodevice crossbar. Finally, although with equivalent logic function as previously proposed FET-based demux design solutions, this proposed hybrid resistor/FET-logic demux maintains the inherent advantages of resistor-logic demux in terms of manufacturability and speed. The proposed demux demonstrates the potentials to be adopted in high-density memory design, where the floating nanowires will be set to certain voltages.

4 Effects of Process Variations

The above discussion assumes that all the resistors have the same resistance. However, such an ideal assumption is not valid in practice. This section investigates their effects on the reliability of the proposed hybrid demux design. The demux reliability is measured using a metric *functioning probability* P_{demux} defined as

$$P_{demux} = \prod_{i=1}^{N_{nano}} P_{nano}^{(i)}, \tag{5}$$

where N_{nano} is the total number of nanowires, and $P_{nano}^{(i)}$ is the nanowire functioning probability that the i-th nanowire can be *correctly* selected. To simulate the randomness in nanoscale fabrication, we assume resistor conductances are independent identical normal random variables. In this way, both random defects and parametric variations could be modelled through values from Guassian distribution. As pointed in [18], it is preferable to use *conductance* rather than *resistance* in modelling the resistor variations. The main reason is, for the fabrication of resistors, a short defect is much more disruptive than an open defect, hence the fabrication process should ensure the probability of short defects is extremely low at the cost of higher probability of open defects. This may lead to a highly asymmetric distribution of the resistance, which may result in a more symmetric distribution of the conductance.

Each resistor-based voltage divider in the hybrid demux determines the source voltage of the associated pFET, and at this point, all pFETs have the same threshold voltage V_{tp}. Let $V_{gs}^{(i)}$ denote the voltage difference between gate and source of the pFET along the i-th nanowire, and we define the voltage gap $V_{gap}^{(i)} = V_{gs}^{(i)} - V_{tp}$. Clearly, the i-th nanowire is selected or unselected when $V_{gap}^{(i)}$ is negative or positive. Due to the randomness of all the conductances , the voltage gap of each nanowire is a random variable (we will show later that it may further be approximated as a normal random variable). For one nanowire with the characteristic vector of $\mathbf{v}^{(i)}$, its functioning probability $P_{nano}^{(i)}$ depends on the statistical characteristics of voltage gaps of all the nanowires when the input vector equals to $\mathbf{v}^{(i)}$. Let $P(V_{gap}^{(i)} < 0)$ and $P(V_{gap}^{(i)} > 0)$ represent the probabilities that $V_{gap}^{(i)}$ is negative and positive, we have

$$P_{nano}^{(i)} = P(V_{gap}^{(i)} < 0) \cdot \prod_{j \neq i} P(V_{gap}^{(j)} > 0). \tag{6}$$

Let d denote the Hamming distance between the input vector and the characteristic vector of one nanowire, V_{sel} and V_0 are the two voltages on the microwires corresponding to 1 and 0 in the input vector, and c_j is the conductance of each resistor. Therefore, by denoting the gate voltage of pFET as V_g, the corresponding voltage gap can be written as

$$V_{gap} = V_g - \frac{\Sigma_{j=1}^{d/2} c_j \cdot V_0 + \Sigma_{j=d/2+1}^{w} c_j \cdot V_{sel}}{\Sigma_{j=1}^{w} c_j} - V_{tp}. \tag{7}$$

As assumed formerly, the conductances of resistors are independent identical normal random variables, thus, the voltage gap V_{gap} of the nanowires possessing the same Hamming distance with the input voltage vector will obtain the equal probability density function. However, because it involves the ratio between normal random variables, as shown in (7), it can be very difficult, if not impossible, to obtain a concise closed form expression of the probability density function of V_{gap}. We argue that the probability density function of V_{gap} can be approximated as a normal distribution based on our extensive numerical simulations which is illustrated in the following example.

Example 4.1 *Given one nanowire with the characteristic vector* $\mathbf{v}$ *of* $[1,1,1,1,1,0,0,0,0,0]$ *and the input vector* $\mathbf{h}$ *is* $[1,1,0,0,1,1,1,0,0,0]$*, Hamming distance* $d = 4$*. We carried out simulations to capture the distribution of voltage gap with the following setup. We normalize the distribution of resistor conductance as* $\mathcal{N}(1, \sigma_c)$*. Since the conductance cannot be negative, the distribution is truncated into the range* $[0, \infty)$*. We normalize* V_{sel} *and* V_0 *as 1 and 0, and set the pFET threshold voltage* V_{tp} *as -0.1. The gate voltage of the pFET is set as* $V_g = V_{sel} - V_{wire}^m/2 + V_{tp}$*, where* $V_{wire}^m = \frac{d_{min}}{2w}(V_{sel} - V_0)$ *is the minimal voltage difference between the selected nanowire and other unselected nanowires. By increasing* σ_c *from 0.06 to 0.16 with the step of 0.02, we randomly generate* 10^6 *sets of conductance values and calculate the corresponding* 10^6 *samples of* V_{gap} *for each* σ_c*. Fig. 2 shows the histogram of the voltage gap when* $\sigma_c = 0.1$*, which turns out to be close to a normal distribution. Based on these* 10^6 *samples, we further calculated the mean* μ_{gap} *and standard deviation* σ_{gap}*. The red curve in Fig. 2 corresponds to the probability density function of* $\mathcal{N}(\mu_{gap}, \sigma_{gap})$*. The same conclusion can be drawn from the simulation results with the other* σ_c *setups. Therefore, we expect that voltage gap* V_{gap} *generally can be approximated to be random variable with normal distribution.*

As the voltage gap distribution depends on the Hamming distance between the input vector and the characteristic vector of this nanowire. For the i-th nanowire with characteristic vector $\mathbf{v}^{(i)}$, we define a nanowire Hamming distance profile $\{(d_1, n_1), (d_2, n_2), \cdots, (d_{s_i}, n_{s_i})\}$ that means there are n_j nanowires whose characteristic vectors have the same Hamming distance d_j with $\mathbf{v}^{(i)}$. Correspondingly, we have s_i different voltage gap normal distributions $\mathcal{N}(\mu_{gap}^j, \sigma_{gap}^j)$ for $1 \leq j \leq s_i$. After obtaining P_{nano}^i, we may use (5) to calculate P_{demux}. Up to

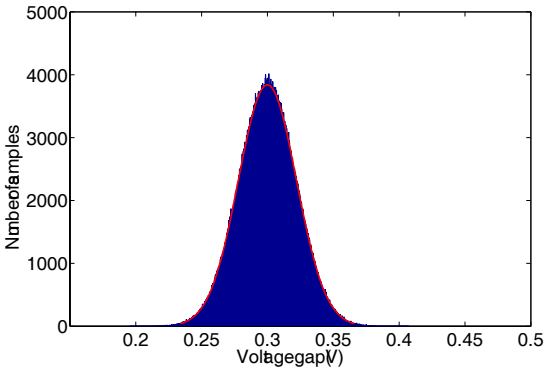

Figure 2. Histogram of voltage gap.

now, we may summarize the procedure to calculate the demux functioning probability P_{demux} as follows, and define a function $Q(x)$ as $Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty e^{\frac{-y^2}{2}} dy$. We

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Procedure `Calculation of Demux Functioning Probability` P_{demux}

Input: Constant weight code parameters, resistor conductance distribution $\mathcal{N}(\mu_c, \sigma_c)$, and the values of V_{sel}, V_0, V_g, and V_{tp}.
for *i=1 to* N_{nano} **do**
  Identify the nanowire Hamming distance profile $\{(d_1, n_1), (d_2, n_2), \cdots, (d_{s_i}, n_{s_i})\}$.
  for *j=1 to* s_i **do**
    Obtain the mean μ_{gap}^j and standard deviation σ_{gap}^j through computer simulations.
  end
  Calculate the nanowire functioning probability $P_{nano}^{(i)} = \prod_{j=0}^{s_i} \left(Q(-\mu_{gap}^j/\sigma_{gap}^j)\right)^{n_j}$.
end
Calculate the demux functioning probability $P_{demux} = \prod_{i=1}^{N_{nano}} P_{nano}^{(i)}$.

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use a constant weight code (10, 252, 2, 10, 5) so that all the nanowires have the same Hamming distance profile $\{(2, 25), (4, 100), (6, 100), (8, 25), (10, 1)\}$. Because $(Q(-\mu_{gap}^0/\sigma_{gap}^0))$ for the selected nanowire is 1 at this point, we only need to obtain the five pairs of $(\mu_{gap}^j, \sigma_{gap}^j)$. The resistor conductance distribution is $\mathcal{N}(1, \sigma_c)$ and we use 0.06, 0.08, 0.10, 0.12, 0.14, and 0.16 as σ_c. For each σ_c, we carried out 10^5 simulation runs to obtain μ_{gap}^j and σ_{gap}^j. We set V_{sel}, V_0, V_{tp} as 1, 0, and -0.1. The mean of voltage gap is directly calculated from (7), where c_js are the mean value of the conductance (i.e., 1). Hence, $\mu_{gap}^1 = 0.1$, $\mu_{gap}^2 = 0.3$, $\mu_{gap}^3 = 0.5$, $\mu_{gap}^4 = 0.7$, and $\mu_{gap}^5 = 0.9$. The values of σ_{gap}^j are obtained through computer simulations for different d and σ_c. The results are illustrated in Fig. 3.

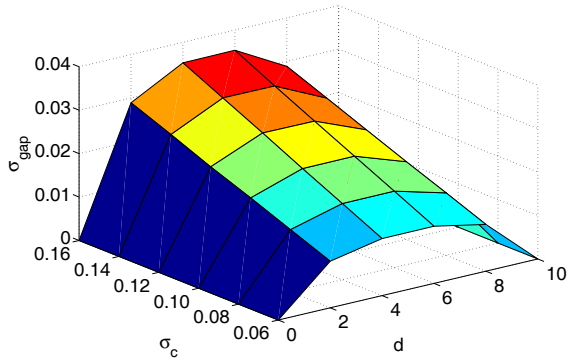

Figure 3. Effect of d and σ_c on σ_{gap}.

The next step is to calculate $Q(-\mu_{gap}^j/\sigma_{gap}^j)$, then determine $P_{nano}^{(i)}$, which are listed in Table 1. For verification, at each σ_c we carried out 10^5 simulation runs to directly obtain the estimations of $P(V_{gap}^{(i)} < 0)$ and then calculate the nanowire functioning probability which are denoted as $\tilde{P}_{nano}^{(i)}$ in Table 1. Furthermore, With $P_{nano}^{(i)}$, we calculate the overall demux functioning probability P_{demux} based on (5). Since all nanowires have the same function probability and the demux contains 252 nanowires, $P_{demux} = (P_{nano}^{(i)})^{252}$ are also listed in Table 1.

5 Conclusions

This paper presents a demux design solution to tackle the inter-domain interconnect challenge in the emerging hybrid CMOS/nano-device electronic systems. The key of this proposed demux design is to complement a resistor-logic demux with a single column of pFET switches. Such a hybrid demux structure can well approximate the nonlinear behavior of an ideal demux while maintaining the advantages of resistor-logic demux in terms of the manufacturability and speed. Furthermore, we studied the effects of resistor and pFET variability on the demux operational reliability by assuming the electrical characteristics of the same type device have independent identical random normal distribution. We presented simple approaches to estimate the demux operational reliability in presence of such process variations, which are further demonstrated and evaluated through a demux design example.

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Table 1. Effect of conductance variability on $P_{nano}^{(i)}$ and P_{demux}.

σ_c	0.06	0.08	0.10	0.12	0.14	0.16
$Q(-\mu_{gap}^1/\sigma_{gap}^1)$	1	1	$1-1.4\times10^{-8}$	$1-1.6\times10^{-6}$	$1-3.7\times10^{-5}$	$1-2.7\times10^{-4}$
$Q(-\mu_{gap}^2/\sigma_{gap}^2)$	1	1	1	1	1	1
$Q(-\mu_{gap}^3/\sigma_{gap}^3)$	1	1	1	1	1	1
$Q(-\mu_{gap}^4/\sigma_{gap}^4)$	1	1	1	1	1	1
$Q(-\mu_{gap}^5/\sigma_{gap}^5)$	1	1	1	1	1	1
$P_{nano}^{(i)}$	1	1	$1-3.4\times10^{-7}$	$1-3.9\times10^{-5}$	0.9992	0.9934
$\tilde{P}_{nano}^{(i)}$	1	1	1	1	0.9990	0.9918
P_{demux}	1	$1-10^{-8}$	$1-8.5\times10^{-5}$	0.9902	0.7890	0.1885

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