Thermals

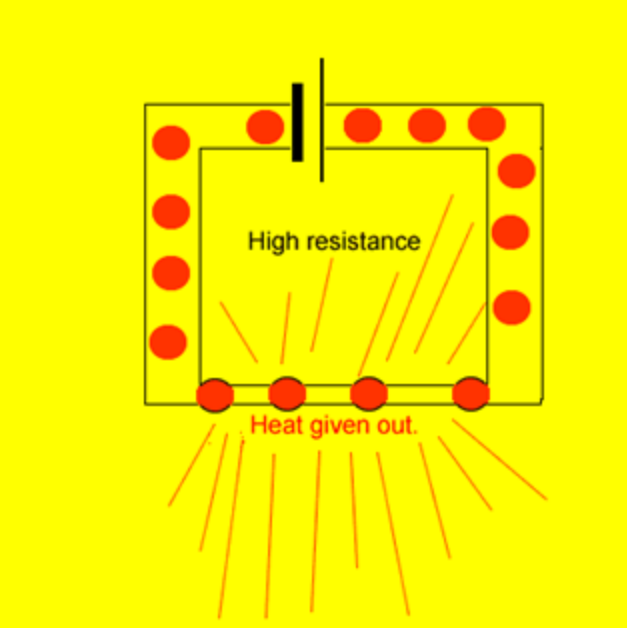
IEEE EPS @ RPI | 09/26/24

What are you going to learn?

1. Thermals Basics
2. Canonical Problems with Thermal Challenges
3. Thermal Simulation and Modeling for Chips

Thermals Basics

Why do transistors produce heat?

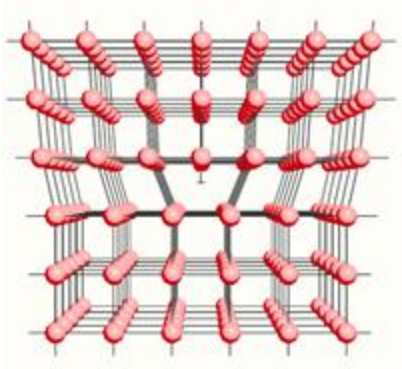


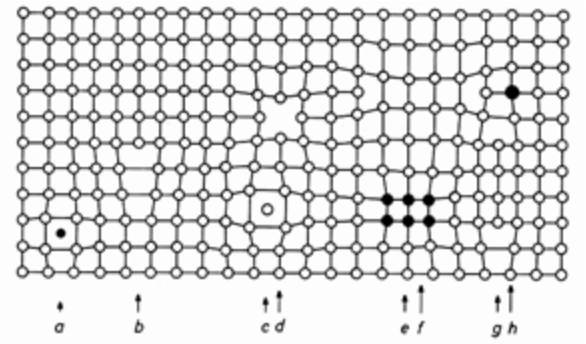
Joule Heating (P = I^2 * R Losses)

Dependent on two things:

1. Resistance
2. Current

Why does resistance produce heat?





Three Reasons:

1. Impurities in periodic crystal lattice
2. Dislocations in periodic crystal lattice
3. Phonons (Fancy word for a particle of heat)

All of these reasons cause **electron scattering.**

This causes a change in the direction of the electron's momentum, transferring some energy into the lattice.

This energy transfer manifests as heat

Currents impact on power dissipation

When there is current, power is being dissipated.

Static: When transistor isn't switching

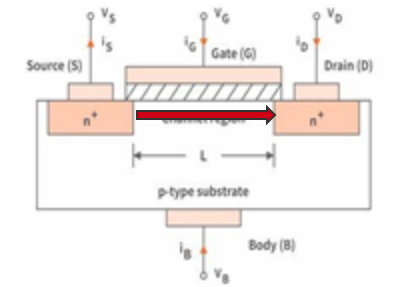
- Leakage Power:
  - Subthreshold Leakage
  - Gate Leakage
  - Junction Leakage

Dynamic: When transistor is switching

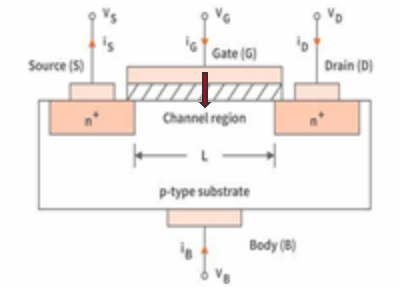
- Switching Power
- Internal Power

Leakage Power

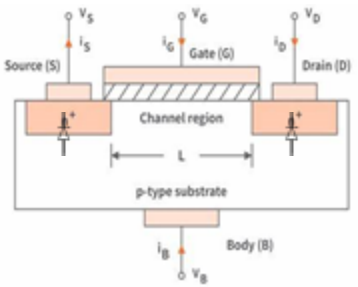
Subthreshold



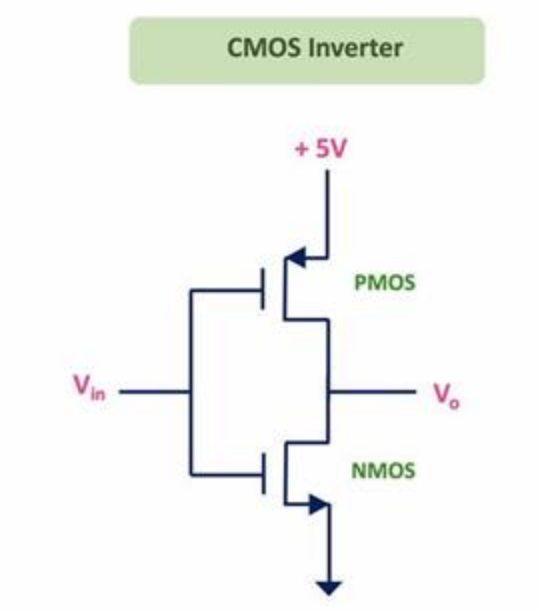
Gate



Junction



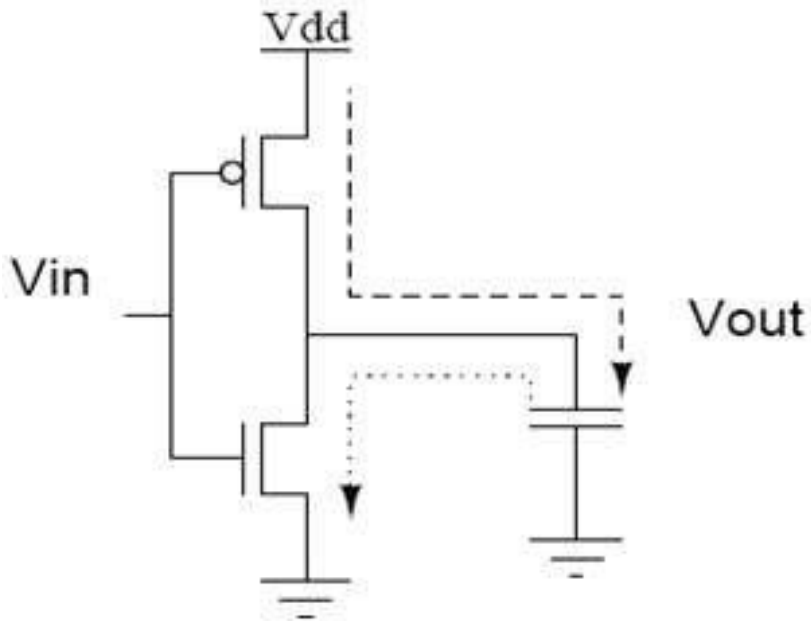
Dynamic - Transient Power Dissipation



There is a moment where both transistors are on, causing a short.

This is wasted energy.

Capacitive-Load Power Consumption



The wires are very close together.

Two pieces of metal separated by an insulator… that sounds familiar.

Canonical Problems with Thermal Challenges

Component Degradation

1. **Electromigration**: Metal atoms move, causing voids and breaks
2. **Dielectric Breakdown**: The dielectric no longer resists current, causing shorts
3. **Thermal Expansion and Mechanical Stress**: Different expansion rates in materials, causes cracking and warping.
4. **Oxidation**: Corrosion of metal components, reducing conductivity

Signal Integrity

1. Resistance increases -> Data Corruption
2. Capacitance Variations -> Signal Propagation Speeds Change
3. Oscillator Temperature Variation -> Clock Jitter

Failure of TIM

TIM (Thermal Interface Material) can fail

1. Pump-Out effect
2. Drying
3. Oxidation

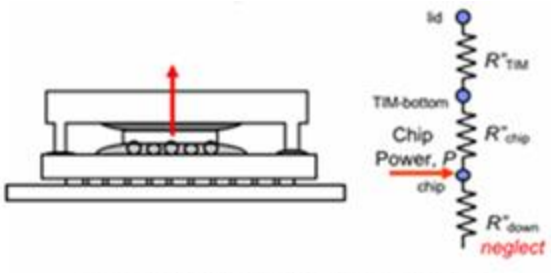


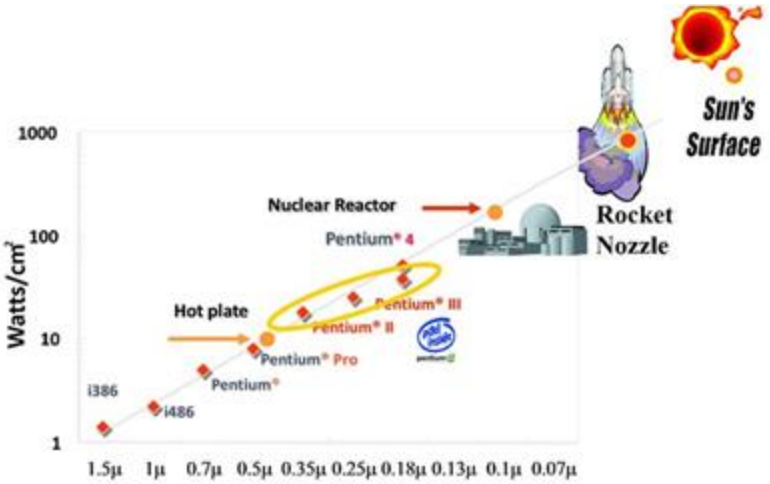
Figure 7. Conduction paths in a high-power 2D package

Heterogeneous Integration Impacts

Typical heat distribution:

1. TIM
2. Lid
3. Heat Sink

It isn't as simple with 3D integration



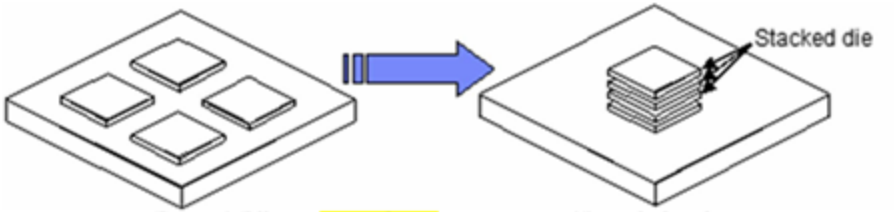
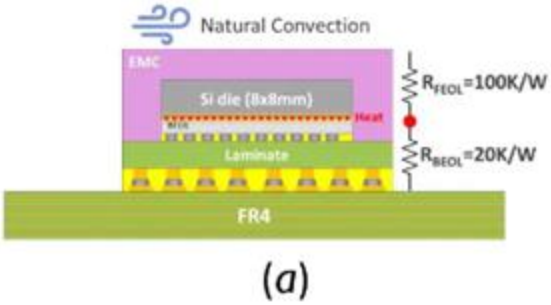


Figure 6. Effective power density increases in a 3D stacked package

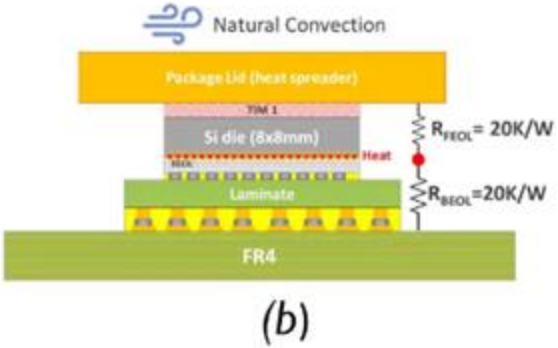
$$P_D = \frac{P}{A}$$

Simulations and Modeling

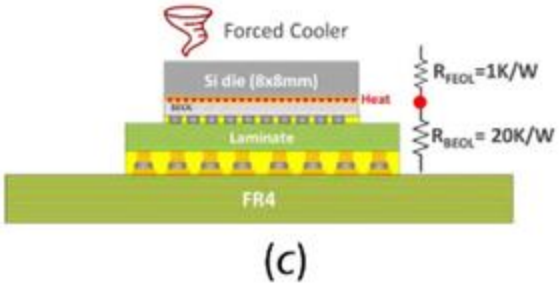
Thermal Modeling



(a)

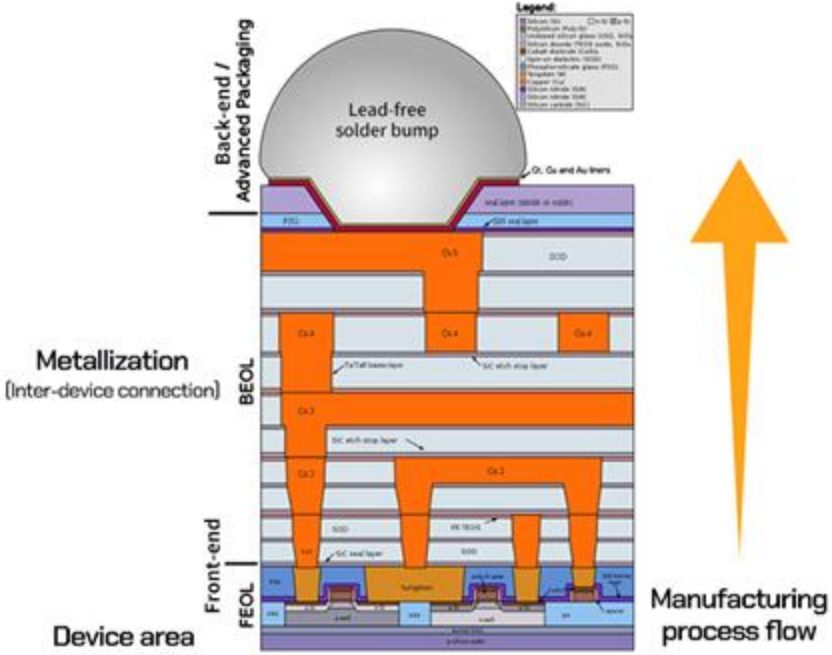


(b)



(c)

Chips as a “Scooby-Doo sandwich”



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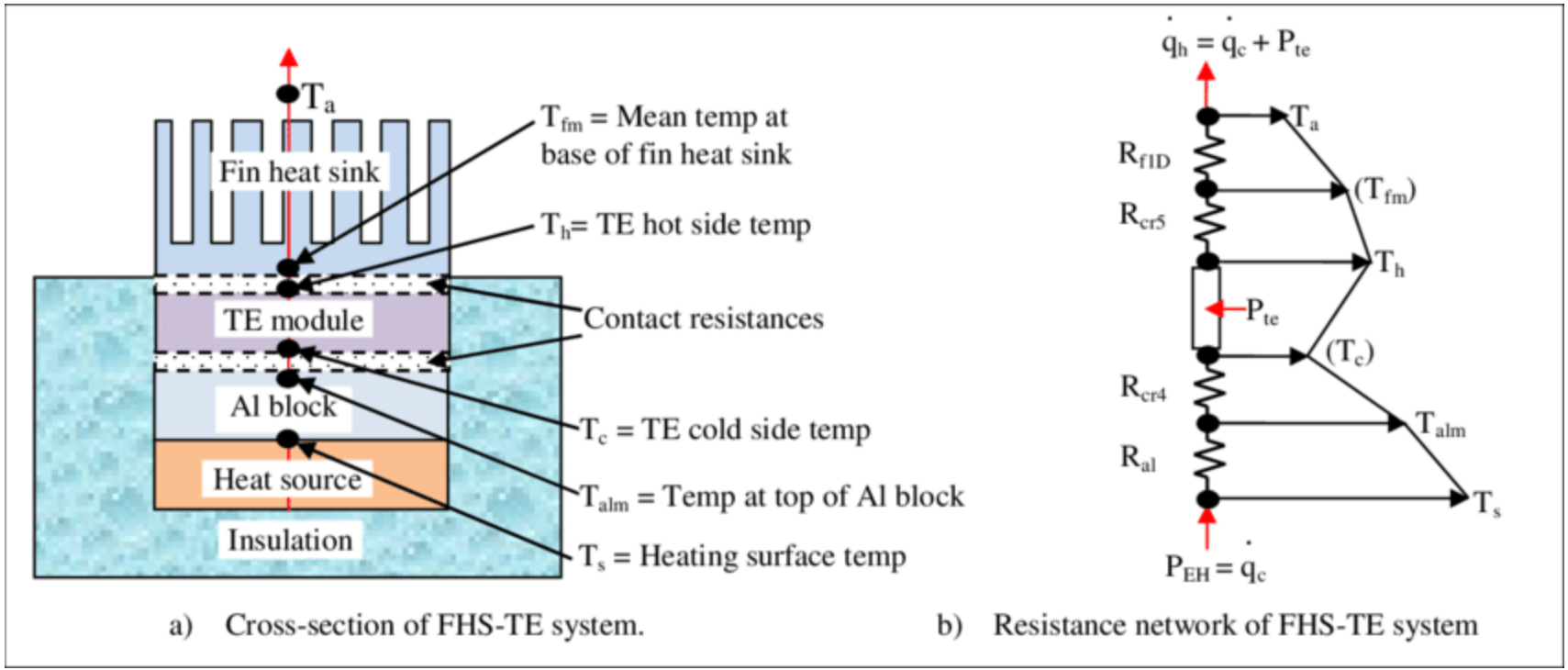
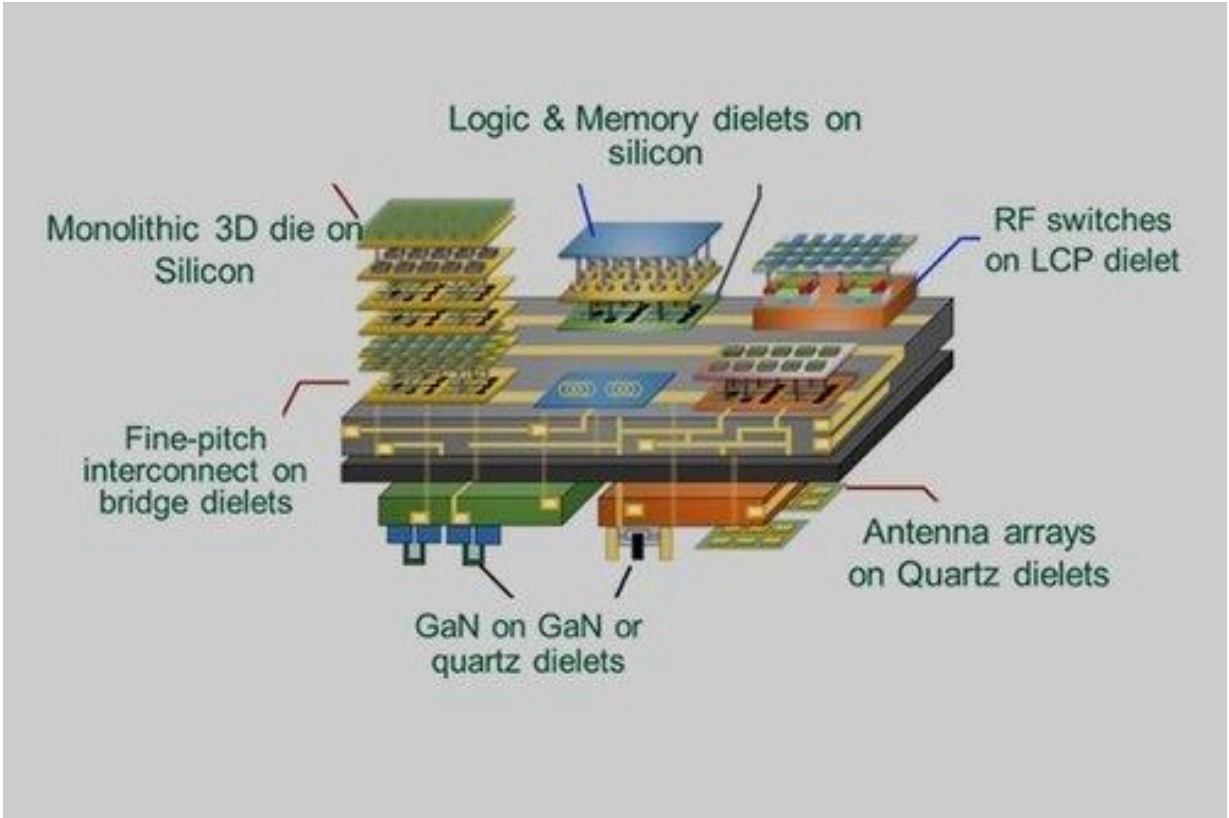


a) Cross-section of FHS-TE system.

b) Resistance network of FHS-TE system

Ok, but a REALLY big, complex sandwich



Increased emphasis on transient performance

More localized hot-spots, with less clear thermal dissipation pathway (3D thermal modeling)

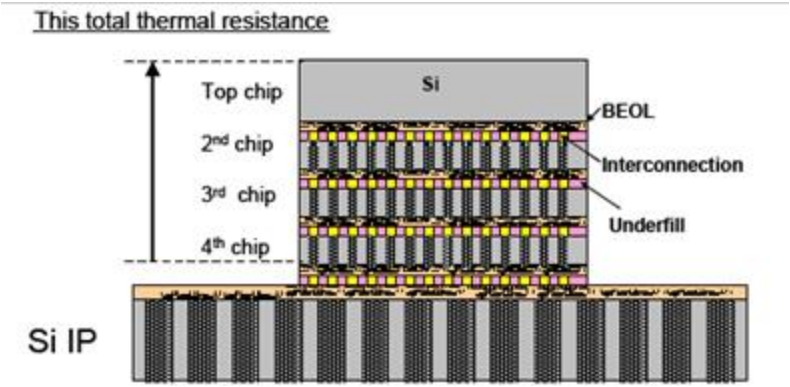


Figure 17: 3D Chip Stack Combined Model [5]

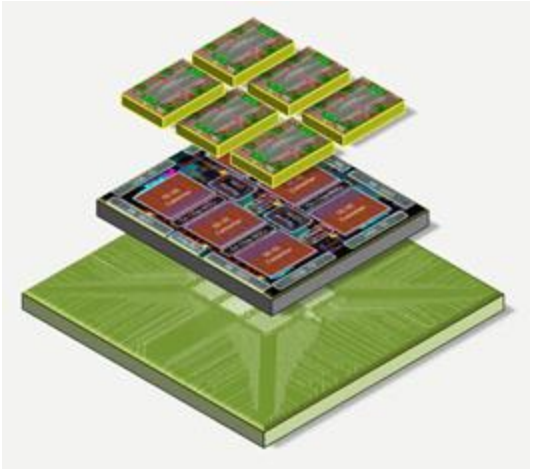


Figure 18: 3D Chip Stack Schematic

Relative importance of various components is modeled below using a DOE from finite element modeling/simulation

Models are extremely complex; In most cases, an experimental “Average” must be determined

TABLE II. MATERIAL PROPERTY SENSITIVITY STUDY FOR BEOL EQUIVALENT THERMAL CONDUCTIVITY AND JOULE HEATING

Parameter	BEOL $k_{equ,z}$ Sensitivity	Joule heating Sensitivity	Reference value
k_low-k	0.50	-0.45	0.3 W/m-K
k_metal	0.17	-0.21	65-230 W/m-K depending on metal CD
k_etch-stop	0.14	-0.21	5 W/m-K
k_barrier	0.07	-0.05	5 W/m-K
ρ_metal		0.97	49-175 Ohm·nm depending on metal CD
ρ_barrier		0.22	1200 Ohm*nm

Table 1: Influential Characteristics for thermal Models [6]

Thin Films exhibit poor thermal performance

10-100x lower heat dissipation than bulk counterparts

-Porosity

-Grain Boundaries

-Impurities

New Technologies may aid in increasing thermal conductivity for next-gen chips

-Carbon nanotubes (6000+ W/m*K)

-Via Interconnects (Eg. 2.5D)

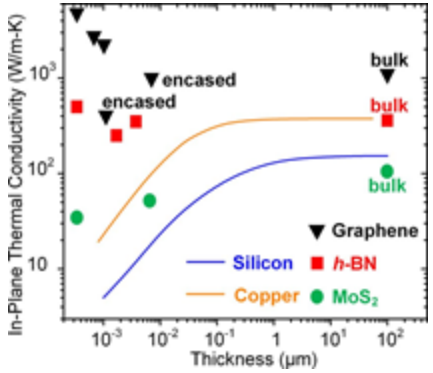


Figure 12: Thin Film Thermal Characteristics [7]

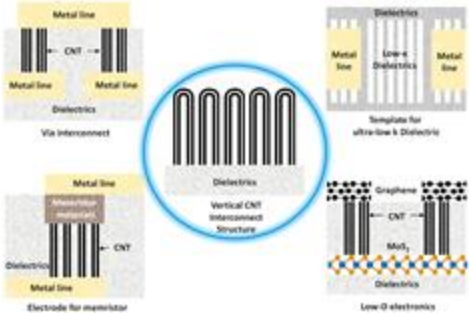
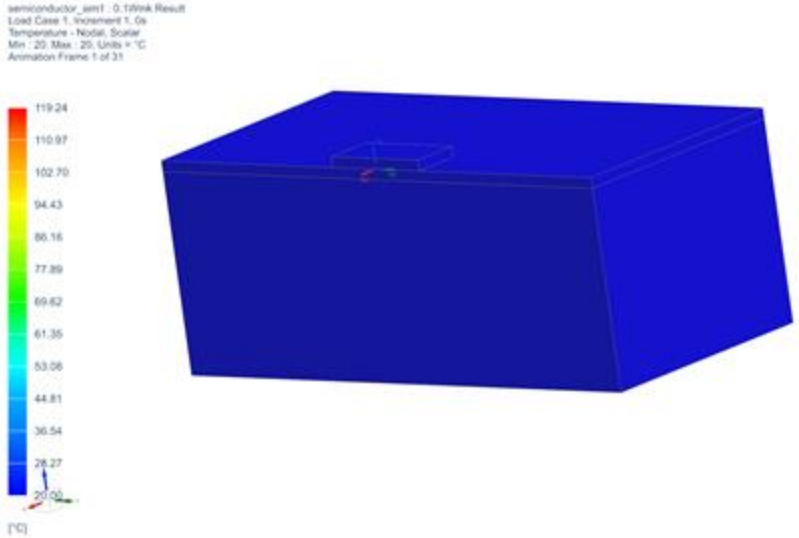


Figure 13: Carbon nanotube Interconnects [1]

Thermal Simulation (NX)



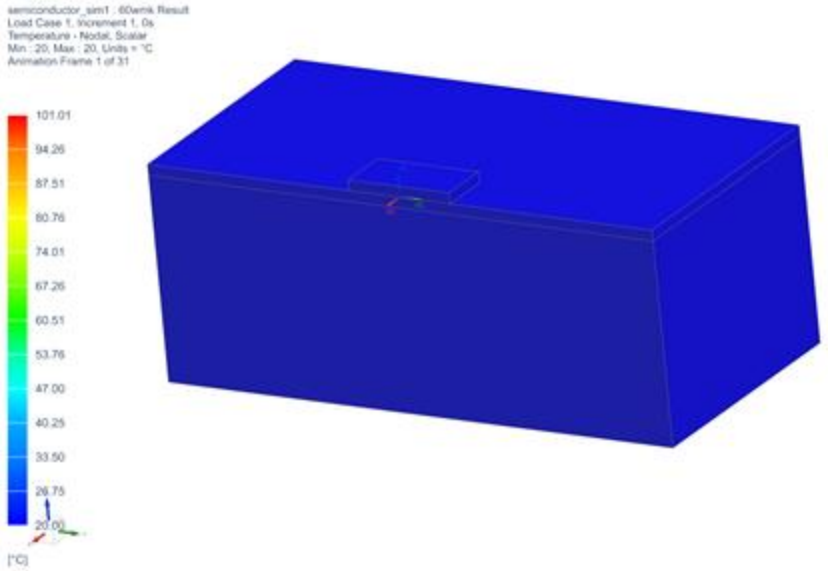


Figure 14, 15: Generated Thermal simulation showcasing effect of ULK thermal characteristics

Thermal modeling techniques differ significantly depending on boundary conditions

-Strong dependence on density and distribution of interconnects

-Relative “anisotropy” within interconnects has major implications on heat rejection & Hot spots

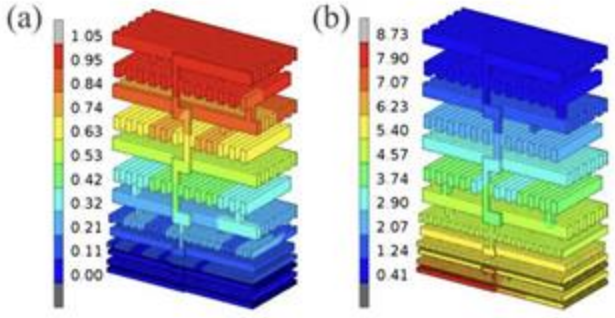


Figure 16: BEOL Structure simulation using:
a)External Heat Flux b)Joule Heating

-Accurately model Hot spots

-Accurately model transient performance

-High Computational Efficiency (Design iteration on day to day scale)

Metric?	Macro-Scale Modeling	Micro (or Nano) scale Modeling	Heterogeneous Modeling
Hot Spot Measurement	Poor	Great	Good
Transient Measurement	Poor	Great	Good
Computational Efficiency	Great (Hours)	Poor (Weeks)	Moderate (Days)
Implementation Difficulty	Easy	Moderate	Difficult

Table 2: Modeling Methodologies

Voltage = Temperature? (Thermistors, TCR)

$$R = R_{ref}\,[1 + \alpha(T - T_{ref})]$$

Where,

R = Conductor resistance at temperature "T"

R_{ref} = Conductor resistance at reference temperature T_{ref}, usually 20°C, but sometimes 0°C.

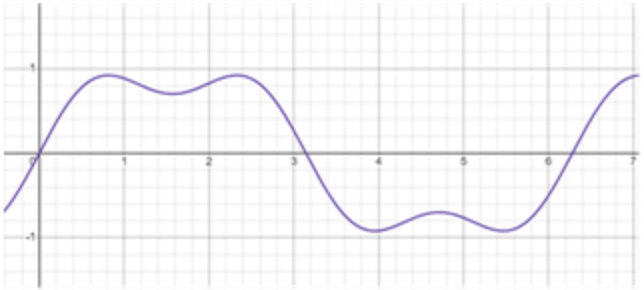
α = Temperature coefficient of resistance for conductor material.

T = Conductor temperature in degrees Celcius.

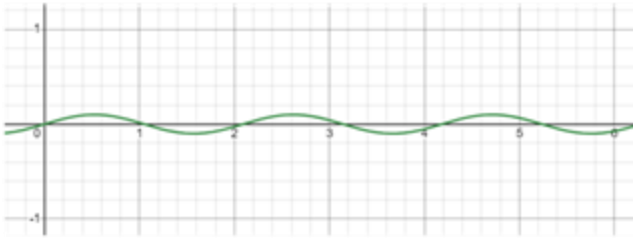
T_{ref} = Reference temperature that α is specified at for the conductor material

Measurement Techniques- 3 Omega (3w)

Input Signal Gen.



Measured Wave



3w

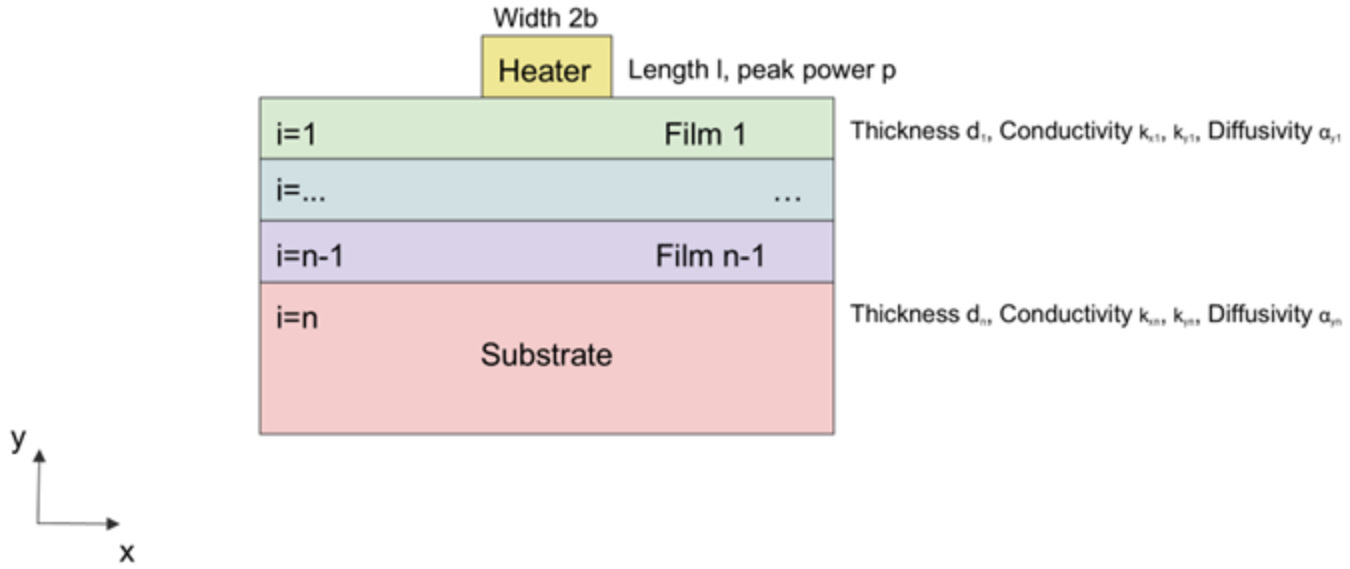
Contribution

1st Harmonic: Input Signal (AC current & power)

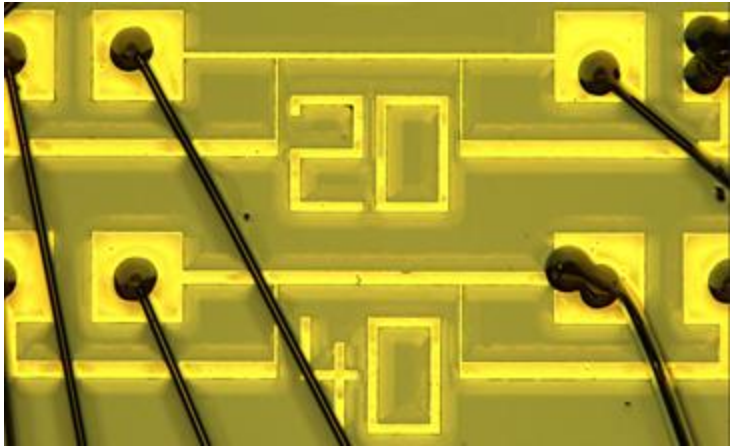
2nd Harmonic: Temperature across heater (Resistance)

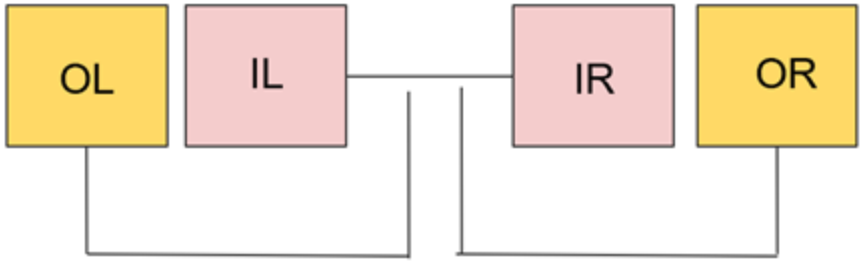
3rd Harmonic: Voltage shift

3 Omega Schematic (Cross Section)



3 Omega Schematic (Top Down)





Measurement Techniques- Scanning Thermal Microscopy

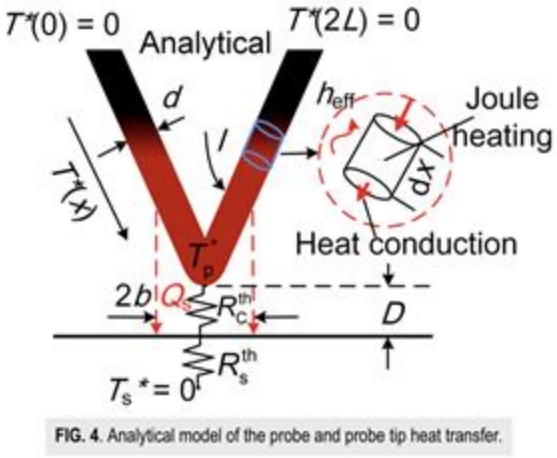
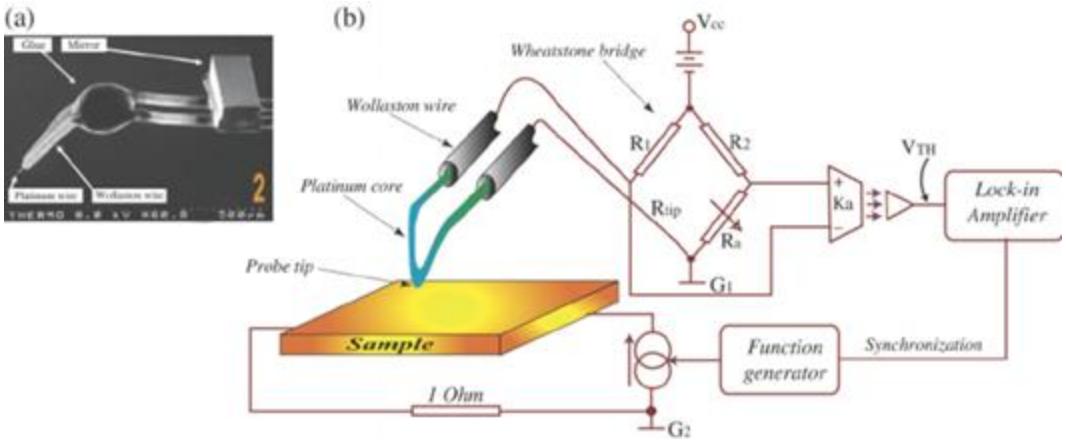


FIG. 4. Analytical model of the probe and probe tip heat transfer.

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