Lithography & Patterning

Jonas Kendra

GBM Attendance

General Updates

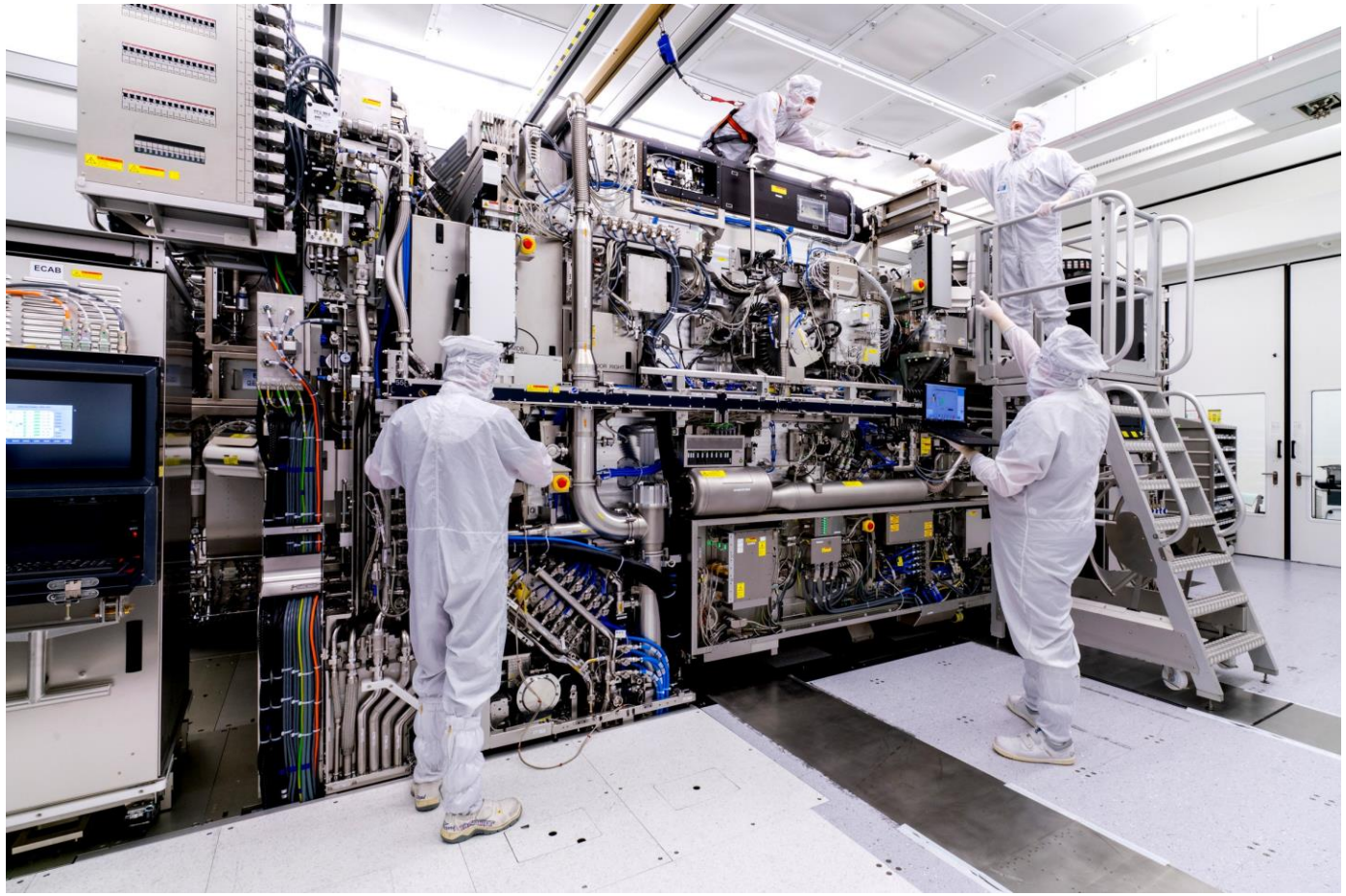
- Dr. Singh in 2 weeks
  - Electromigration

Albany Nanotech Complex Tour

- Albany Nanotech Complex
  - A state-of-the-art campus that brings together industry leaders, academia and international partners to develop next-generation chips and chip fabrication processes.
  - Major Companies:
    - IBM, Applied Materials, Tokyo Electron, Wolfspeed
  - Tour Dates:
    - February 26th (Wednesday), 11:30 AM – 1:30 PM
    - March 12th (Wednesday), 11:30 AM – 1:30 PM
- More tours are coming in the future!
- **<u>Tour attendees must be IEEE EPS members!</u>**

Overview

- Review of Fabrication Techniques
- Lithography Over the years
- Lithography Types & Settings
- Physics Behind Lithography
- Future State of Lithography

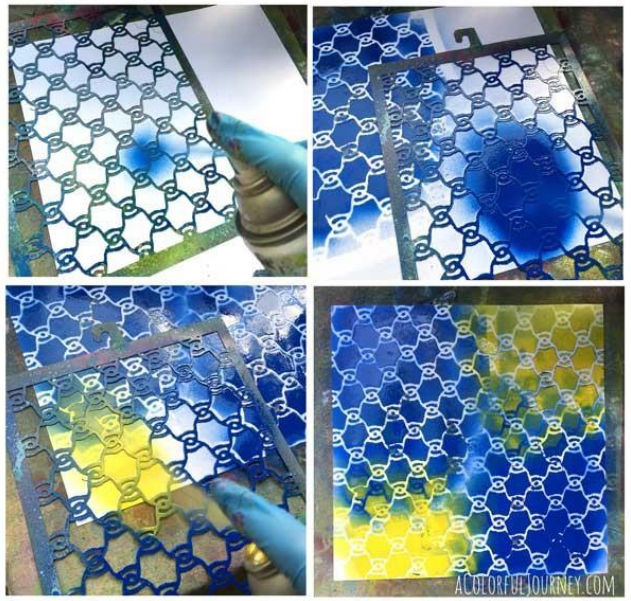


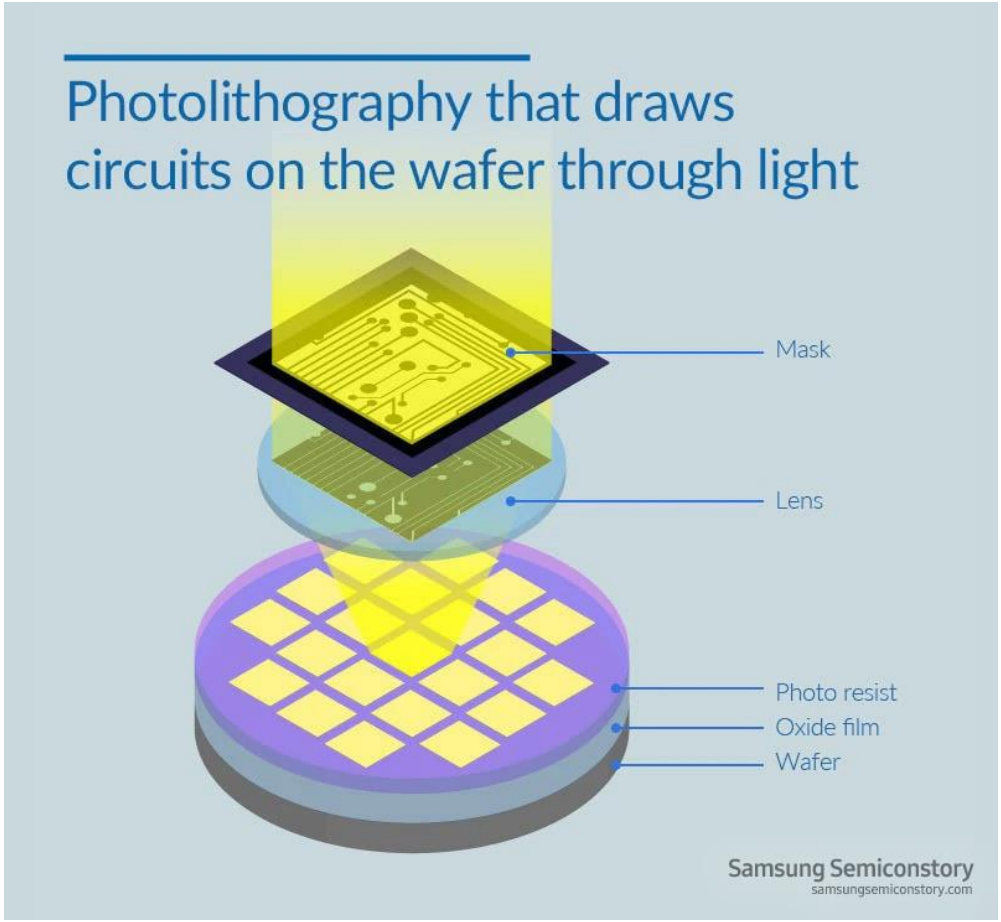
Fabrication Techniques

- Lithography (Framing)
- Implantation (Modification)
- Deposition (Additive)
  - Oxidation
  - Plating
- Etching (Subtractive)
  - Wet, Dry

Fabrication Techniques- Lithography

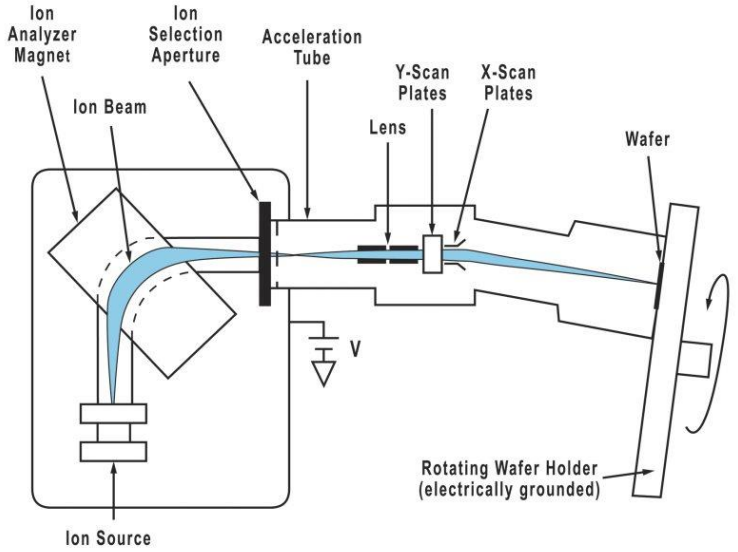
- Technique used to define where you want a pattern to stick
- In Semiconductor industry, involves wavelengths of light reacting with a chemical below
- New material can be added on top, or this can be seen as a stencil where material is removed

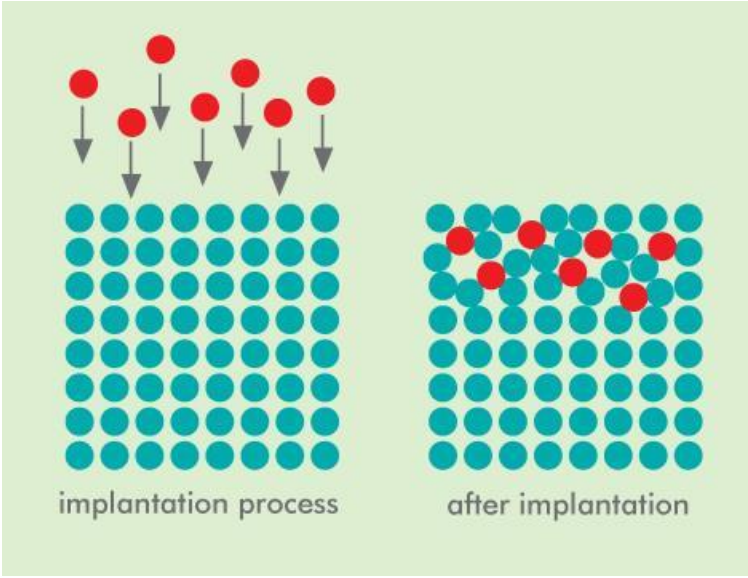




Fabrication Techniques- Implantation

- Used to modify properties of the wafer underneath
- In Silicon, dopants may result in excess electrons or holes (N, P-type)
- Slight changes in concentration results in large change in electrical conductivity (~100x)
- Always causes damage to substrate- must be repaired with an anneal step





Fabrication Techniques- Deposition

- Additive technique for wafer fabrication
- 3 (main) types
  - Oxidation
  - Deposition
    - Many sub-categories:
      - CVD, LPCVD, PVD, PECVD…
  - Electroplating

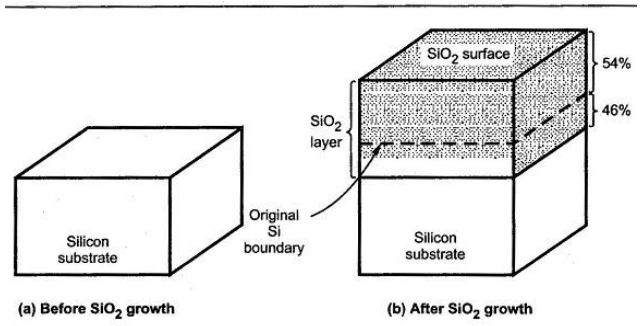
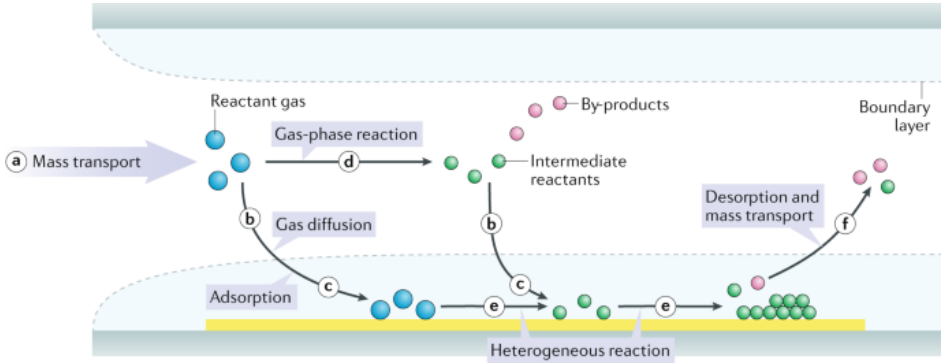
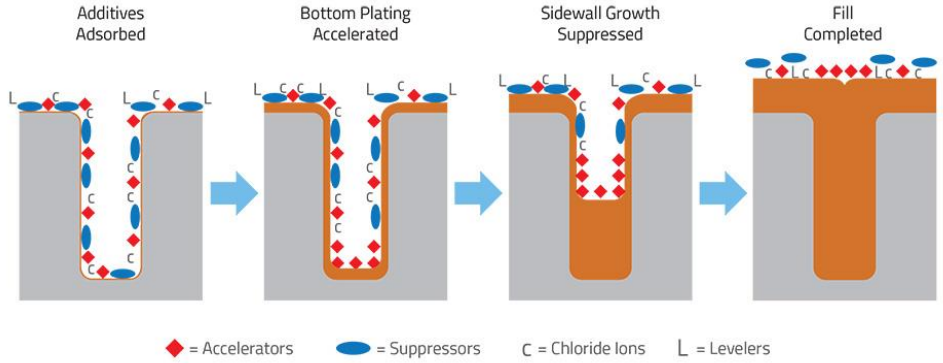


Fig. 1.4 Thermal Oxidation





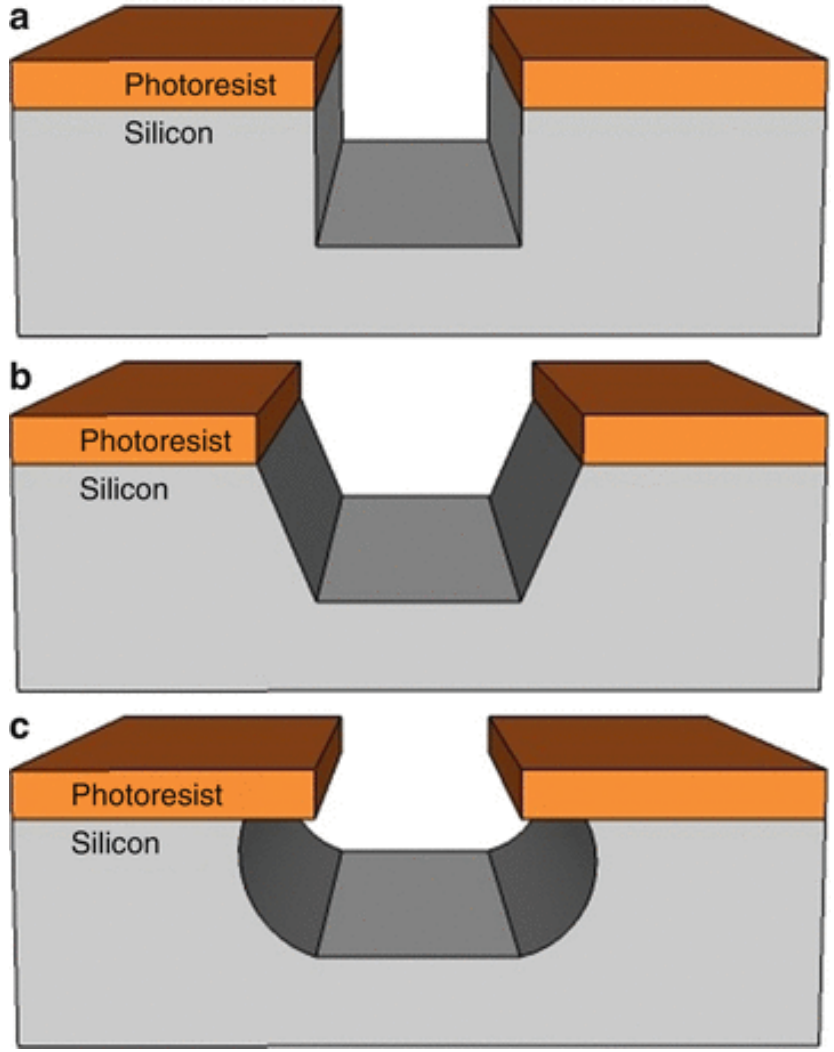
Fabrication Techniques- Etching

Two important characteristics

- Selectivity: How quickly one material is etched relative to another
- Anisotropy Ratio: How quickly material is consumed in a certain direction versus another

Two main types

- Wet Etching (Typically with acids/other wet chemistry)
- Dry Etching (Typ. Reactive Ion Etching)

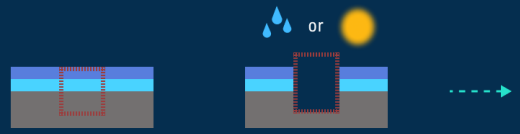


Fabrication Techniques- Etching

TOPSEIKO

Etching process overview

Etching is a crucial process in semiconductor manufacturing used to create patterns and structures. It involves selectively removing material to define circuitry and features. Etching is classified into **wet** and **dry** methods.



Dry etching is a physical-based process using plasma, a highly ionized gas. The substrate is placed in a vacuum chamber, and plasma generated using reactive gases chemically reacts with the material, removing the exposed portions. Dry etching offers precise control and anisotropic etching.

Both wet and dry etching play vital roles in semiconductor manufacturing. Wet etching is cost-effective and used for large-area patterning. Dry etching provides better control and precision for complex and fine-scale patterning.

COST EFFECTIVE / SPEED = WET ETCHING (ISOTROPIC)

PRECISION / CONTROL = DRY ETCHING (ANISOTROPIC or ISOTROPIC)

Wet etching is a chemical-based process where the substrate is immersed in a chemical solution called an etchant. It dissolves or etches away the exposed material uniformly in all directions. Wet etching is suitable for isotropic etching.

Dry etching techniques include reactive ion etching (RIE), plasma etching, and ion beam etching. These techniques allow for precise and intricate patterning required in advanced semiconductor devices. Dry etching is commonly used for achieving high-resolution patterns.

The choice between wet and dry etching depends on specific requirements. Wet etching is advantageous for simplicity and cost-effectiveness, while dry etching offers greater control and precision. The appropriate etching method is selected based on pattern resolution, device complexity, and production cost considerations. Etching enables the creation of intricate circuitry and structures in semiconductor manufacturing.

Lithography Over the Years

- What is the goal for Lithography Machine Companies?

Lithography Over the Years- Characteristic Equation

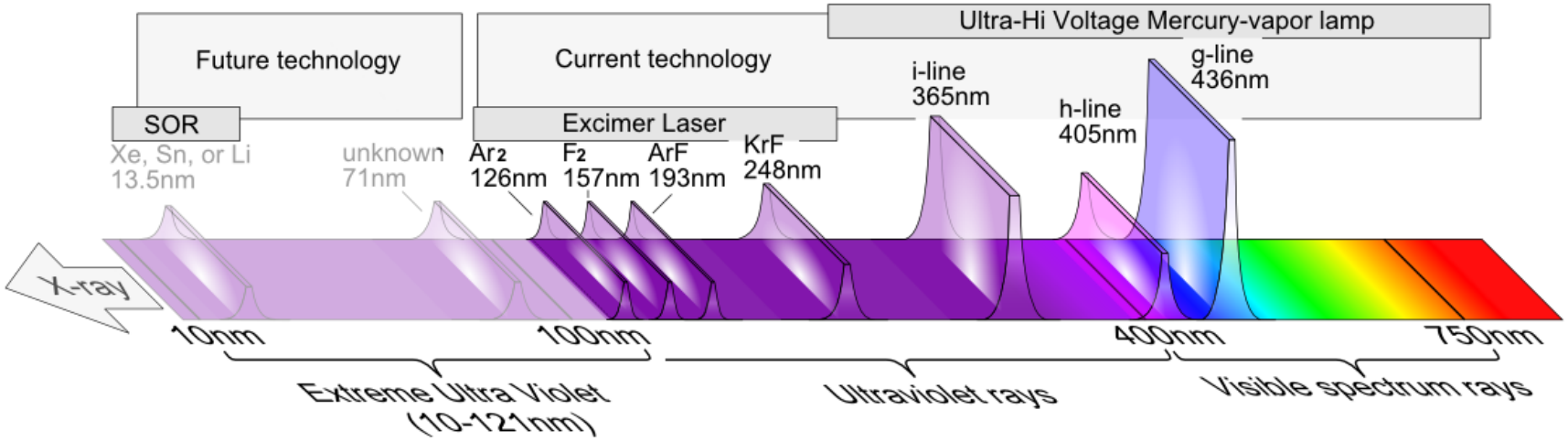
- CD: Critical Dimension (Minimum feature size)
- K1: Process Coefficient
  - Typ. 1, Can go to ~0.5 or lower
- Lambda: Wavelength of incoming light
- NA: Numerical Aperture
  - Typ. 0.5-0.7, can go above 1

We'll come back to this…

$$CD = k_1 \frac{\lambda}{NA}$$

Lithography Over the Years- Wavelengths

- Mercury Lamp
  - G-line, I-line, H-line
- Laser
- DUV/EUV



Lithography Over the Years- Wavelengths

Technology generation	Wavelength (nm)	Exposure source
EUV G LINE	436	Mercury
EUV H LINE	405	Mercury
EUV I LINE	365	Mercury
Excimer laser	248	KrF
Excimer laser	193	ArF
Excimer laser	157	F2
Extreme ultraviolet	13. 5	Tin vapor

????

https://www.youtube.com/watch?v=ZPa_RKFTBPc

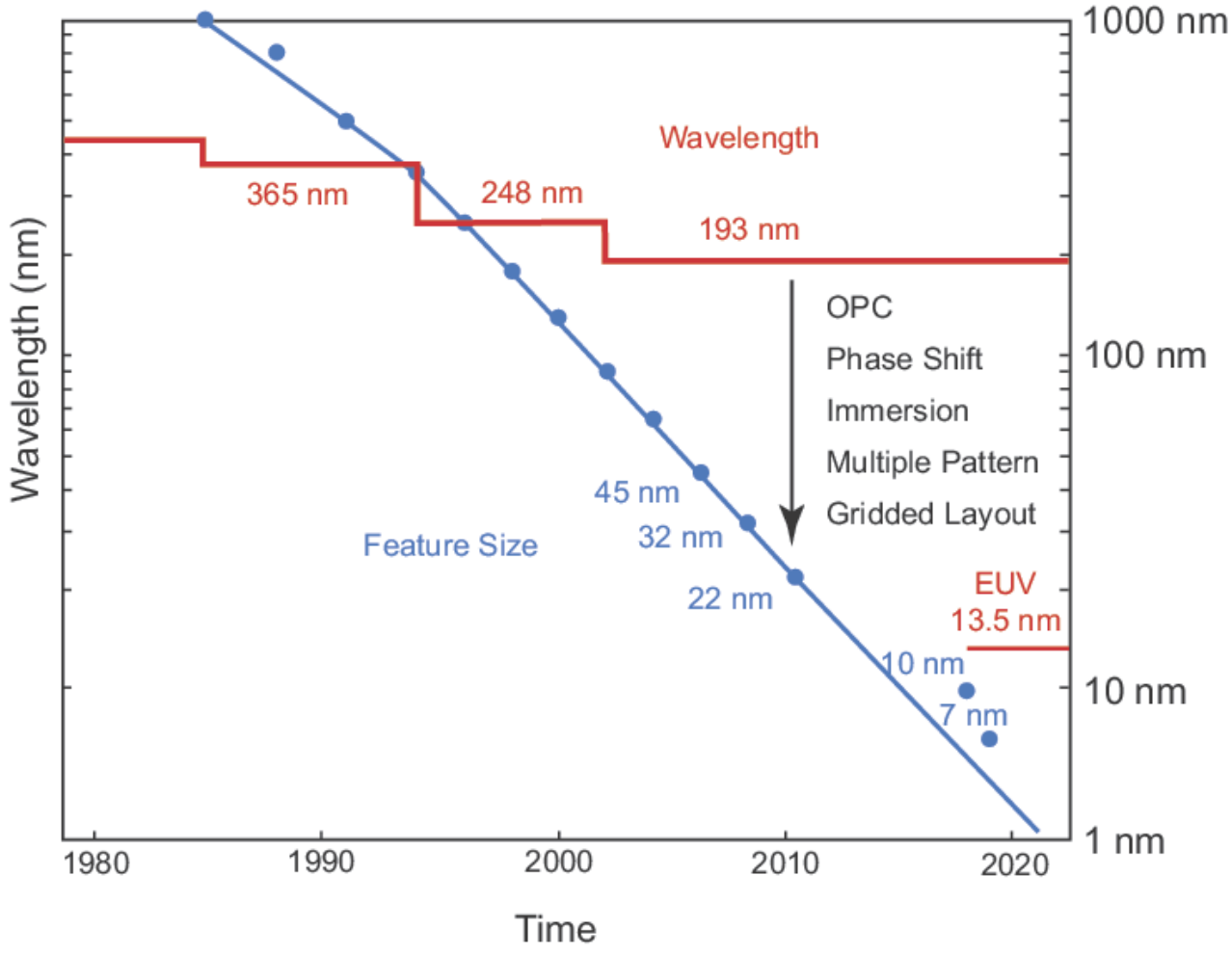
Lithography Over the Years- Why 193???

Before 1990:

- "Like drawing thick lines with a sharp pencil"

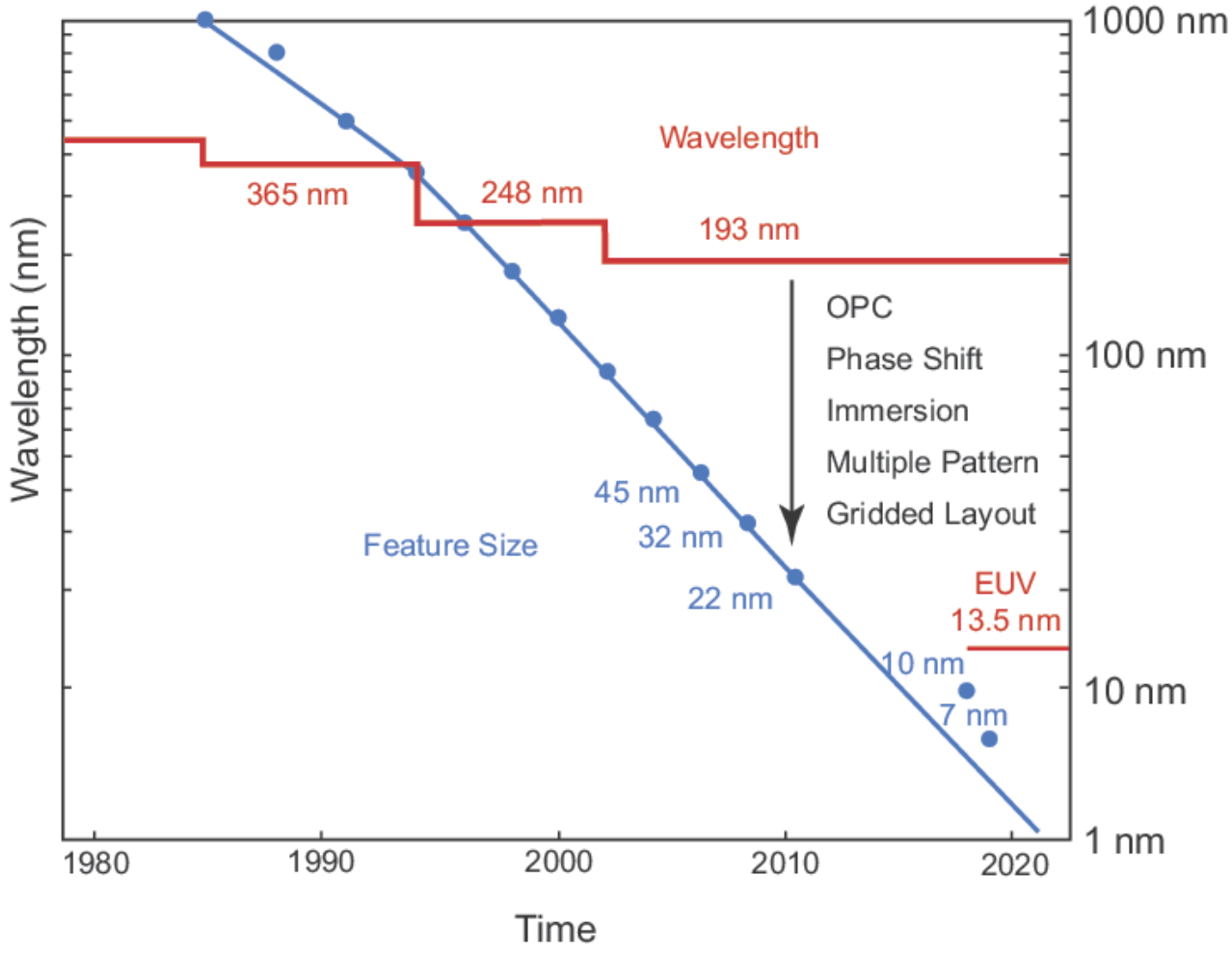
After 1990

- "Mask Designer's Nightmare"



Lithography Over the Years- What happened to 157?

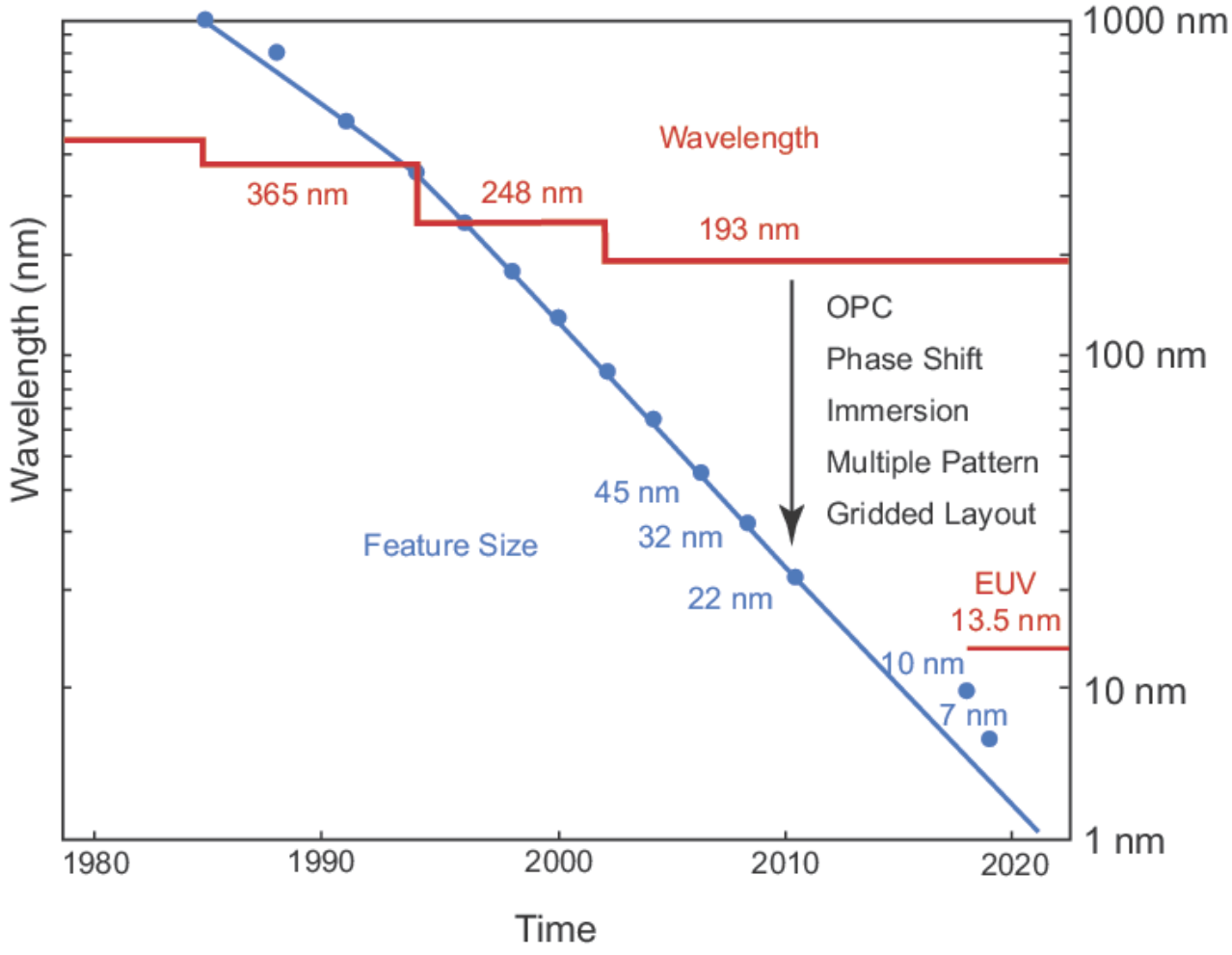
- Poor Photoresist
- Needed new reticle design
- Expensive processing
- Immersion technology!?
- EUV *supposed* to come out in 2001



Lithography Over the Years- What happened to 157?

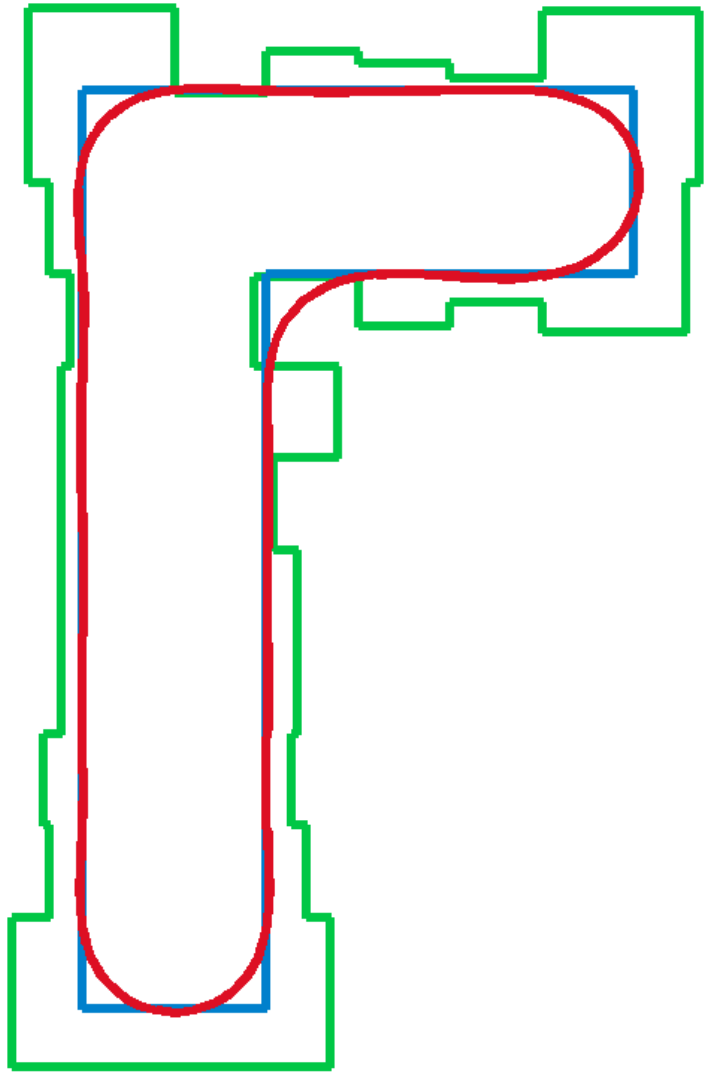
- Poor Photoresist
- Needed new reticle design
- Expensive processing
- Immersion technology!?
- EUV *supposed* to come out in 2001

  (GTA6 of Semiconductor Industry)



Brute Force for Moore's Law (k1)- OPC

- Optical Proximity Correction

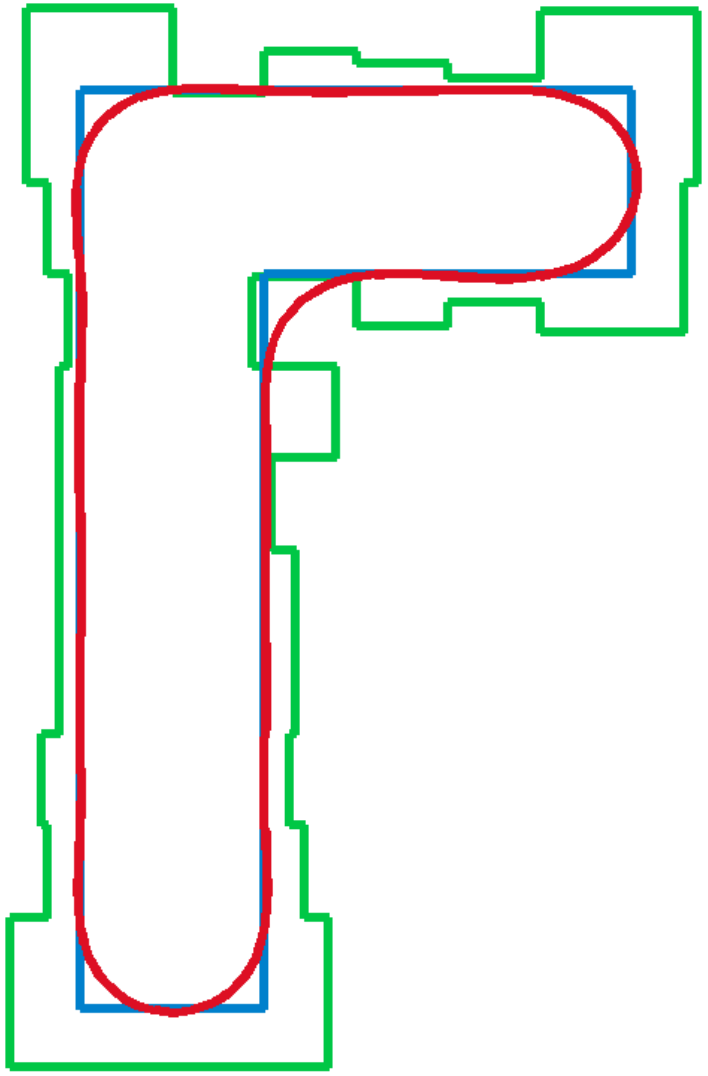


Brute Force for Moore's Law (k1)- OPC

- Optical Proximity Correction

Constructive/Destructive Interference- Introduce Serifs/additional patterns so OUTPUT looks correct (Mask doesn't)

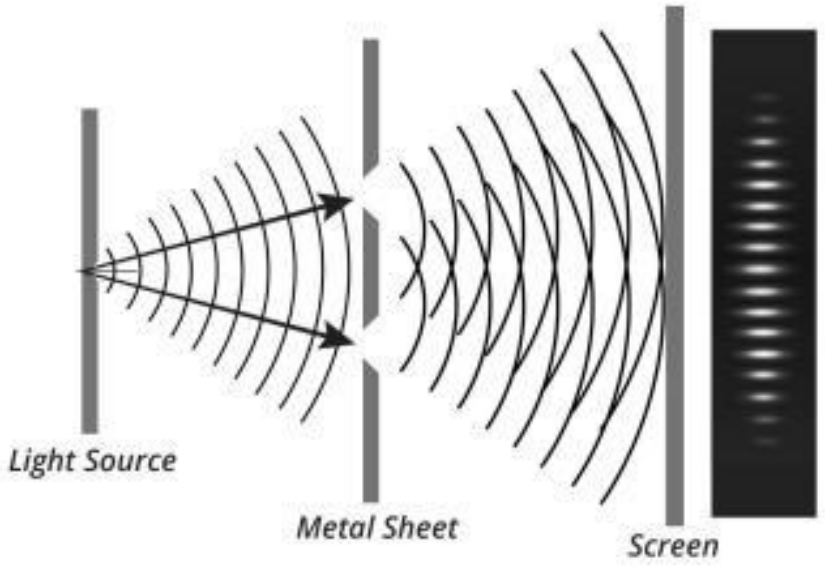
VERY interesting field for optics engineering & computer science

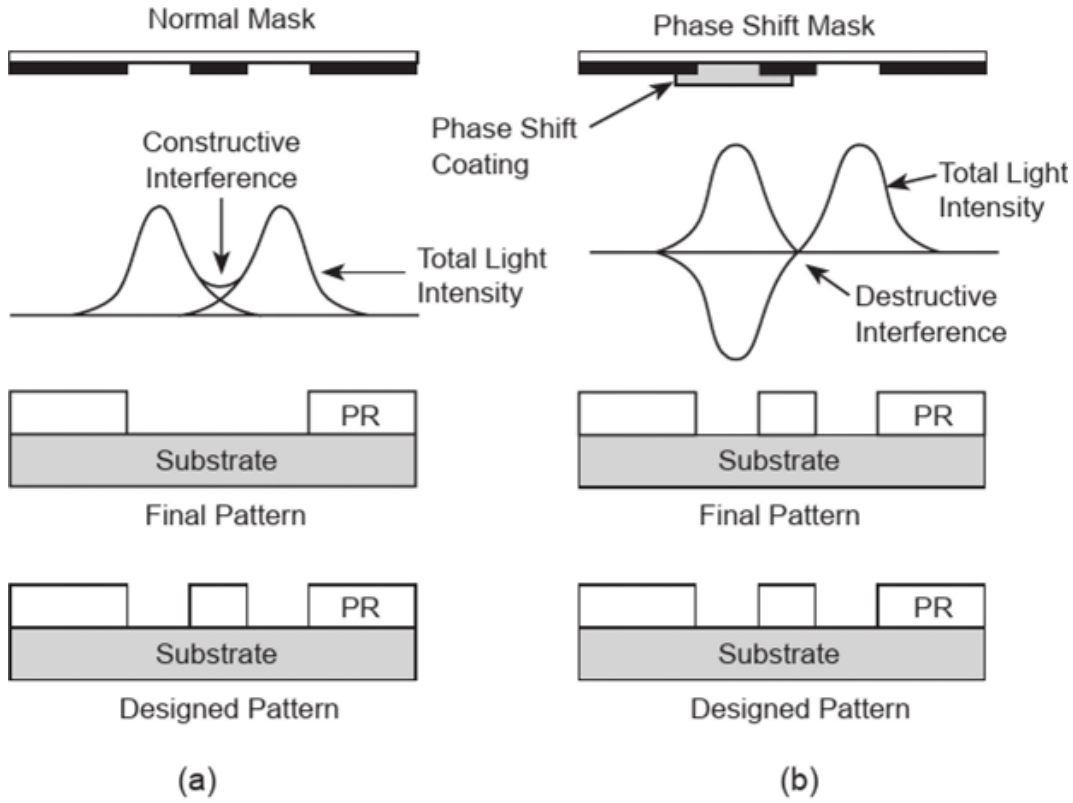


Brute Force for Moore's Law (k1)- Phase Shift

- Optical Proximity Correction

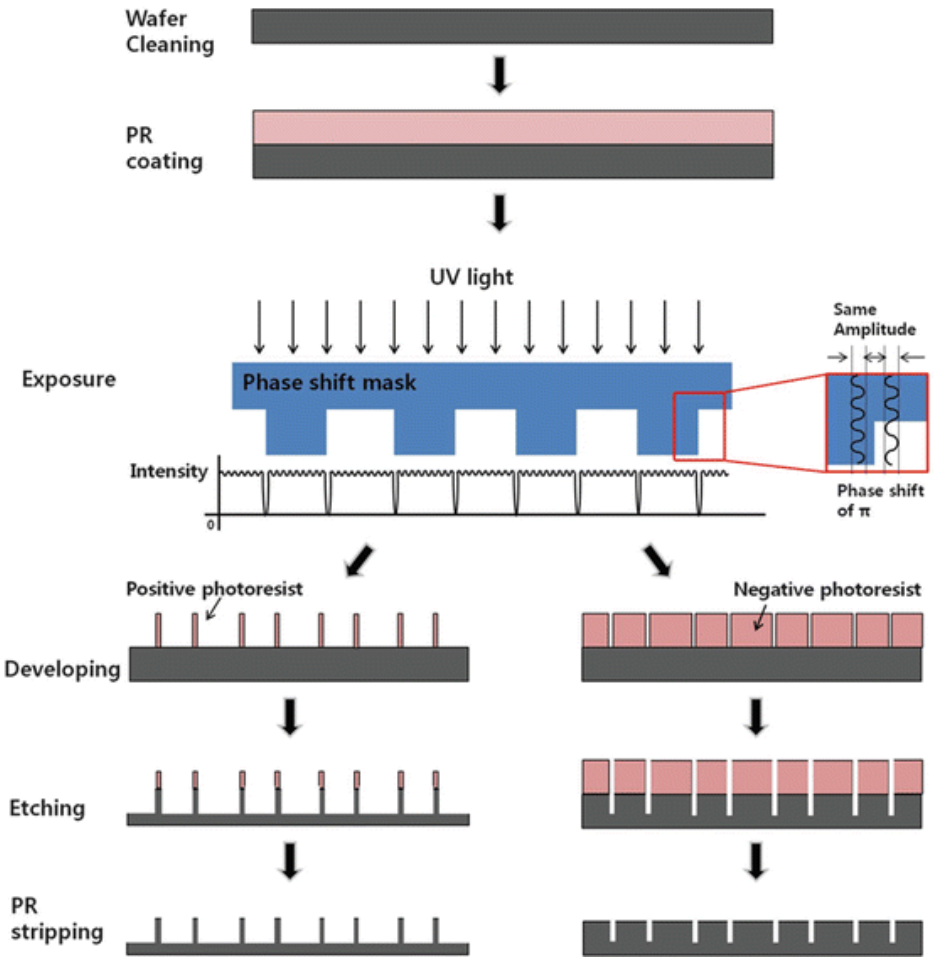
Constructive/Destructive Interference- Introduce Serifs/additional patterns so OUTPUT looks correct (Mask doesn't)





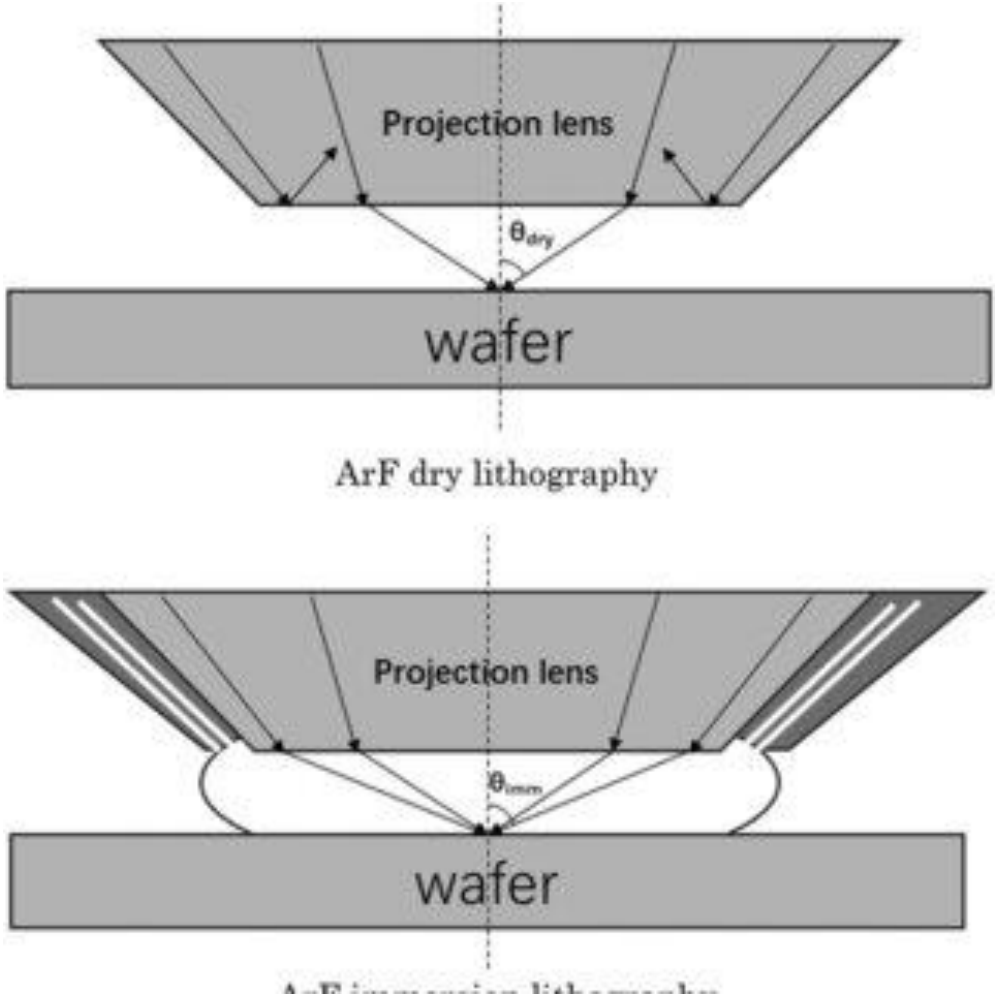
Brute Force for Moore's Law (k1)- Phase Shift

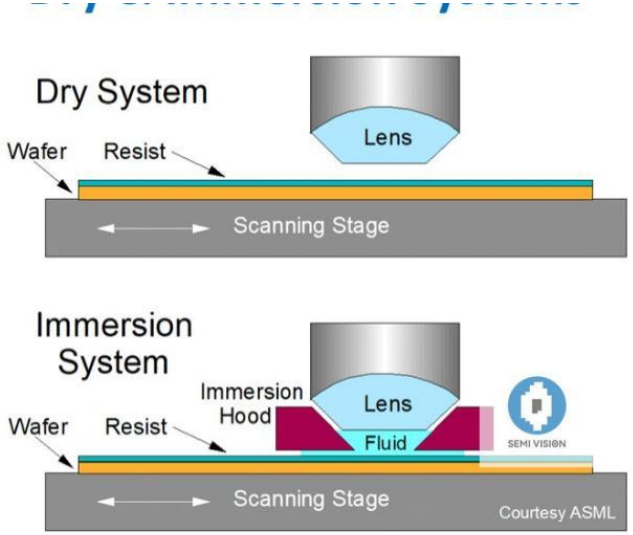
- Mask Design No longer Binary
- Designed constructive/destructive interference for high-resolution output



Brute Force for Moore's Law (NA)- Immersion Lithography

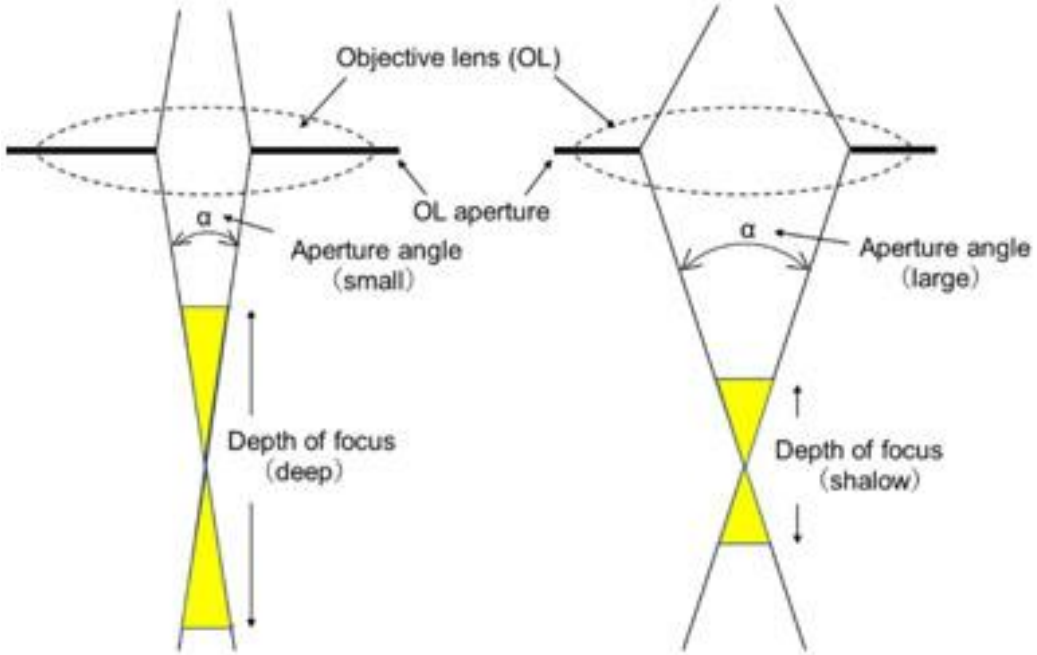
- Happy Mask Designer ☺
- Increase Numerical Aperture (Sharper Focusing of light)





Brief Aside- The issue with NA

- More precision in distance from lens
- In EUV, photoresist needs to be ~10s of nm thick
- Remember our “Selectivity” equation from earlier?

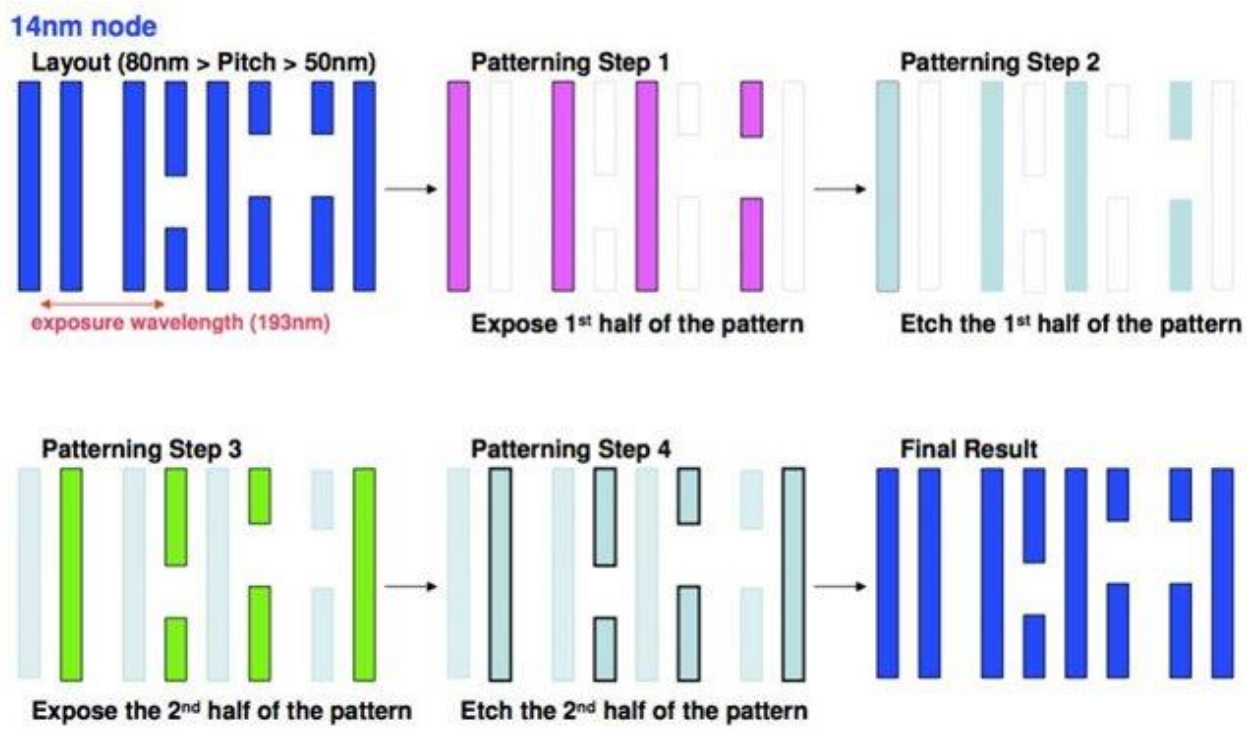


$$DOF = K_2 \frac{\lambda}{NA^2}$$

K_2 : depending on the criteria used to define acceptable imaging & on the type of feature

Brute Force for Moore's Law (k1)- Double Patterning

- Solve Interference Problem by just making more masks
  - 2x, 4x patterning

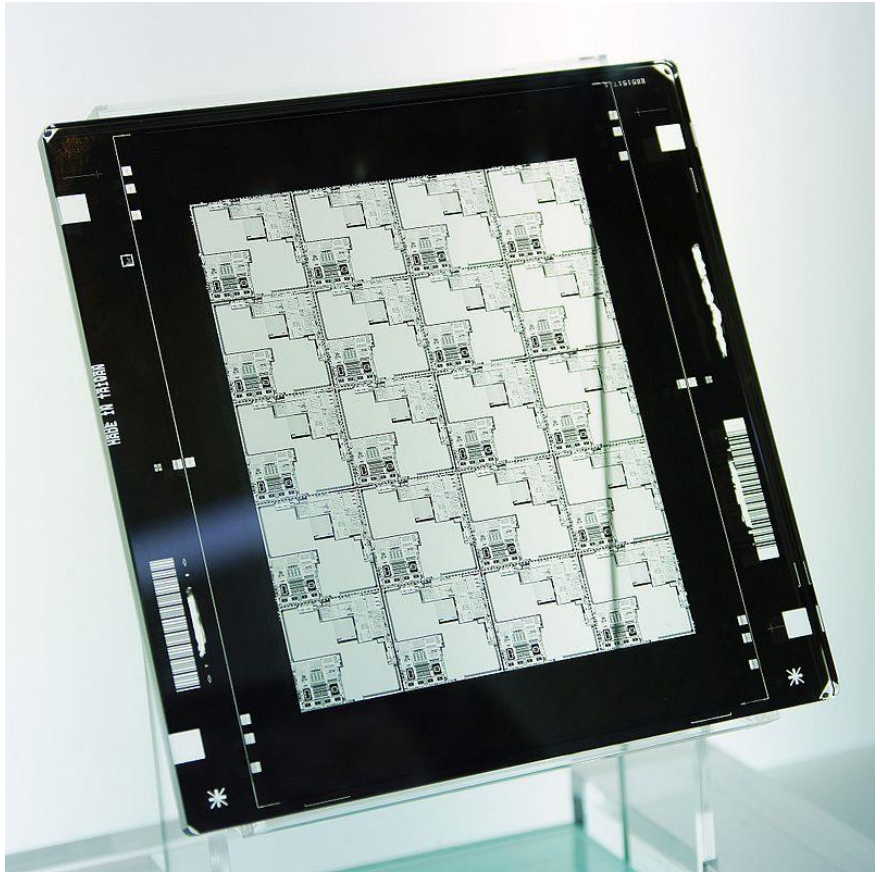


POV: Mask designers selling more masks to do the same work

Mask Design

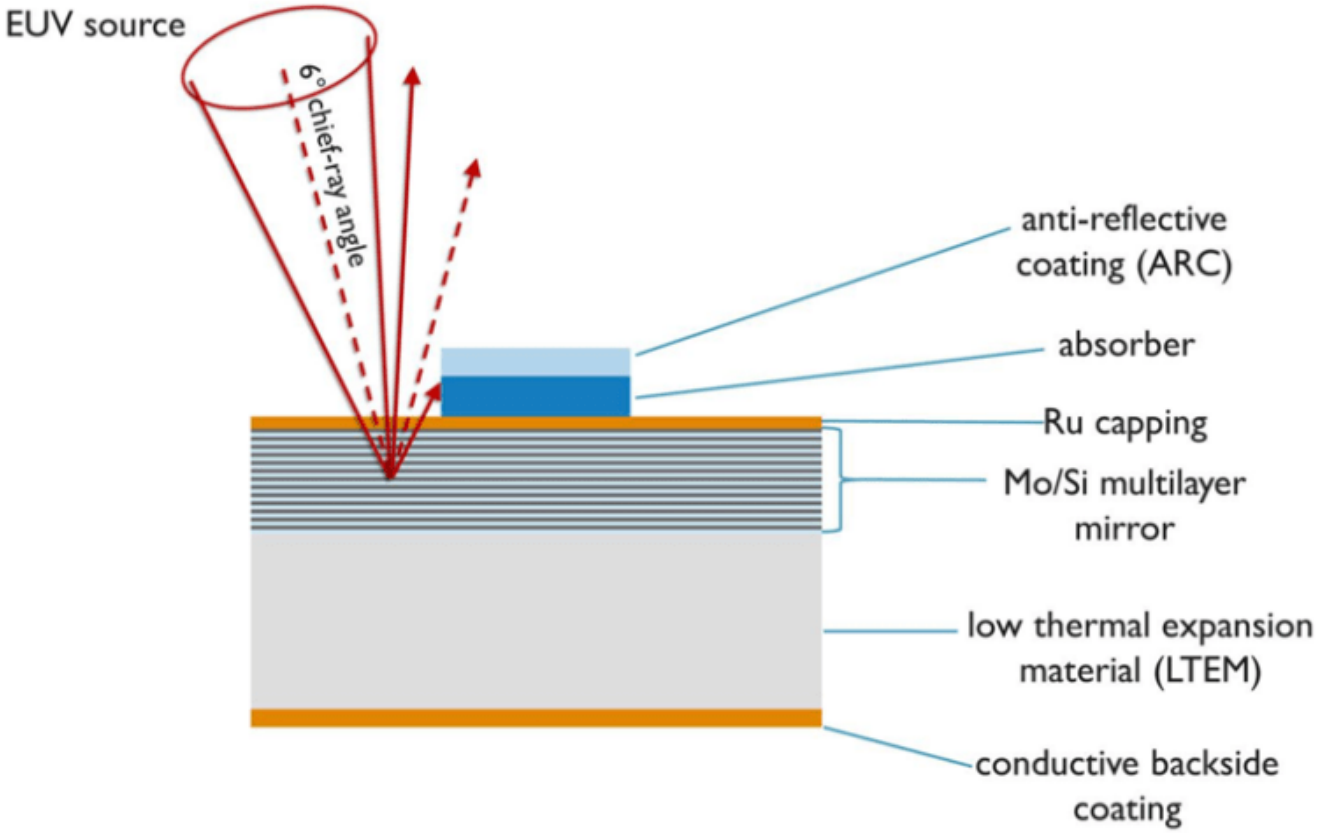
- Exposure Area:
  - Limited by Reduction Lenses
  - ~26x33 mm max
- DUV/Older systems:
  - Quartz (Fused Silica)
  - Chromium
  - Can cost ~10-100k

https://youtu.be/9RZreu5z_Gc?si=rI32Z36lvvmAOuUI

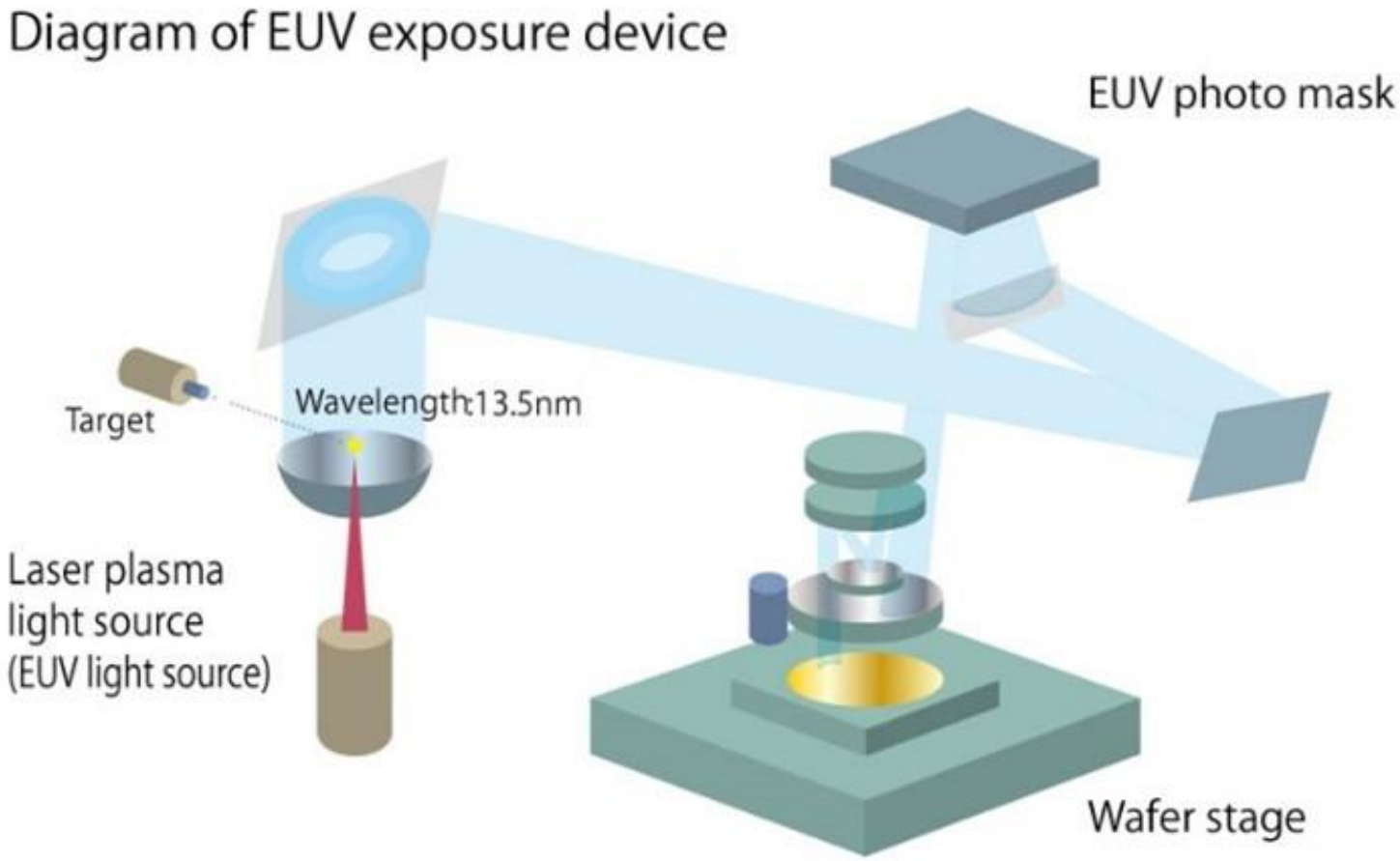


Mask Design (EUV)

- Extremely Expensive
  - “Mirror mask”
  - Most energy is adsorbed (High heat gen)
  - 50+ layers inside, Molybdenum, Silicon
  - Can cost ~500k each

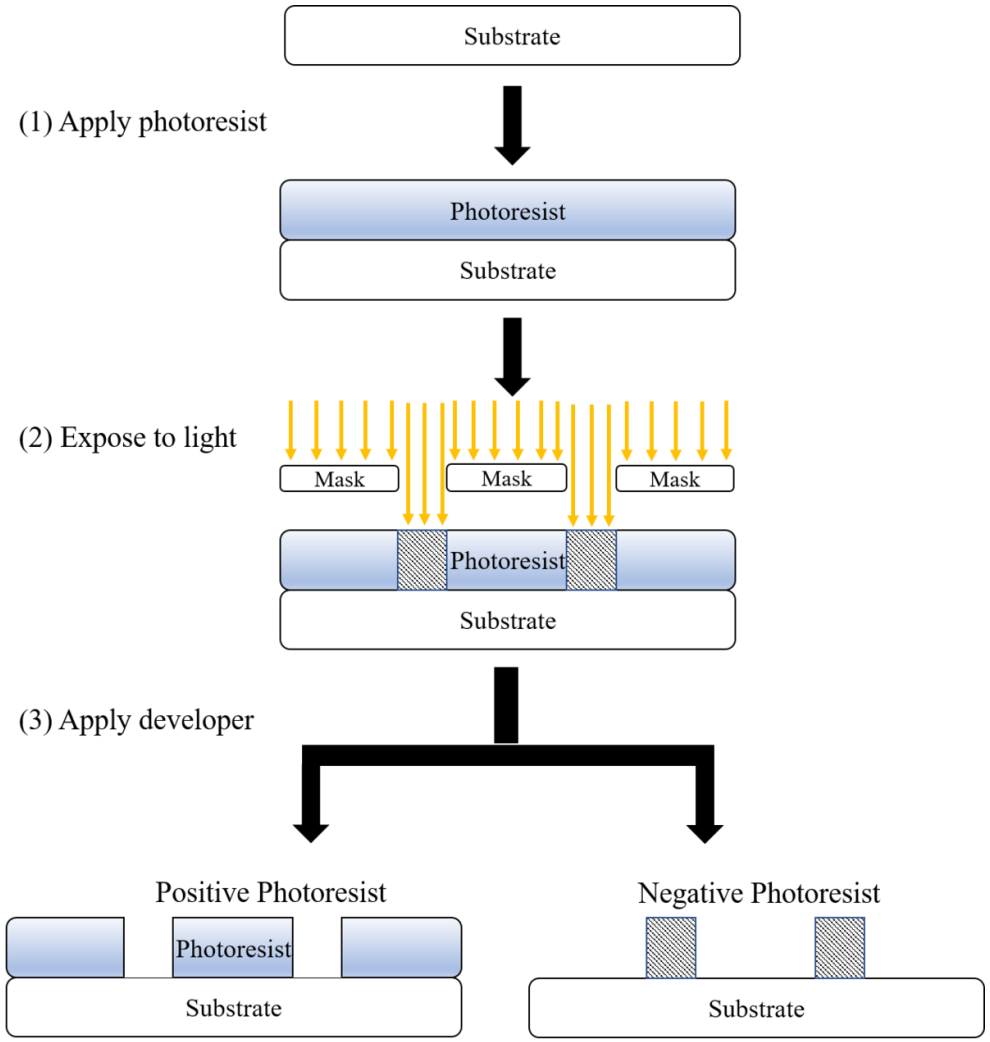


Mask Design (EUV)



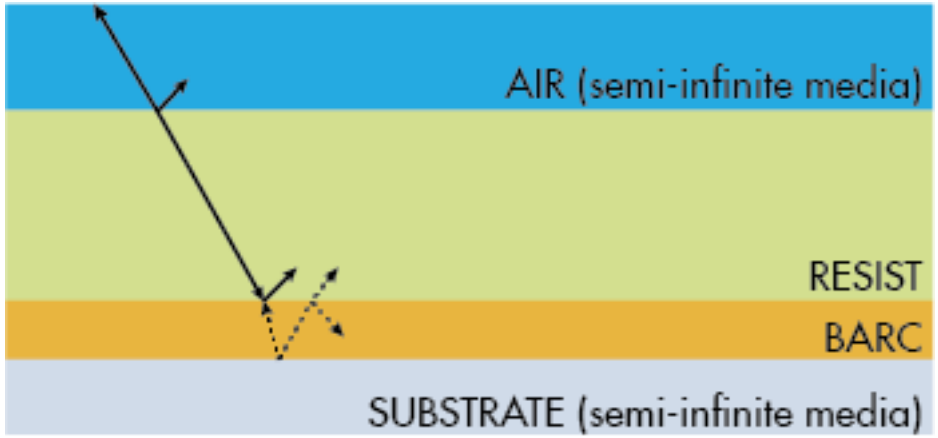
Photoresist

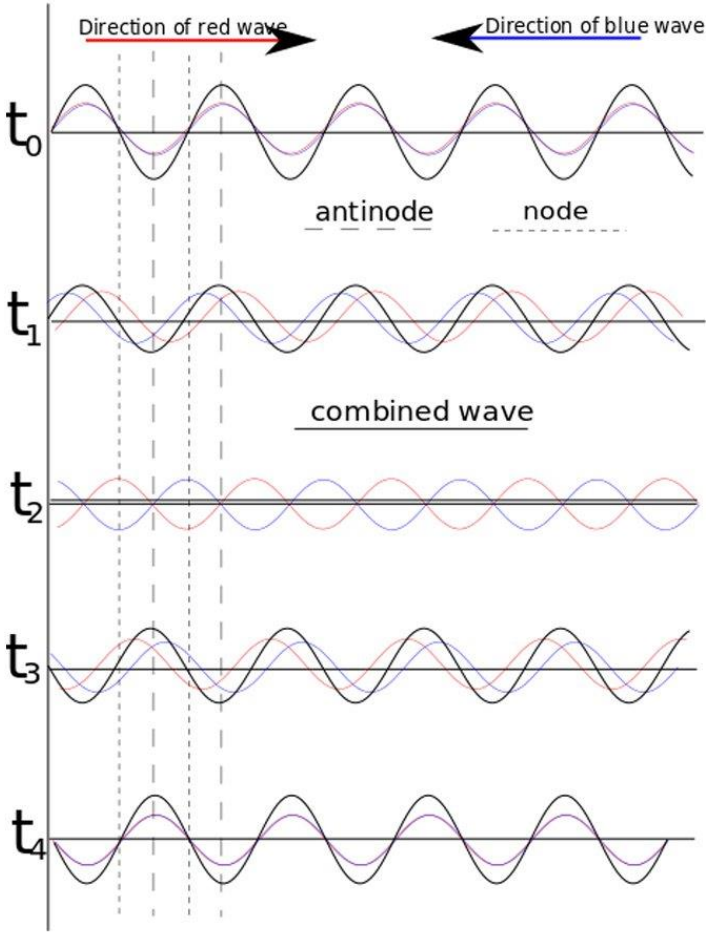
- Large, Organic polymers
- When exposed to light, cross-linking occurs between polymers
- Good photoresist requires the following
  - Specific wavelength sensitivity
  - High uniformity
  - Very strong chemical resistance (When exposed)
  - Easy development (Removal of “blank” areas)
  - *Limiting factor for new wavelengths!*



Weird Photoresist (EUV)

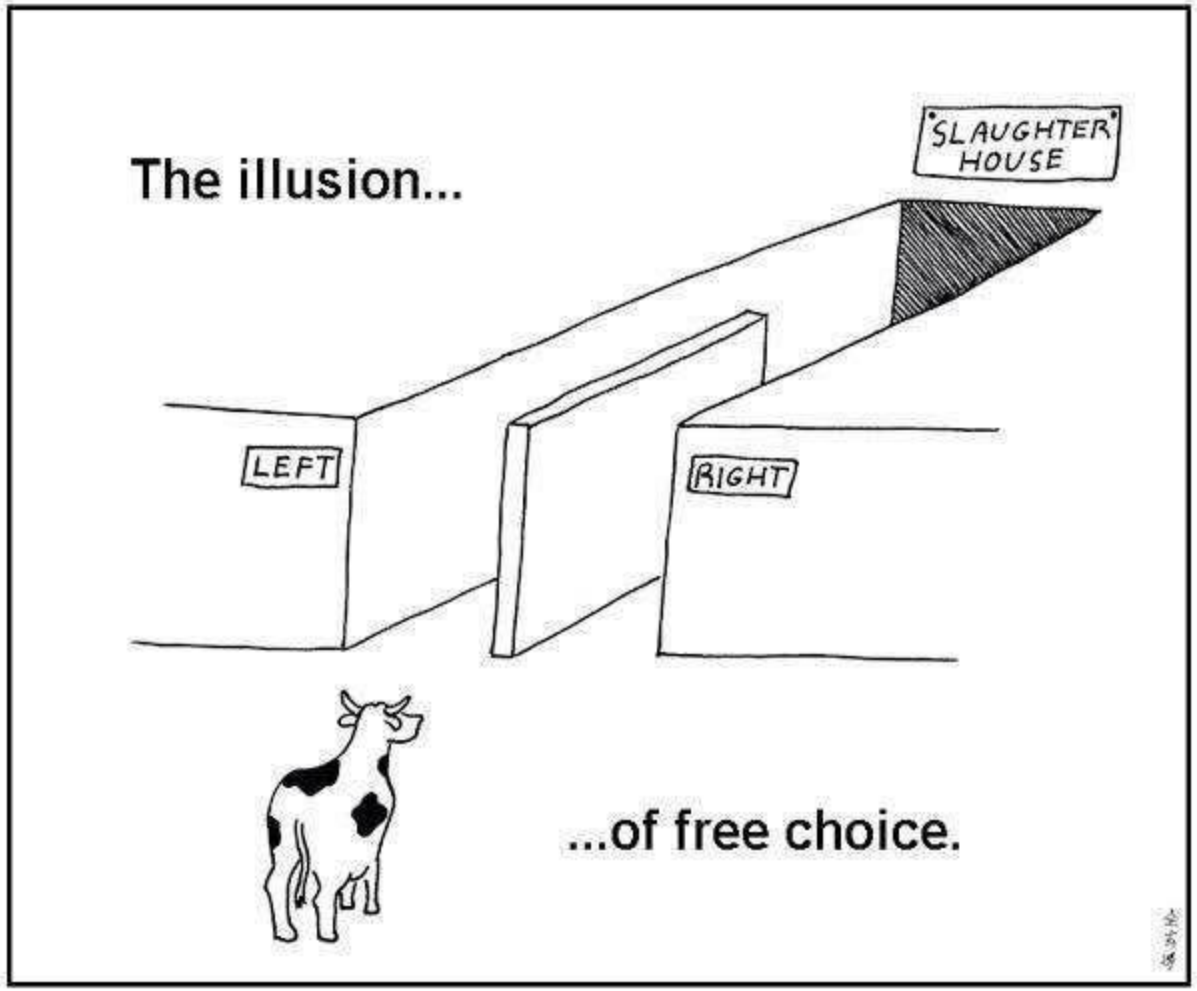
- Etch rate additives
  - Actual resist is too thin to work long enough…
- BARC/Underlayers
  - Reduce “Standing waves”
  - Improve adhesion/resolution



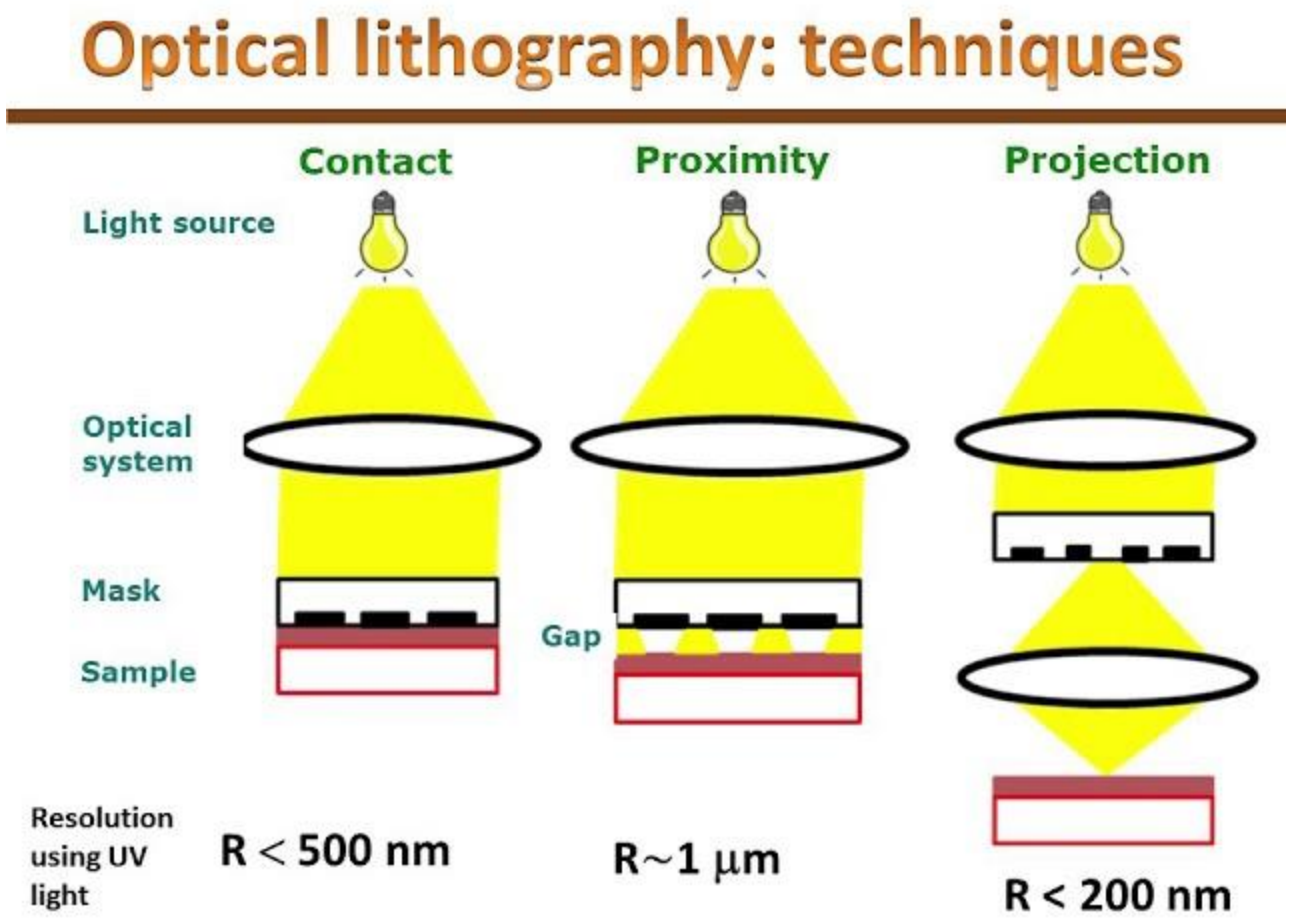


Lithography Types- “Choose your own adventure”

- Contact
- Non-Contact
- Projection
- E-beam*



Lithography Types- “Choose your own adventure”



Lithography Types- Performance Comparison

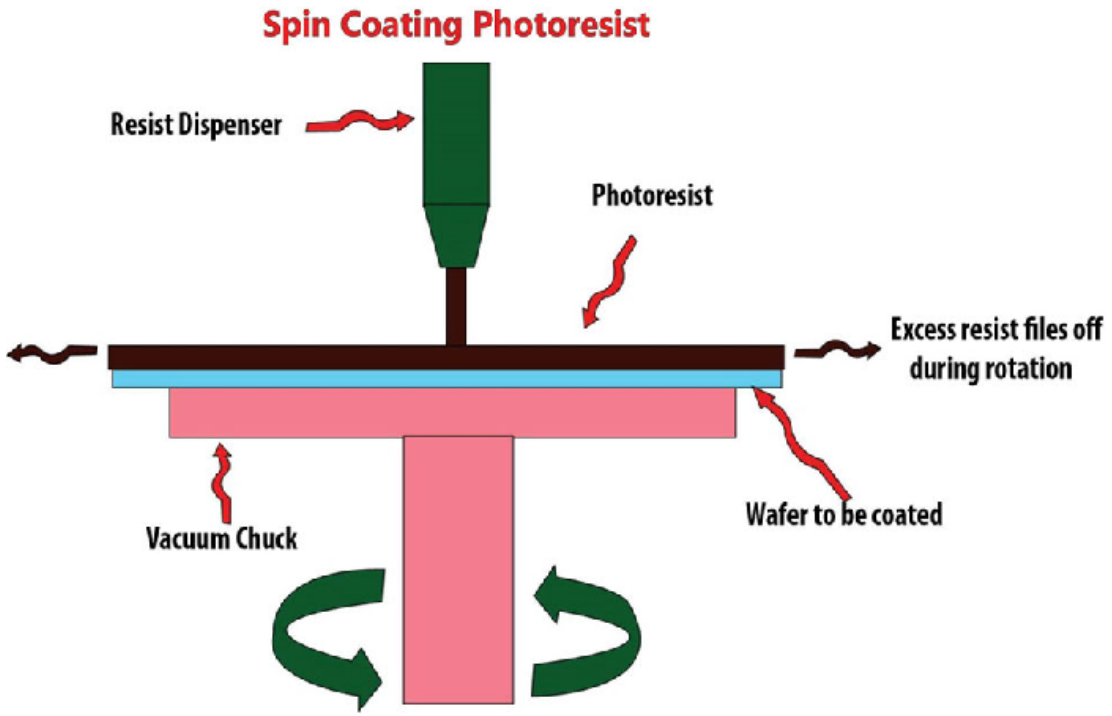
- Each are useful!
  - Which would you use for…
    - Academic (Very low volume)
    - Industry (High Volume)
    - Research

Parameter	Contact	Non-Contact	Projection	E-beam
Cost	Low	Low	High	High
Speed	Med	High	High	Low
Defectivity	Very High	Low	Low	Low
Resolution	Med	Low	High	Very High
Complexity	Low	Med	High	Med

Lithography Procedure

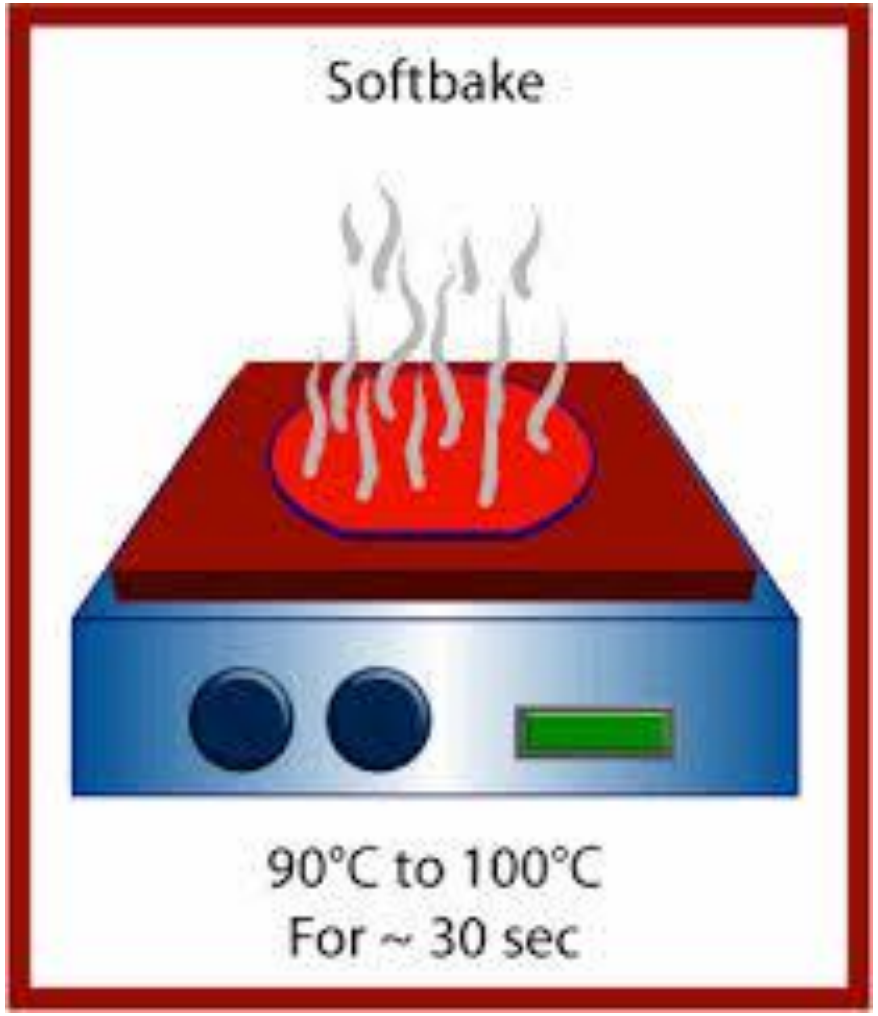
- Spincoat
- Soft-Bake
- Expose
- Post-exposure Bake (Optional)
- Develop
- Hard-Bake

Lithography Procedure- Spincoat



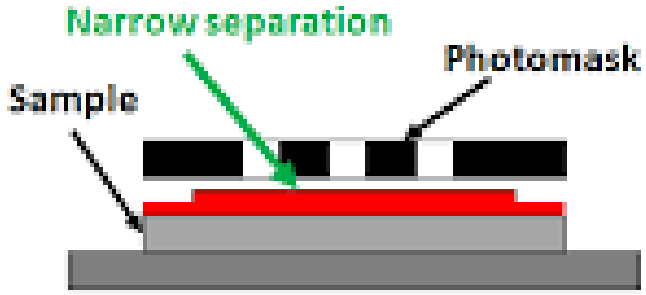
Lithography Procedure- Softbake

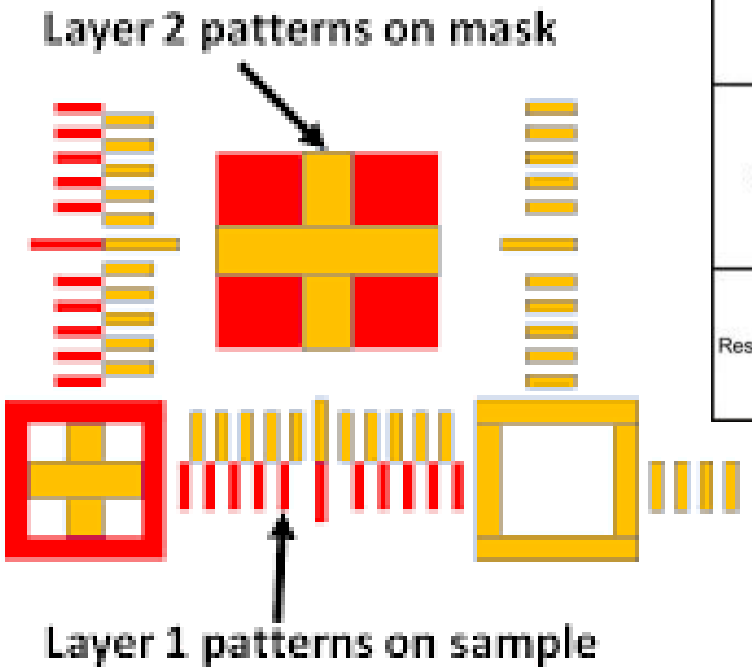
- Solidify photoresist
- Removes solvent
- Can be done with hotplate in research applications
- Integrated in lithography machine for industry applications

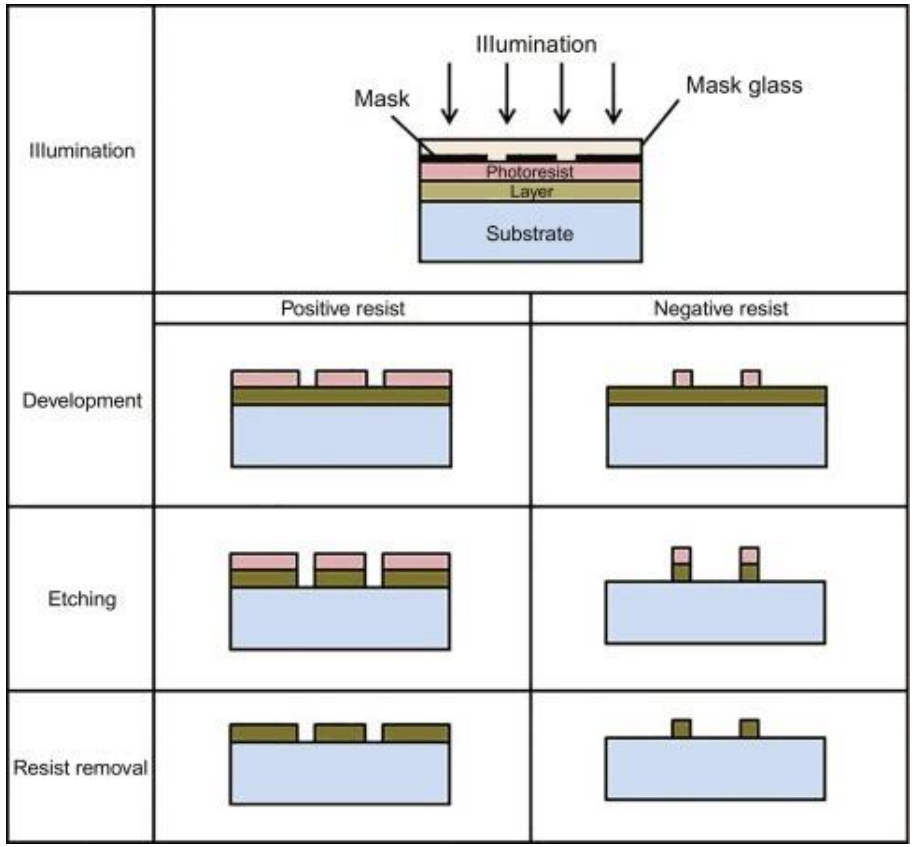


Lithography Procedure- Exposure

- Align with previous layers of mask
- Use lightsource (EUV, DUV, etc) to bond photoresist

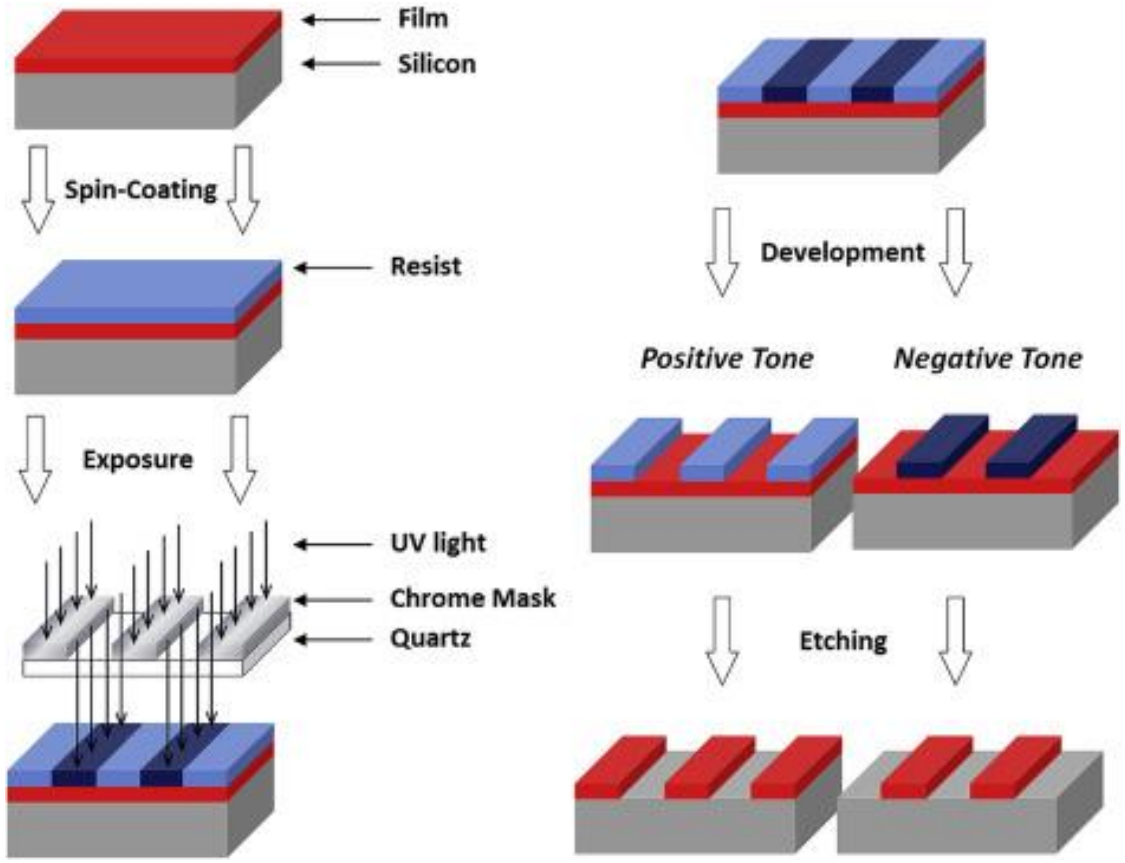






Lithography Procedure- Develop

- Dissolves un-bonded photoresist



Lithography Procedure- Modern Systems

https://youtu.be/h_zgURwr6nA?si=Jx0LdQDefZiJwbs1

Future State of Litho

- Bringing back Advanced OPC?
- Larger exposure field? (Reticle)
- Mechanical Improvements for High-Throughput/Precision
- Cutting Cost???

The End

Thanks for listening!

GBM Attendance