# EPS Info Session

## Heterogeneous Integration Overview

GBM Attendance

# Meet our EPS executive board

## David King
*Chair*

- Class of ‘27
- Computer Systems Eng. and Electrical Eng.
- Clubs/Affiliations:
  - IEEE

## Evan Chen
*Vice Chair*

- Class of ‘27
- Computer Systems Eng. And Electrical Eng.
- Clubs/Affiliations:
  - HackRPI

## Xinyan Li
*Secretary*

- Class of ‘28
- Electrical Eng.
- Clubs/Affiliations:
  - Undergraduate ECSE Council
  - Student Government

## Jonas Kendra
*Treasurer*

- Class of '24 (M.E.)
- Mechanical Eng.
- Clubs/Affiliations:
  - Engineering Ambassadors
  - Rensselaer Motorsport
  - RPI Esports

**WE NEED OFFICERS. WE WANT YOU!**

# What is IEEE EPS? (Generally)

A chapter of the Institute of Electrical and Electronics Engineers (IEEE) Electronic Packaging Society (EPS)

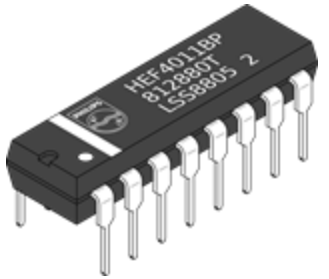
We are a community for people interested in microsystems technology:

- Hardware Design
- Integrated Circuit Manufacturing

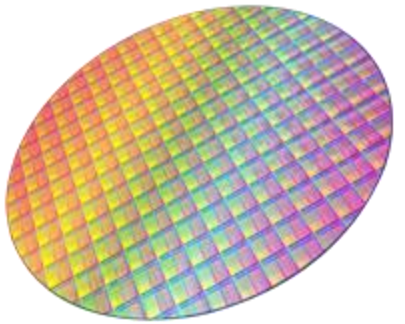
# What is IEEE EPS? (Technically)

"The IEEE Electronics Packaging Society is the leading international forum for scientists and engineers engaged in the research, design and development of revolutionary advances in microsystems packaging and manufacturing."

IEEE EPS Website – About Us




Packaging



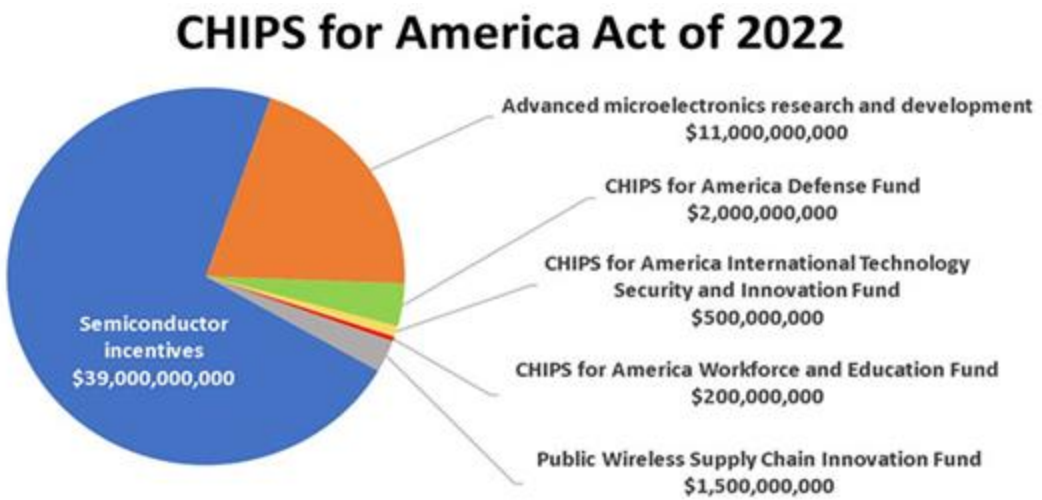
Manufacturing

# Why does EPS exist here and now?

## A weirdly specific question

# Government Support

- Intended to bring manufacturing back to the US to secure supply chains and stay competitive with China.
- Funding distributed over ~one decade
- Investment in education, infrastructure, and manufacturing
- Over 100,000 new jobs are being created between construction, manufacturing, and research.

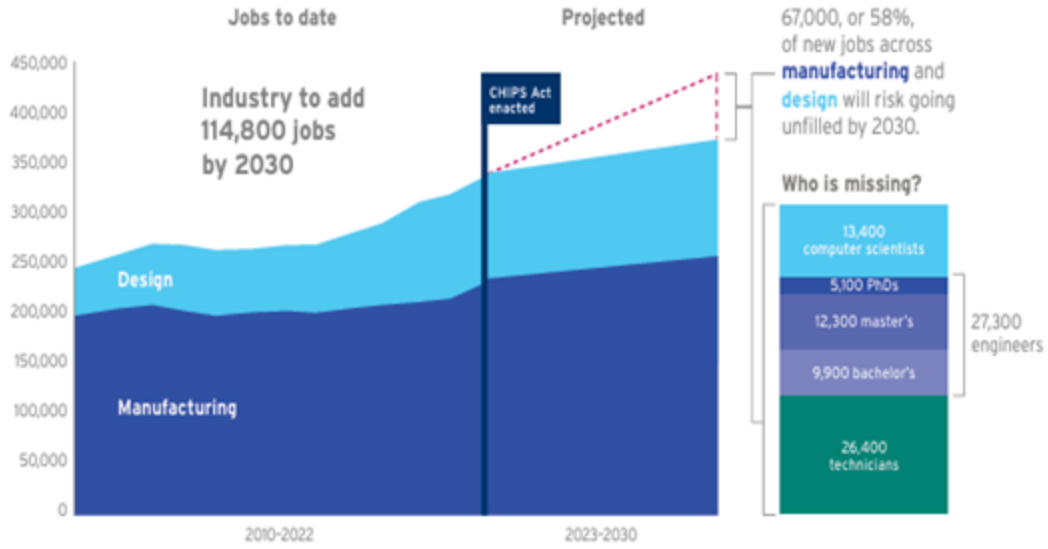


# Talent Shortage

## The Problem

**Significant Shortage:** The U.S. semiconductor industry faces a severe shortage of hardware designers, with an estimated shortfall of 59,000 to 146,000 workers, including engineers, by 2029

**Increasing Demand:** The demand for semiconductor engineers is projected to grow significantly, with annual demand growth expected to peak around 2027. This will be challenging to meet, given the current training and education pipelines

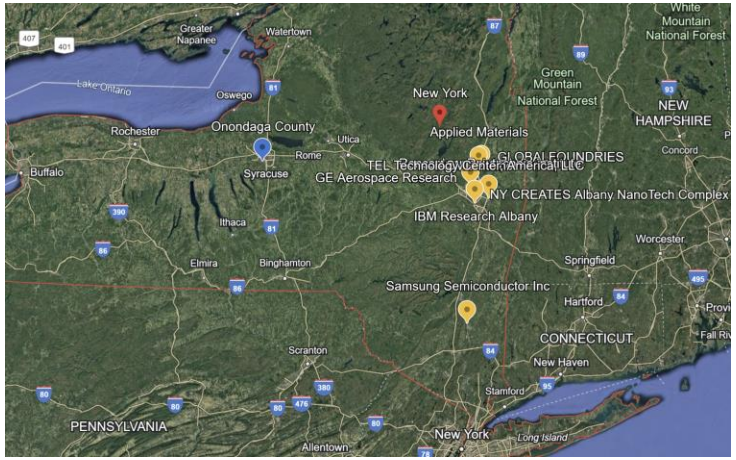


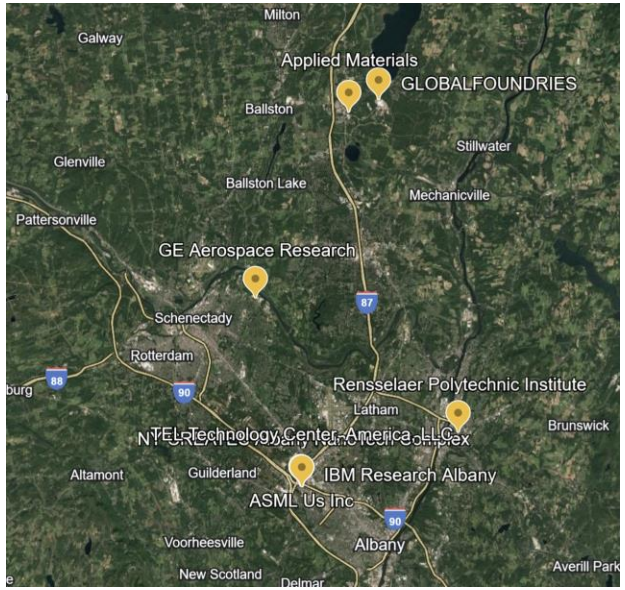
# Location

In New York State there are seven big semiconductor companies:

- IBM
- Micron Technologies
- Applied Materials
- Tokyo Electron
- ASML
- Global Foundries
- Samsung Semiconductor

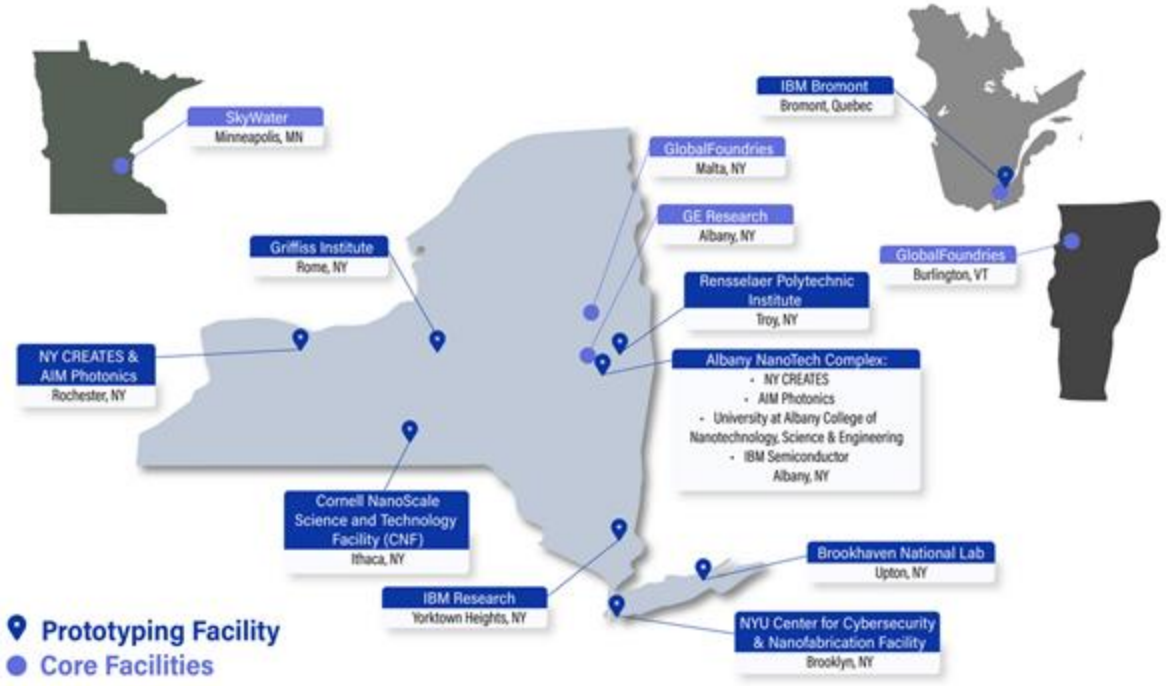
The red is less then 20 min away



# Location Cont. - NORDTECH: Northeastern Region Tech HUB

- Funded through the Chips and Science Act
- A part of the U.S. Microelectronics Commons, an initiative from the DOD to decrease dependence on foreign microelectronics supply chains
- Microelectronics supply chains are critical to the functioning of the entire U.S. economy.



# Why does EPS exist here and now?

It is the perfect time and place to become a semiconductor/hardware engineer!

# Programs

## Providing value to the student body

# Driving Accessibility

OPPORTUNITY

KNOWLEDGE

# Opportunity – Industry Tours

- **Albany Nanotech Complex**
  - Collaboration with the Center for Materials, Devices, and Integrated Systems (CMDIS)
  - A state-of-the-art campus that brings together industry leaders, academia, and international partners to develop next-generation chips and chip fabrication processes.
  - Major Companies: IBM, Applied Materials, Tokyo Electron, Wolfspeed
- **Global Foundries Malta Plant**
  - Collaboration with American Institute of Chemical Engineers @ RPI (AIChE)
  - A world-class semiconductor fabrication facility specializing in high-performance chips for a variety of applications, including consumer electronics, telecommunications, and automotive systems.

Dates will be announced on discord. Interest forms will be provided at the end of the presentation.

These are for EPS members on

# Opportunity – Off-Campus Conferences

- 2025 36th Annual SEMI Advanced Semiconductor Manufacturing Conference (May 5th – May 8th)
  - Albany, NY
- 36th Annual Electronic Packaging Symposium (Sept 3rd – Sept 4th)
  - Binghamton, NY
- Smaller seminars at the ANC also happen and we will provide transport to those.


# Opportunity – On-Campus Colloquiums

- This year's topic will be on Heterogeneous Integration
- There will be six speakers
- Currently working with the IEEE regional section to bring you a pool of companies to network with
- Environment to collaborate and learn about the latest tech advancements

# Knowledge – Seminar Series

- Officer-led presentation and discussion on topical issues in the microsystems field
- Learn content that will prepare you for interviews & enable meaningful conversation with industry engineers
- Excellent way to learn and engage with the field
- Sometimes, there is pizza!

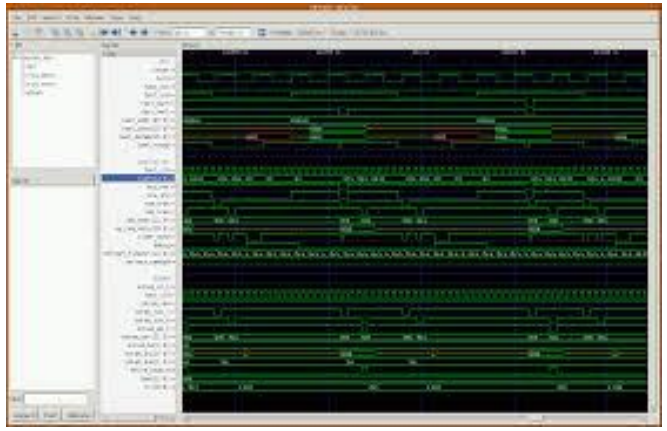

# Knowledge – Seminar Series

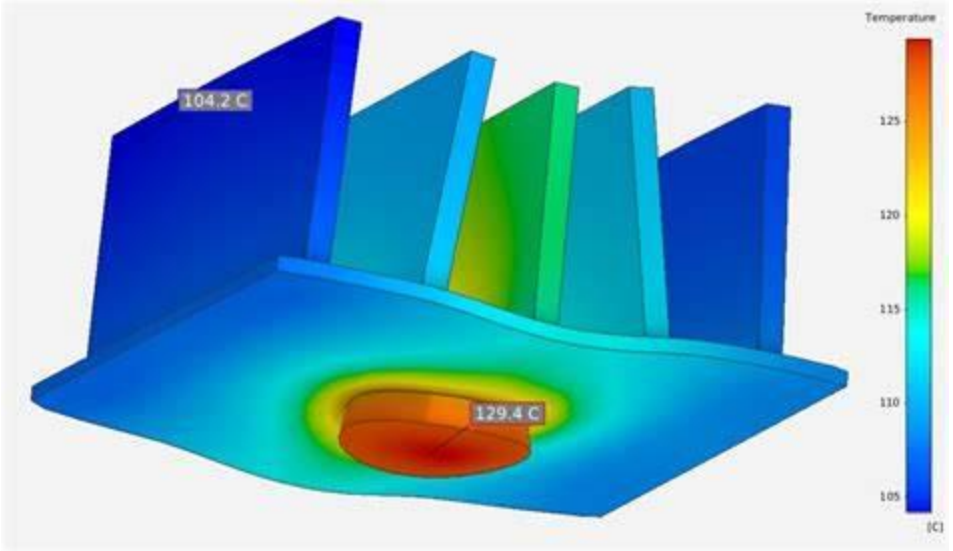
| Week | Name | Desciption |
|---|---|---|
| 1 | Open House / Info Session | An introduction for new and returning members, focusing on recruitment and providing an overview of the semiconductor industry |
| 2 | Officer-Led Presentation | Focus on manufacturing |
| 3 | Officer-Led Presentation | Focus on design |
| 4 | Distinguished Lecture Speaker | A distinguished speaker session with potential networking opportunities |

# Knowledge – Workshops

**Project-Based Learning:** Emphasizing hands-on experience, the program allows students to engage directly with real-world design challenges.

**Tool-Focused**: Focused on teaching well-known open-source or widely-used industry tools, the program provides students with a solid understanding of their functionality and practical applications.

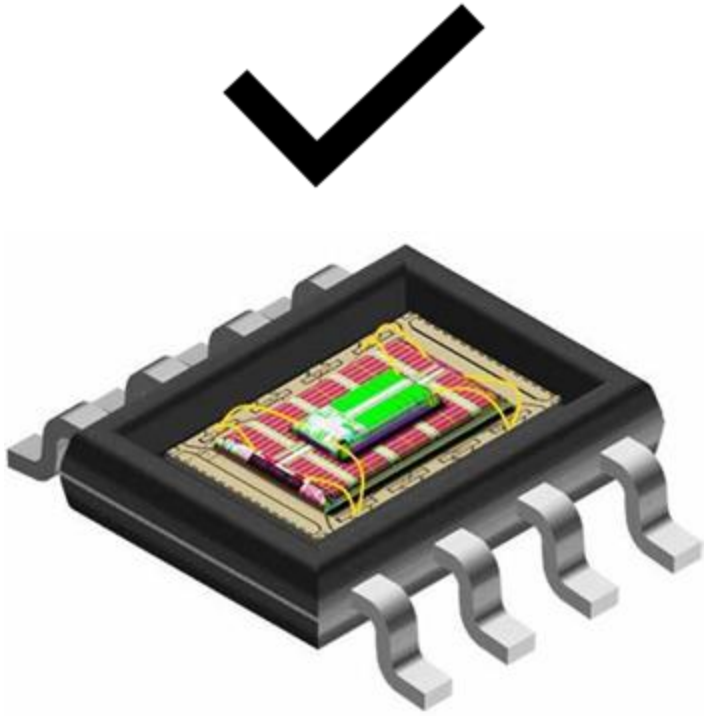




# Packaging Foundations

Let’s get technical

# What is this “packaging” you speak of?

# What is this “packaging” you speak of?

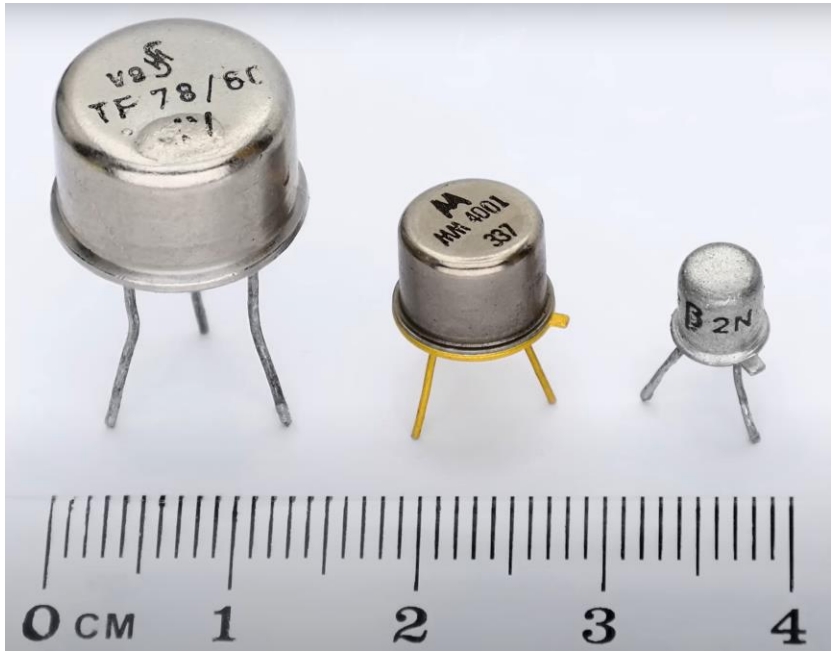
**Physical Enclosure of Chips**: IC packaging refers to the protective housing that encloses integrated circuits.

**Ensures Protection:**

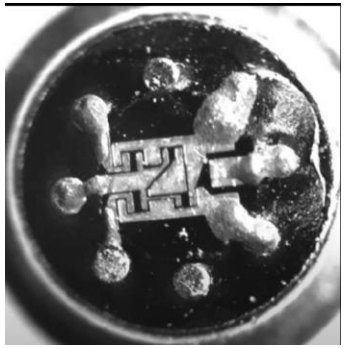
- **Mechanical**: Kinetic shocks, pressure, or vibrations can fracture a wafer.
- **Chemical**: Exposure to moisture or other chemicals can lead to corrosion of metal parts
- **Thermal**: Protects against thermal changes in the environment and ensures good heat dissipation

# How did we begin? (1970)

- In the beginning, only the military and aerospace companies used semiconductor devices.
  - Cost wasn't an issue
  - Total Reliability
- Die is hermetically sealed inside a can with the leads coming from the bottom.
  - Referred to as a transistor outline (TO) package
  - It is also referred to as a squid package
- Problem: Only supports a max of 8-10 leads.

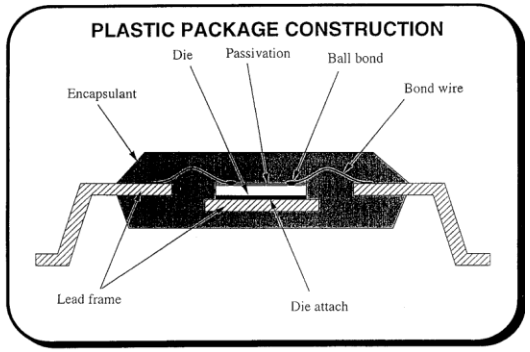






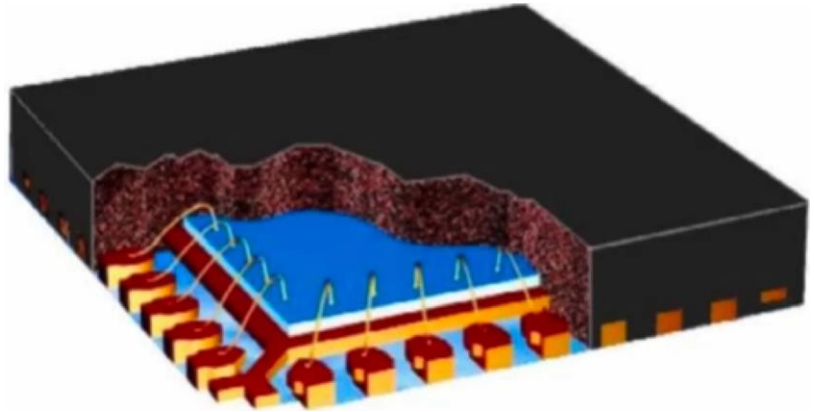
# How did we evolve? (1970-1990)

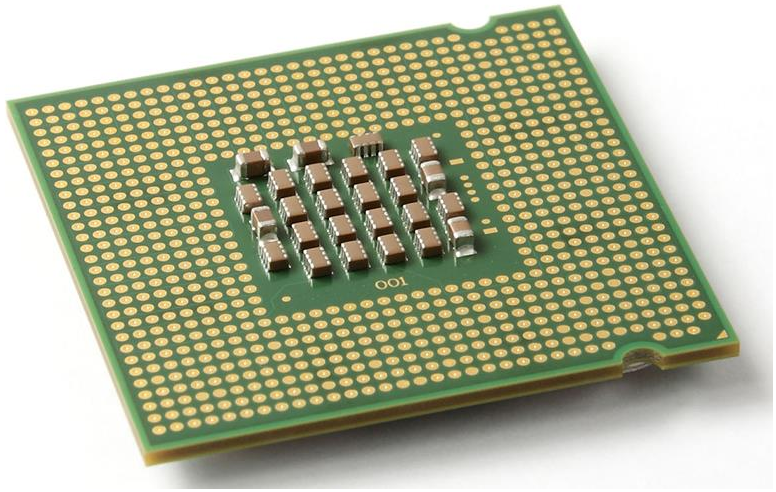
- Dual inline package became the new state of the art
- Plastic encapsulation became the new package manufacturing process
  - Primarily driven by, of course, Fairchild Semiconductor
- Had poor thermal and chemical characteristics but plastic is cheap and easy to do
  - Allowed us to easily outsource to Asia early on



# The start of VLSI (1990-2000)

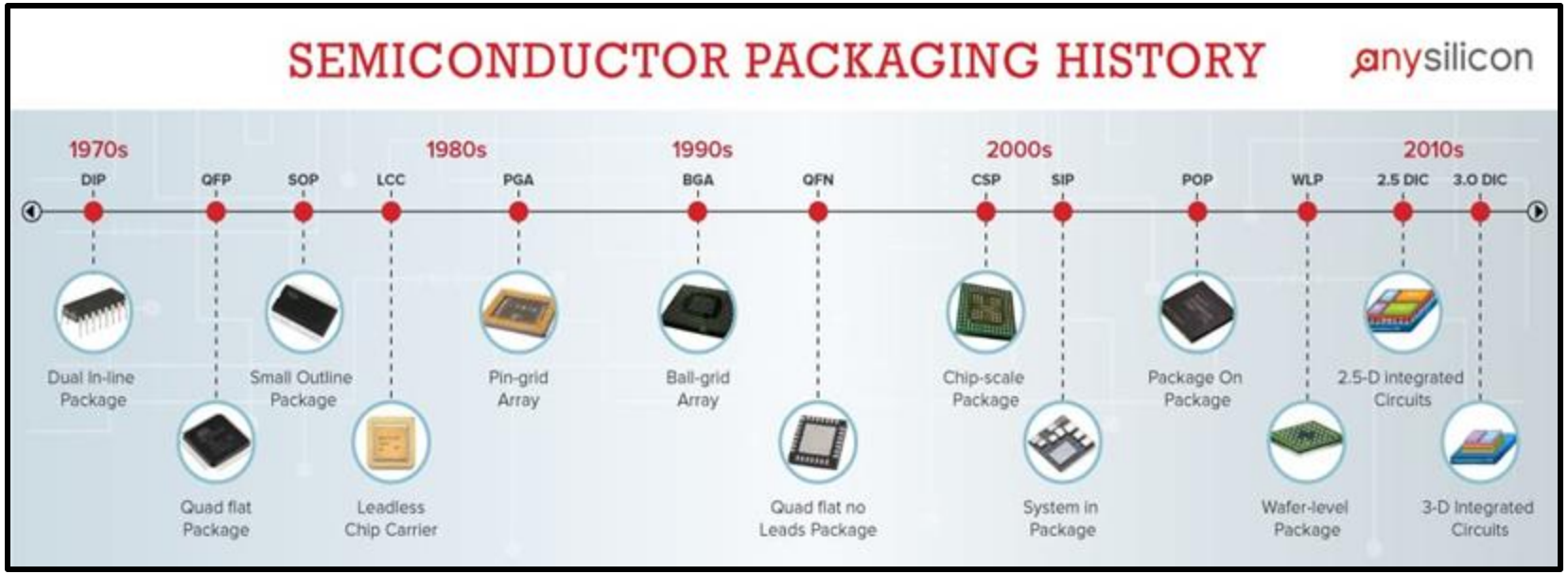
- Our chips are now starting to require more IO than ever.
  - DIPs are no longer feasible for larger or more complicated chips, as the packaging would become unbelievably large.
- Introduction of the quad flat package (QFP) that uses surface mounting technology (SMT) as opposed to through-hole mounting.
- Socketed packaging options also became available such as the LGA





# Packaging History

**NOT VERY EXCITING** → **VERY EXCITING**



# Integrated Circuit Innovations

## Moore's Law

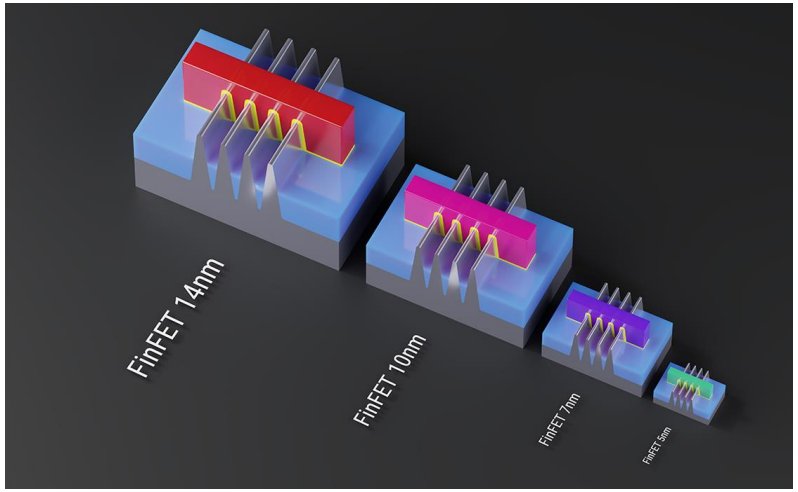
Continuous growth in transistor count

**1.4x Annual Performance Improvement for 40+ Years ≈ 10,000x**

## Dennard Scaling

Power per transistor shrinks as speed and density increase

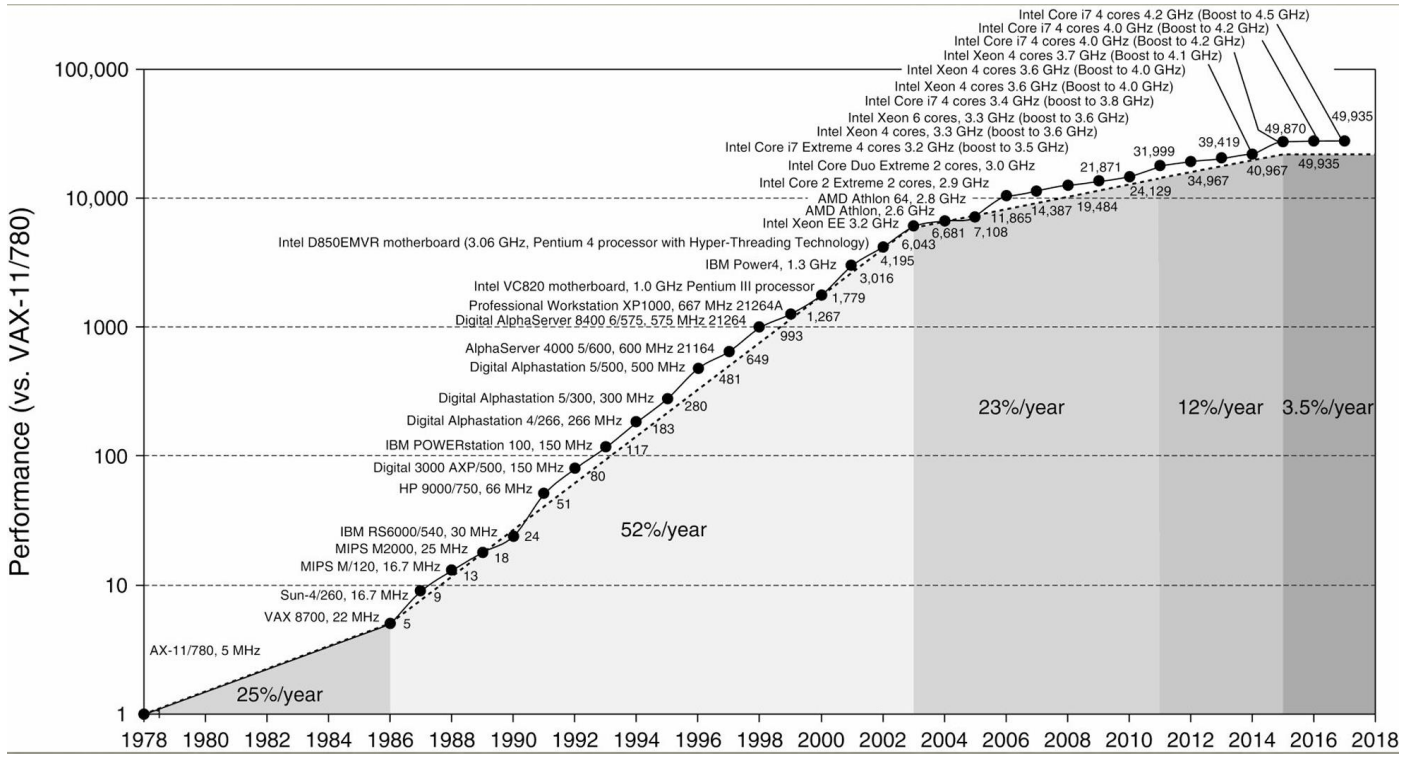
Energy expended per computation is reducing




## Clock Rate Evolution

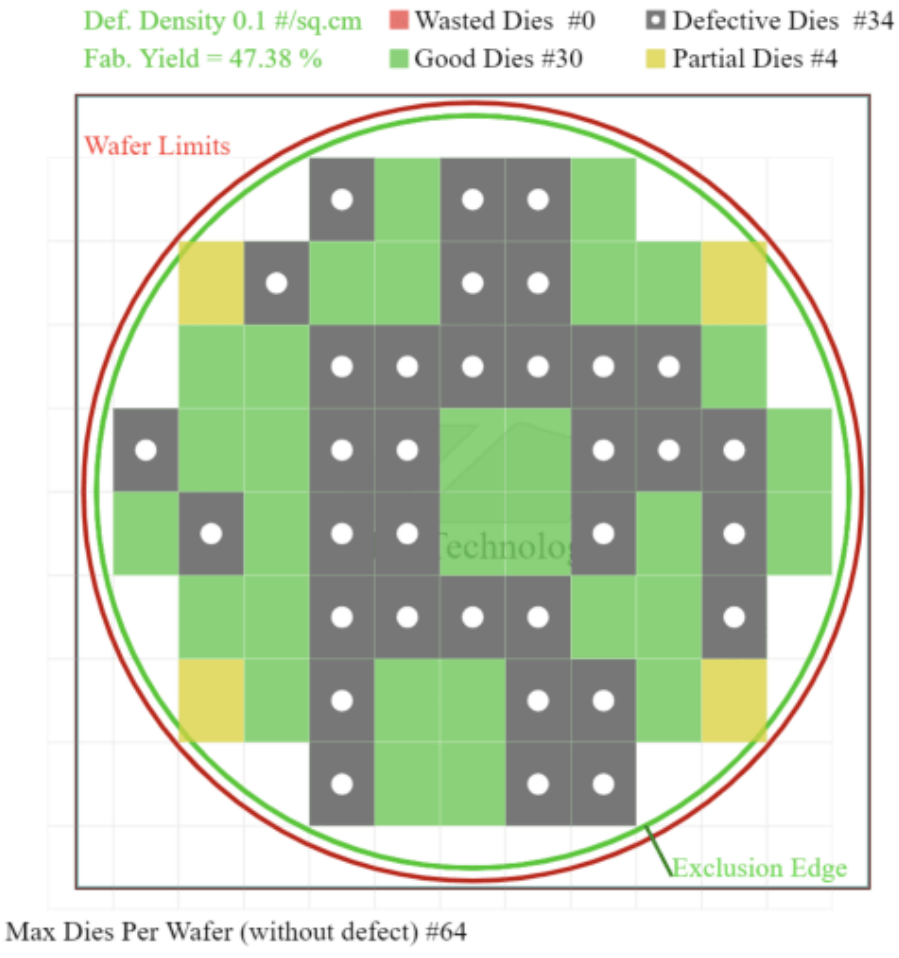
3 MHz to 4 GHz (improved through both technology and architecture)

# Uni-Processor Performance (Single Core)

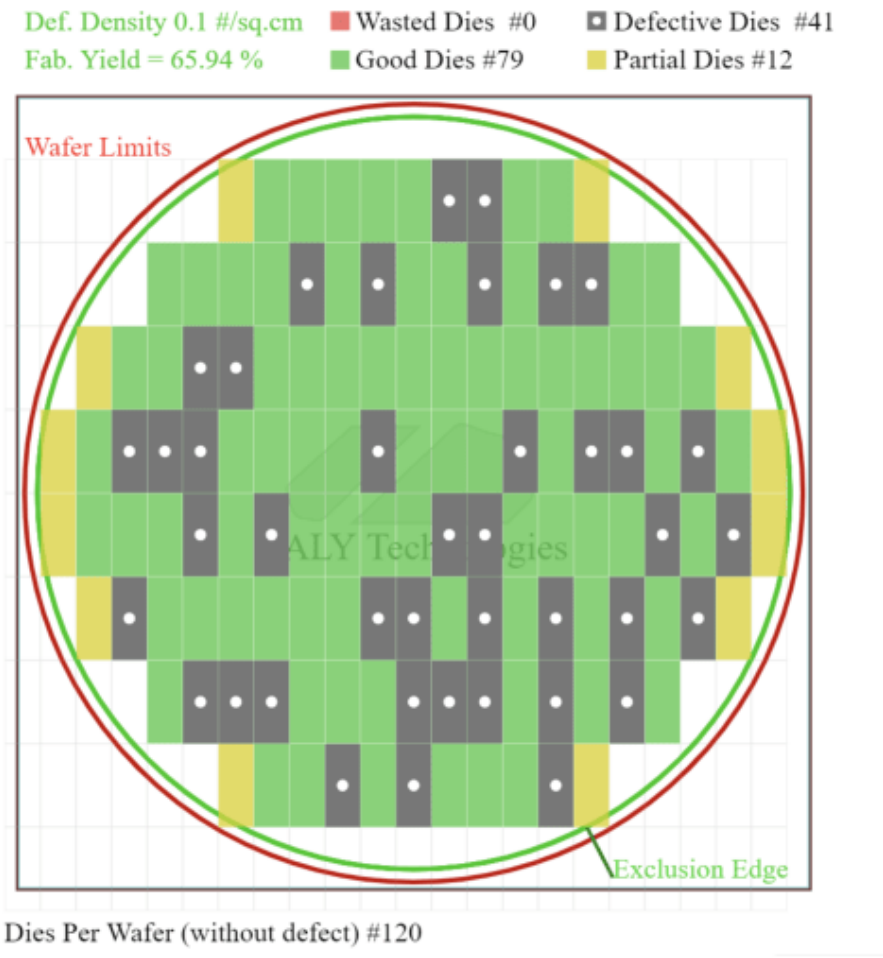



Plateauing of DRAM Density, and Computing Performance. Source: J Hennessy, ERI Conf July 2018

# Let’s make the wafer bigger!

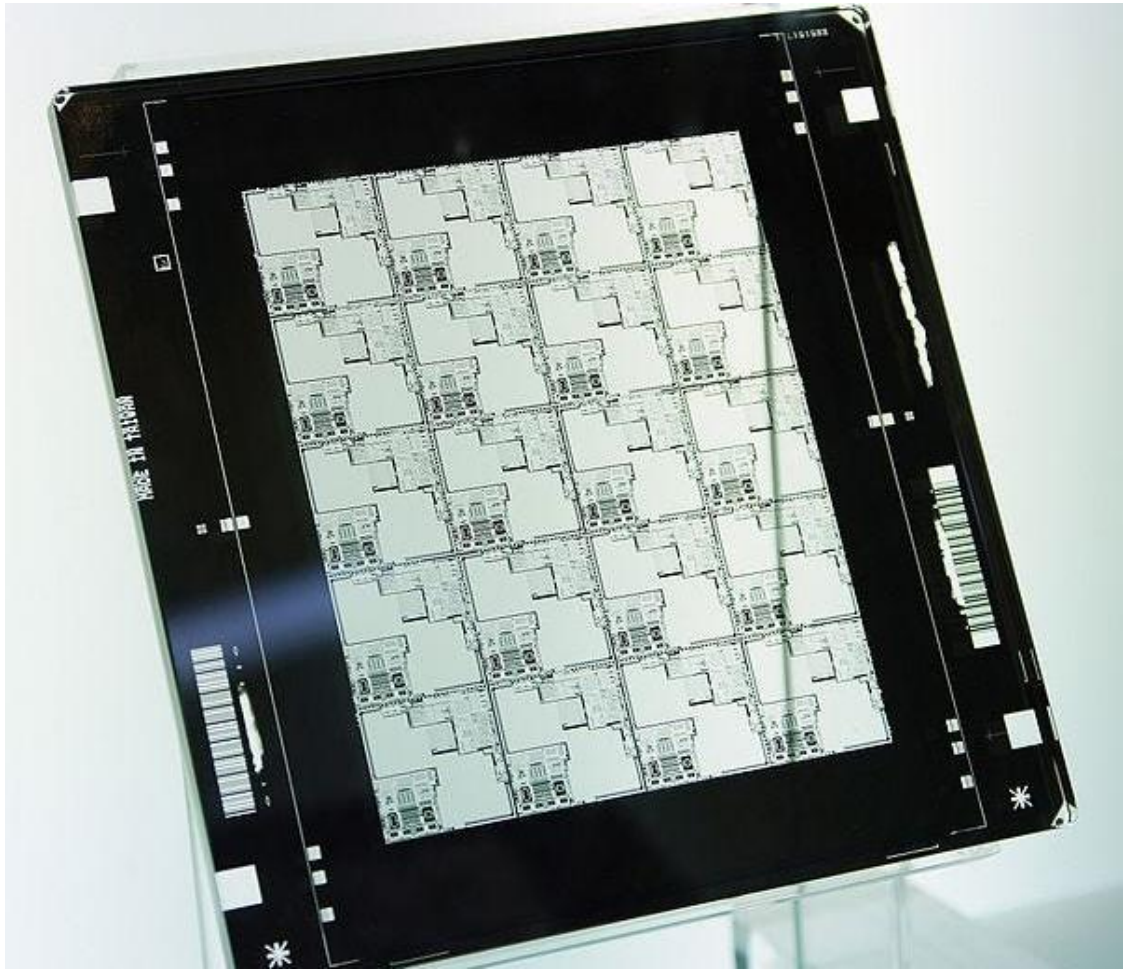



Max Dies Per Wafer (without defect) #64

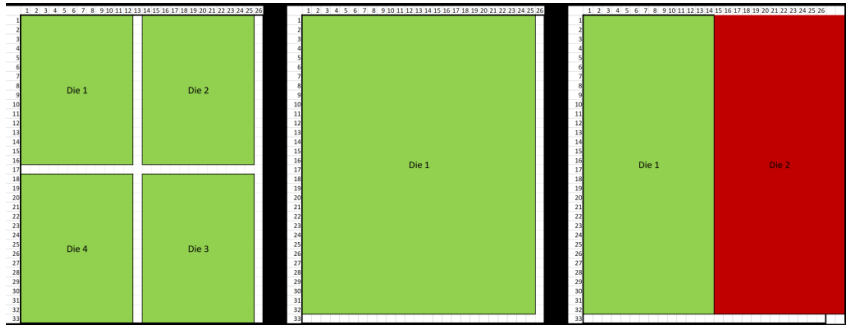



Max Dies Per Wafer (without defect) #120

# A more recent challenge

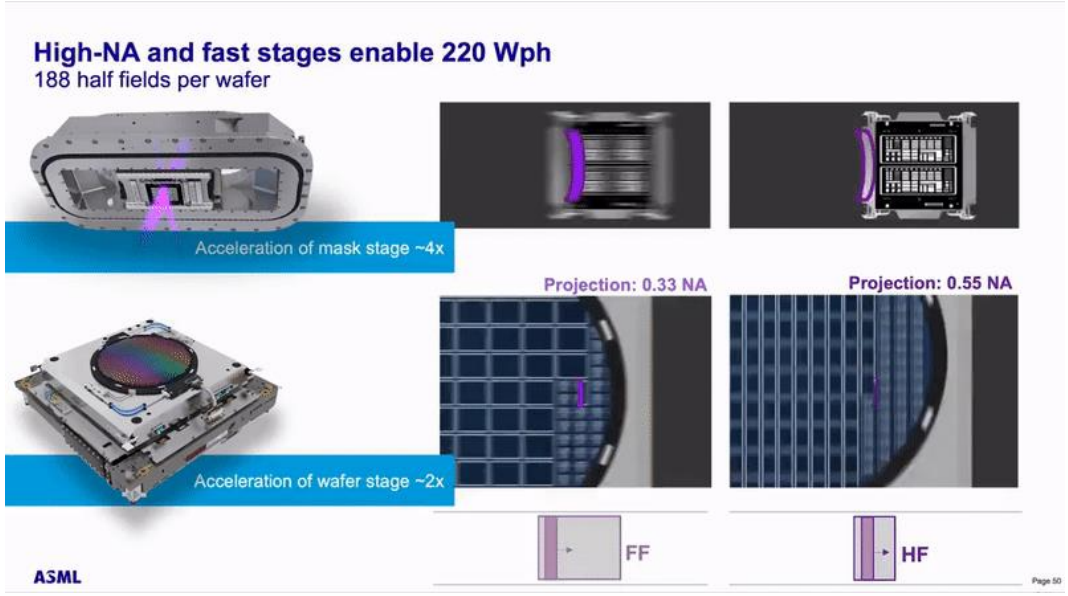


- A standard reticle is 104mm by 132mm
- Most designs do not perfectly line up with the 104 mm by 132 mm dimensions.
  - This results in a portion of the photomask not being exposed.
  - This is what reticle utilization is about.

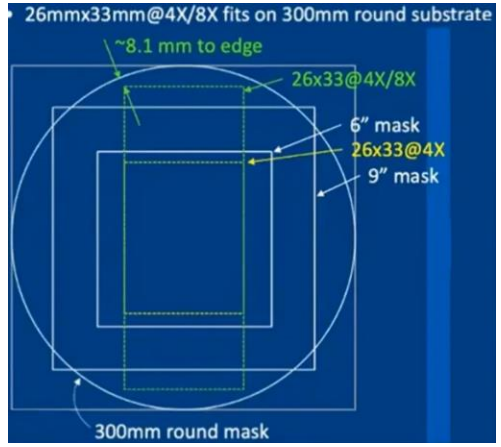


# A more recent challenge

- Why exactly is this problem?
  - Loss of reticle utilization
  - Misalignment chances increase
- This may not seem like a big deal, but lithography tool cost increases with time.



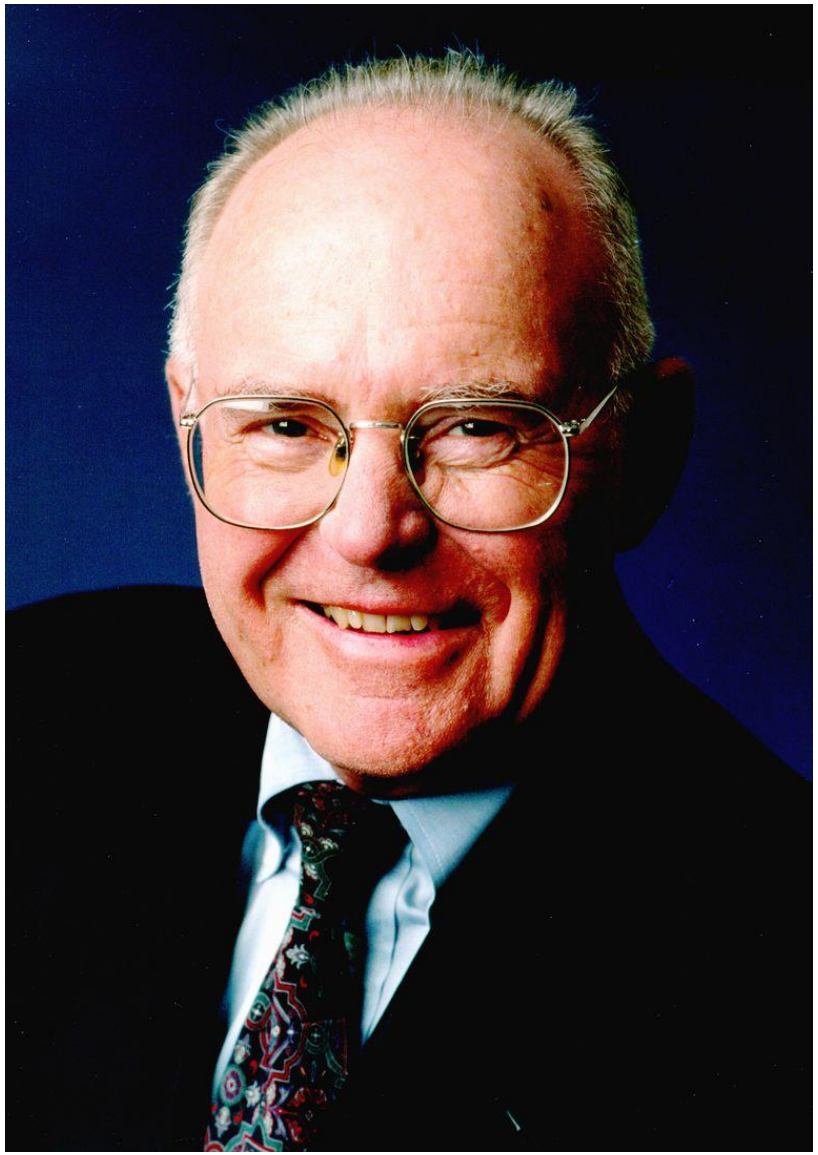

| Hypothetical 5nm Foundry Cost | | |
|---|---|---|
| Process Step/Consumable | Monolithic Cost | Chiplet MCM Cost |
| Wafer Substrate | $ 571 | $ 571 |
| Polish + Epitaxy | $ 211 | $ 211 |
| Ion Implant | $ 142 | $ 142 |
| Lithography Scanner | $ 2,899 | $ 5,072 |
| Photoresist + Coating | $ 553 | $ 553 |
| Etch and Cleaning | $ 2,372 | $ 2,372 |
| Deposition | $ 1,721 | $ 1,721 |
| Total | $ 8,468 | $ 10,641 |



# A Quote from Gordon Moore

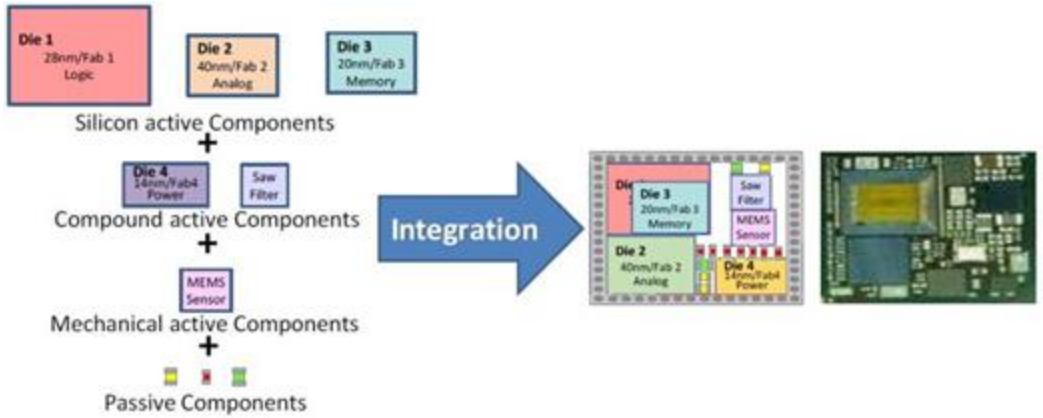
"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically."

Gordon Moore, 1965 (Founder of Moore's Law)



# What is Heterogeneous Integration?

- Involves combining different types of components, such as logic, memory, sensors, and more, into a single package.
- Provides a way to continue advancing performance when scaling traditional chips becomes too costly or inefficient.
- Enables integration of components built on different process nodes or with different materials.



# What is Heterogeneous Integration?

**2.5D Heterogeneous Integration:**

Uses an interposer (usually silicon) to connect multiple dies side by side.

Less complex than 3D in heat dissipation and design, but still allows for integrating different process technologies.

Commonly used in high-performance computing and graphics processors.

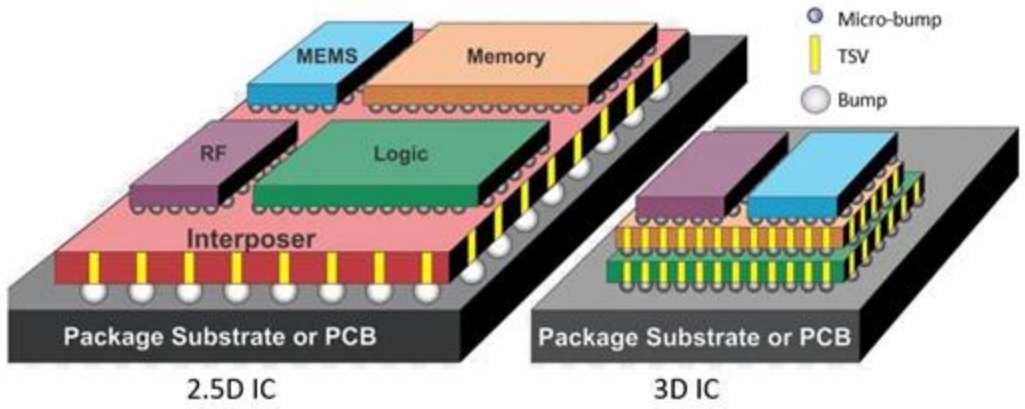
**3D Heterogeneous Integration:**

Involves stacking multiple dies vertically

More compact and allows for shorter signal paths, resulting in faster communication between components.

More challenging in terms of thermal management due to stacked layers, requiring advanced cooling solutions.

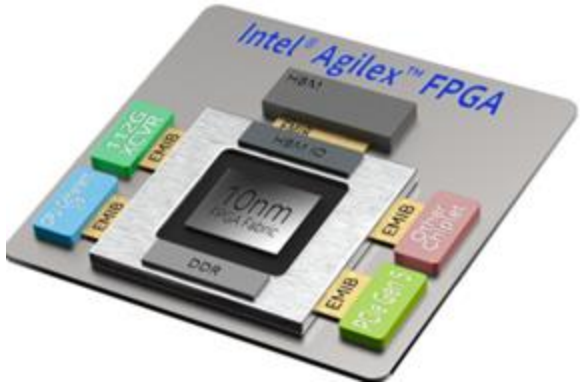
Used in memory stacking (e.g., High Bandwidth Memory or HBM) and advanced logic integration.

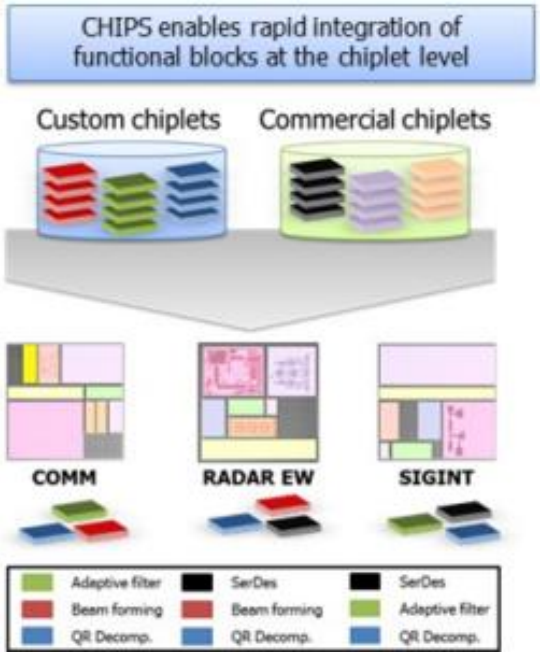


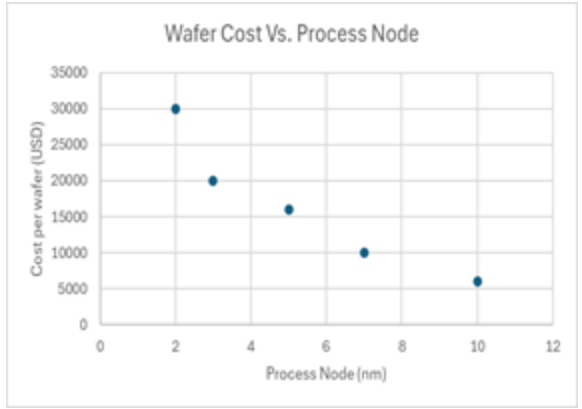
# Advantages of Heterogeneous Integration

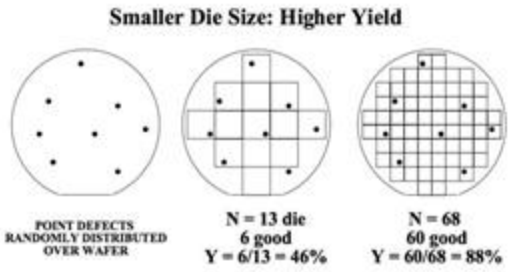
Innovative packaging solutions can improve:

- Time to market for new technology
- Yield/cost-effectiveness



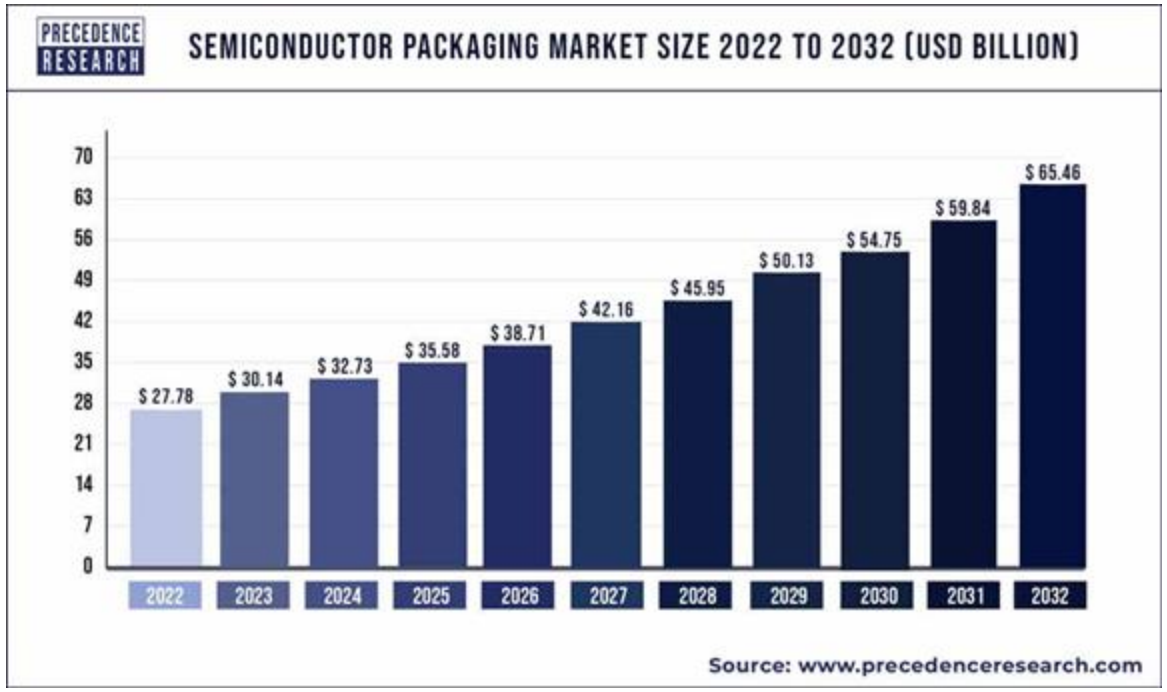



# Packaging Industry Impact

Impacts many industries in the economy:

- High-Performance Computing and Data Centers
- Medical, Health, and Wearables
- Autonomous Automotive
- Mobile
- Aerospace and Defense
- IoT




# Any questions?

# Get involved

Albany Nanotech Complex Tour Interest Form - Spring 2025

Officer Interest Form


Rensselaer
IEEE Student Branch


Rensselaer Polytechnic Institute
EPS

# Thank you!