Introduction

Week 1: Heterogeneous Integration Overview

Meet our EPS executive board

David King
Chair

- Class of ‘27
- Computer Systems and Electrical Eng.
- Clubs/Affiliations:
  - W2SZ

Alex Kim
Vice Chair

- Class of '24+2
- Mechanical Eng.
- Clubs/Affiliations:
  - Rensselaer Motorsport
  - RPI Esports
  - KSA
  - RSAS

Sangeeth Thayaaparan
Secretary

- Class of '26
- Electrical Eng.
- Clubs/Affiliations:
  - RPI Forge
  - RSEi

Jonas Kendra
Treasurer

- Class of '24 (M.S.)
- Mechanical Eng.
- Clubs/Affiliations:
  - Engineering Ambassadors
  - Rensselaer Motorsport
  - RPI Esports

WE NEED OFFICERS. WE WANT YOU!

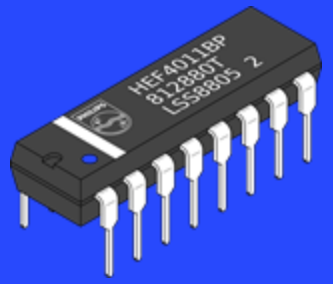
What will you learn today?

- ❑ What IEEE EPS is
- ❑ What IEEE EPS plans on doing at RPI

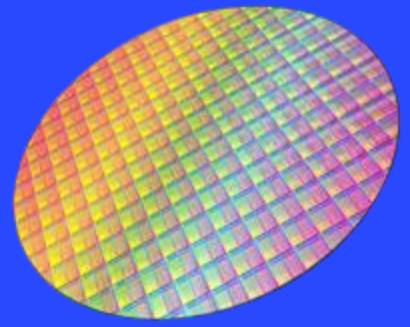
What is IEEE EPS? (Generally)

- A **chapter** of the Institute of Electronics and Electrical Engineers (IEEE) Electronic Packaging Society (EPS)
- We are a community for people interested in microsystems technology.
  - Hardware Design
    - ✓ ASIC
    - ✓ FPGA
    - ✓ Embedded
  - Integrated Circuit Manufacturing
    - ✓ Metrology
    - ✓ Process Engineering
    - ✓ Quality Assurance

What is IEEE EPS? (Specifically)



Packaging

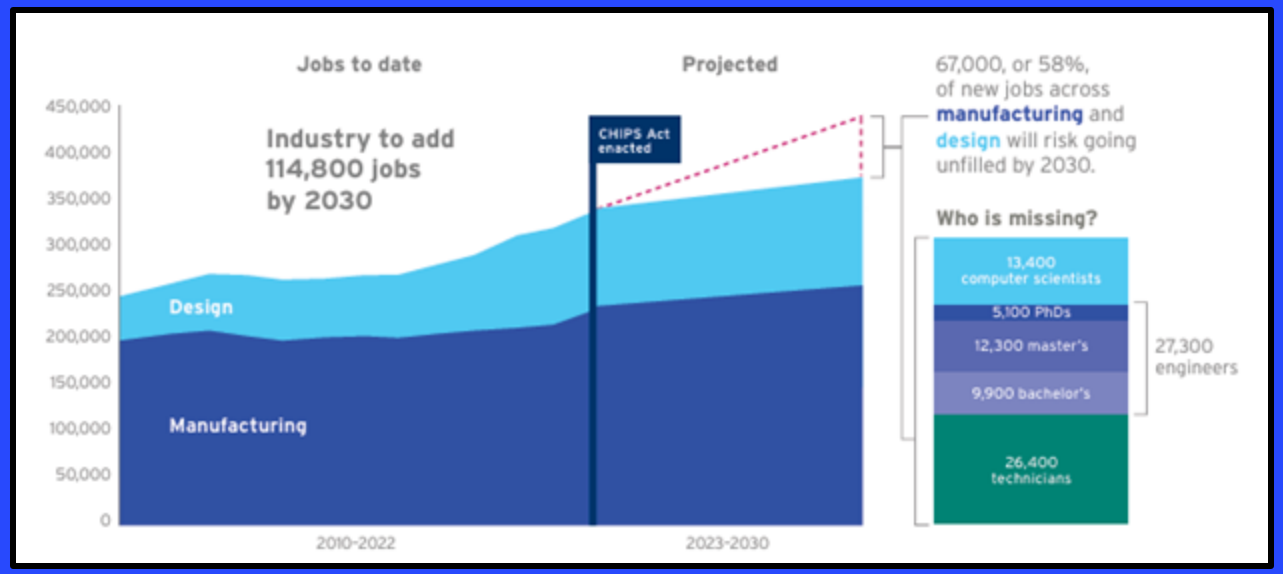


Manufacturing

- “The IEEE Electronics Packaging Society is the **leading international forum** for scientists and engineers engaged in the research, design and development of revolutionary advances in **microsystems packaging and manufacturing**.”
  - IEEE EPS Website – About Us

Why does EPS exist here and now?

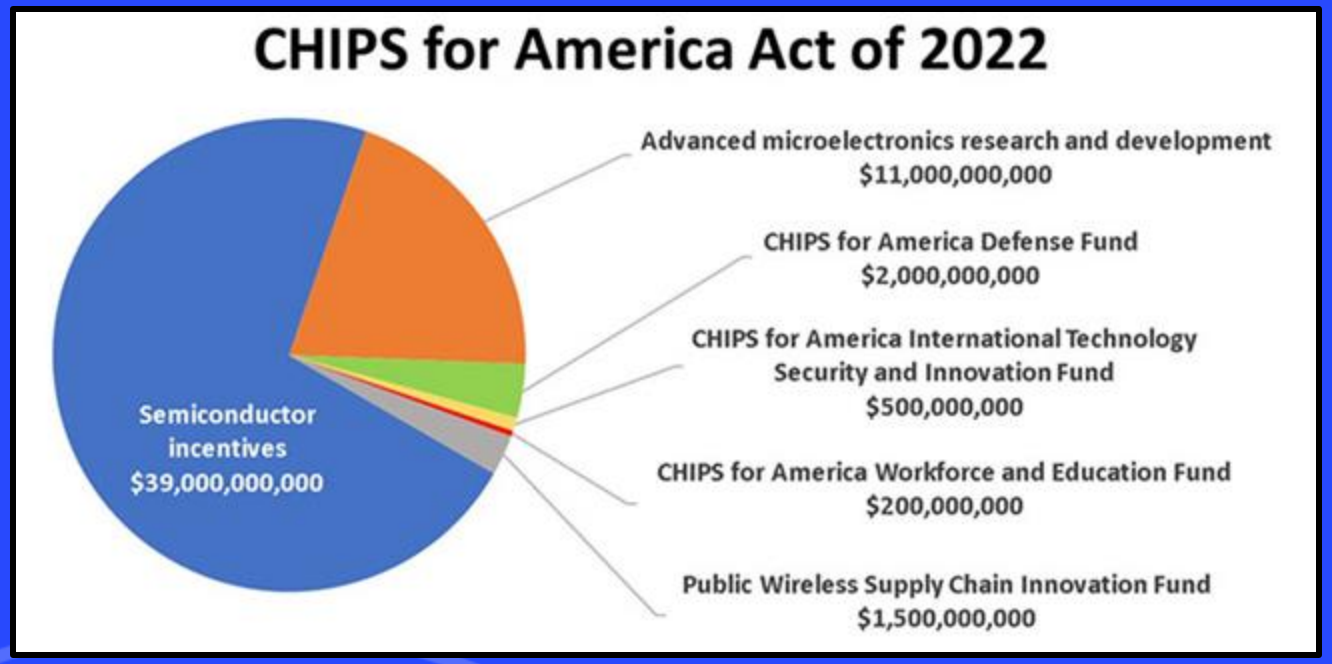
Talent Shortage



The Problem

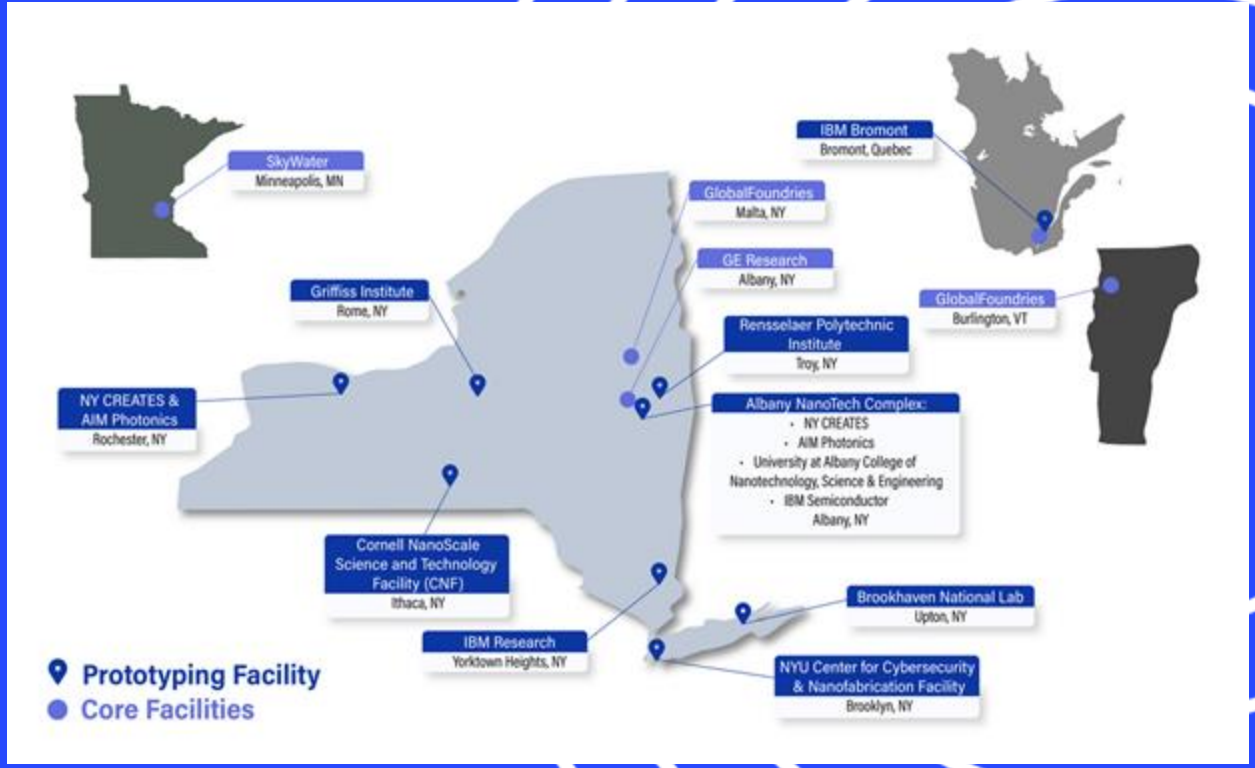
- **Significant Shortage:** The U.S. semiconductor industry faces a severe shortage of hardware designers, with an estimated shortfall of 59,000 to 146,000 workers, including engineers, by 2029
- **Increasing Demand:** The demand for semiconductor engineers is projected to grow significantly, with annual demand growth expected to peak around 2027. This will be challenging to meet given current training and education pipelines

CHIPS and Science Act



- Intended to increase economic competition with China, reducing dependence on foreign supply chains
- Funding distributed over ~1 decade
- Investment in education, infrastructure, and manufacturing
- Over 100,000 new jobs created between construction, manufacturing and research

NORDTECH Hub



NORDTech Hub

- Northeast Regional Defense Tech Hub
- **$ 9 billion** coming into NY (Clark,2023)

Major Companies near RPI

- IBM, Global Foundries, NanoTech, GE Research, Applied Materials, etc.
- **RPI** is at the **Center of Academic Research**

Why does EPS exist here and now?

Massive talent shortage

Government is going band for band with semiconductor industry

RPI is surrounded by NORDTECH

Why does EPS exist here and now?

It is the perfect time and place to become a semiconductor/hardware engineer!

Programs

How are we going to help you?

Networking Opportunities

Workforce Development

Networking Opportunities – Industry Tours

- **Albany Nanotech Complex**
  - A state-of-the-art campus that brings together industry leaders, academia and international partners to develop **next-generation chips and chip fabrication processes**.
  - Major Companies:
    - ✓ IBM, Applied Materials, Tokyo Electron, Wolfspeed
  - **Tour Date: October 2nd (Wednesday) 12:00 PM**
- More tours are coming in the future!

Networking Opportunities – Mini Colloquiums

- Mini-colloquium with **Industry Partners**
  - Currently working with IEEE regional section to bring you a pool of companies to network with
- Environment to collaborate and learn about the latest tech advancements

Event	Time (Tentative)
Semiconductor Manufacturing	November 6th, 2024
Mini Colloquium on Semiconductor Packaging	April 9th, 2025

Workforce Development – HIR Literature Review (Fall Semester)

- **Present**: Present various topics on microsystems technology relevant to the industry
- **Discuss**: Discuss presented topics to provide insight and understanding of topics.
- **Network**: Leverage newfound knowledge to network with researchers and industry professionals.

Date	Presentations (Tentative)
9/5/2024	**Overview**
9/12/2024	Wafer Processing Techniques
9/19/2024	Distinguished Presenter – Mark Poliks – Advanced Manufacturing
9/26/2024	Distinguished Speaker – Eric D. Perfecto – 2.5 D Manufacturing
10/3/2024	Transistor Scaling
10/10/2024	Thermals
10/17/2024	Metrology
10/24/2024	Materials
10/31/2024	Distinguished Speaker – Dongkai Shangguan - Materials
11/7/2024	Distinguished Speaker – Rohit Sharma – 2D Materials-Based Nanoelectronics
11/14/2024	FEOL
11/21/2024	Distinguished Speaker – Chris Bower – Elastomer Stamp Micro Transfer Printing
12/5/2024	BEOL
12/12/2024	Distinguished Speaker – Subu Iyer – 3d Interposer and Wafer Scale Integration and Stacking
12/19/2024	Reliability/testing
1/9/2025	Distinguished Speaker – Mudasir Ahmad - Advanced Reliability (Thermochemical, Mechanical Shock)

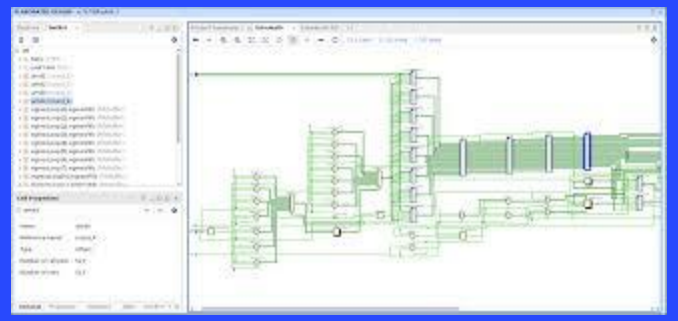
NOTE: Can change due to availability and interest

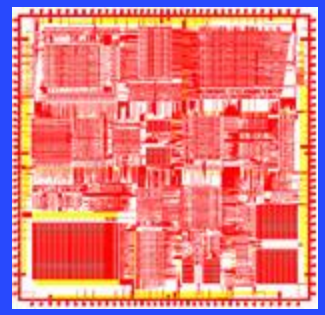
Workforce Development – Hardware Horizons (Spring Semester)

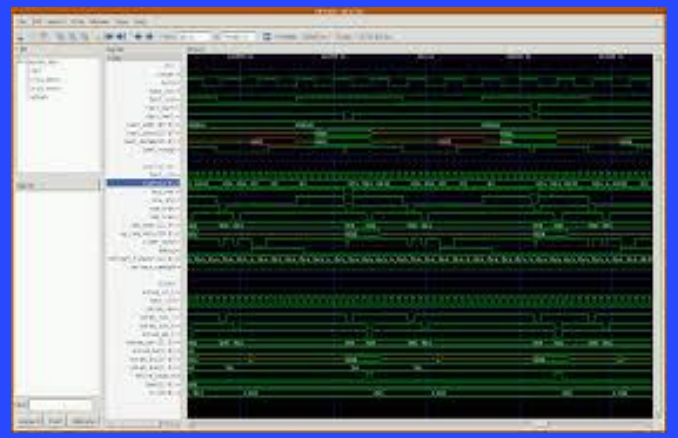
Learn to design a CPU!

Comprehensive Skill Development: A program focused on building essential hardware design skills using an open-source hardware design toolset.

Project-Based Learning: Emphasizing hands-on experience, the program allows students to engage directly with real-world design challenges.



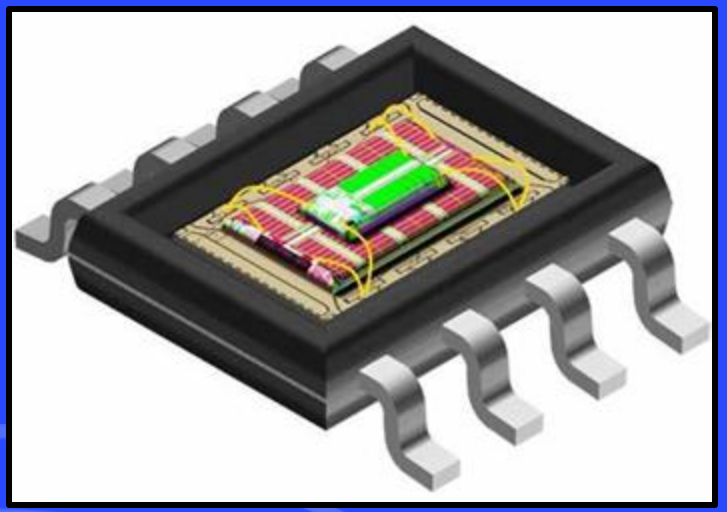




HIR Literature Review

Let's get technical

What is this “packaging” you speak of?

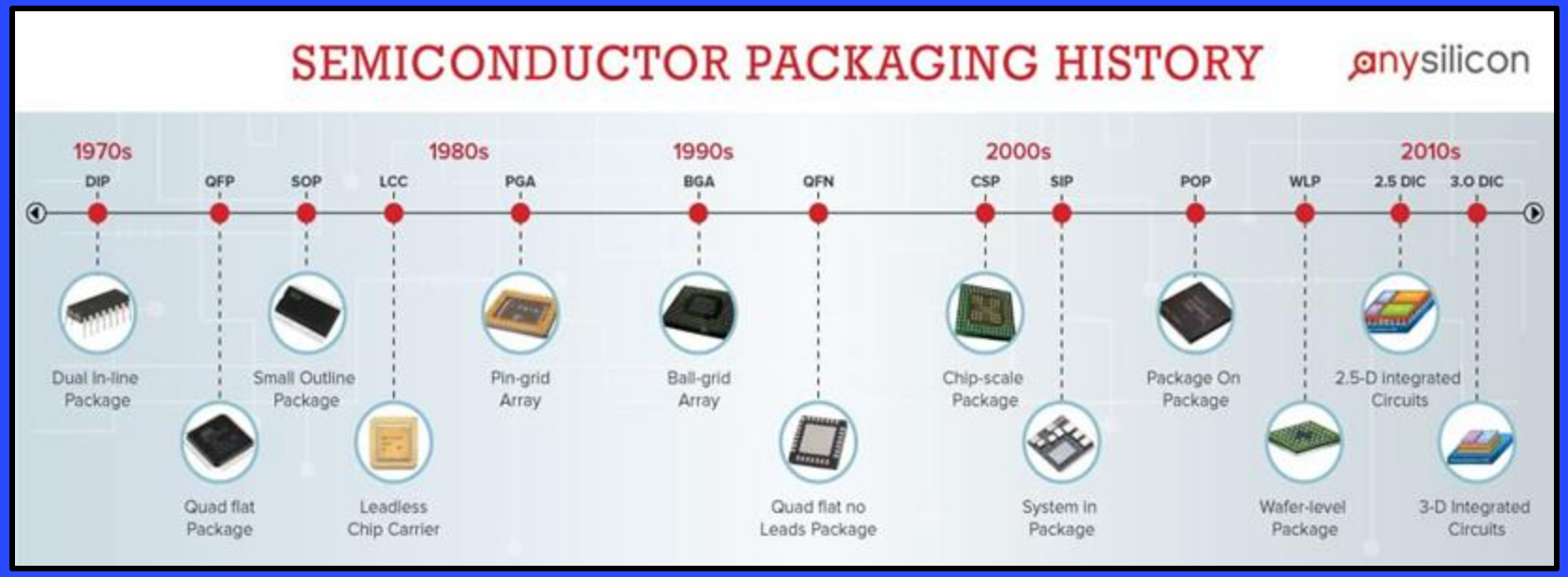


What is this “packaging” you speak of?

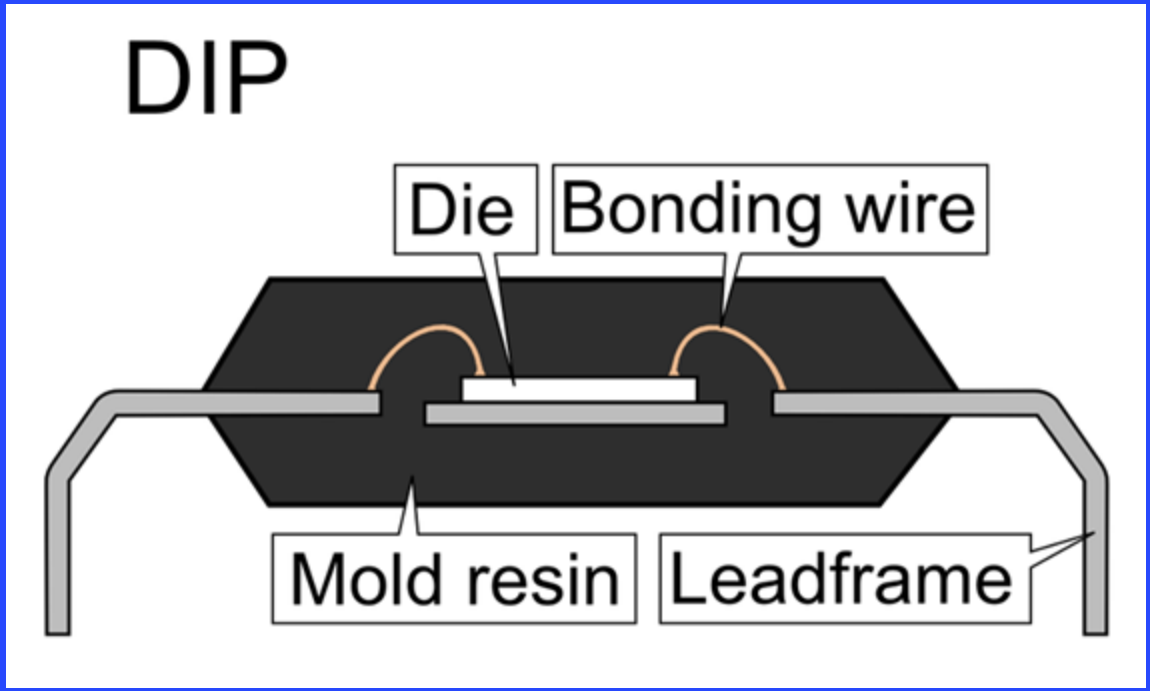
- **Physical Enclosure of Chips**: IC packaging refers to the protective housing that encloses integrated circuits.
- **Ensures Protection:**
  - **Thermal**: Different CTE can cause mechanical strain
  - **Mechanical**: Kinetic shocks, pressure, or vibrations, can fracture a wafer.
  - **Chemical**: Exposure to moisture or other chemicals can lead to corrosion of metal parts

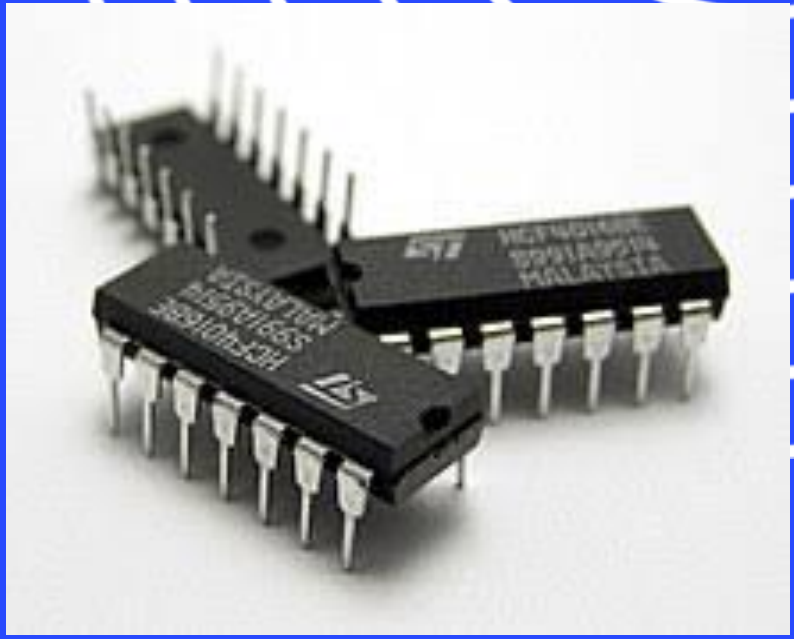
Packaging History

NOT VERY EXCITING → **VERY EXCITING**

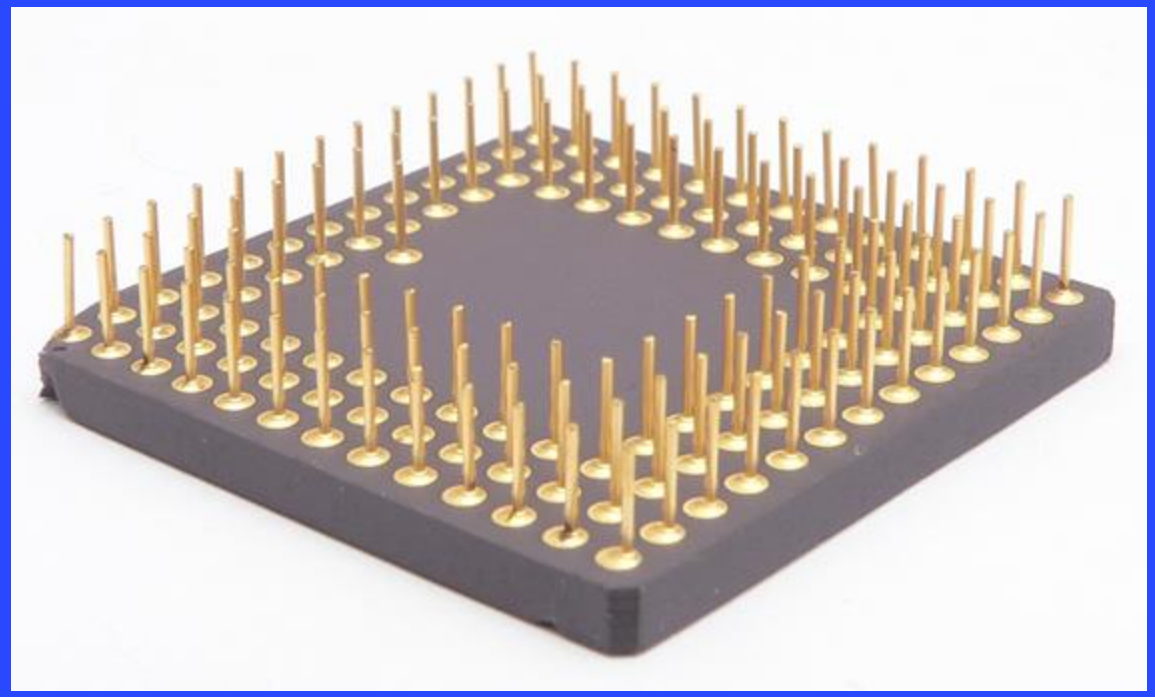


How did we begin?





How did we evolve?



Bigger = Better?

(This isn't Texas)

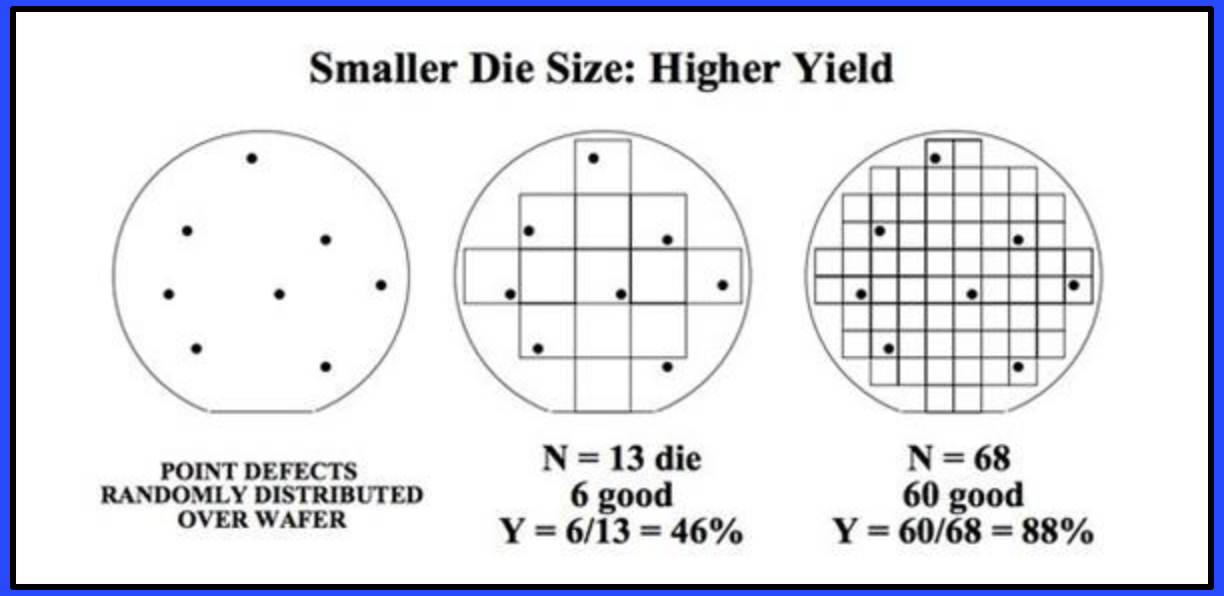
Bigger chips mean...

- More performance (YES)
- More interconnects (Hmm)
- More power (Not too hot...)
- More expensive (No thanks...)

Is smaller better th

- It is becoming increasingly expensive to manufacture chips on smaller process nodes
- Why?
  - Increased fabrication complexity
  - Yield challenges
  - Diminishing Performance and Efficiency gains

We have a solution

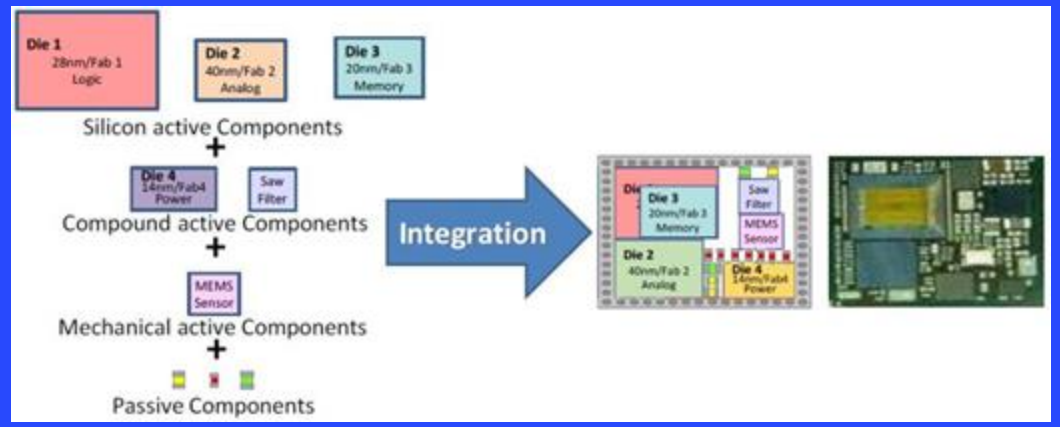


- ❑ Manufacturers incur costs in **tens of thousands of dollars** to produce a single wafer (300mm, or 12” diameter)
- ❑ While larger chips may be more effective at accomplishing a task, they are economically unviable
  - ➢ Random sources of error propagate across surface
  - ➢ Lower yield due to random error, leading to higher costs
    - ✓ (Exponential failure relationship w/increased die size)

The Solution: Heterogeneous Integration

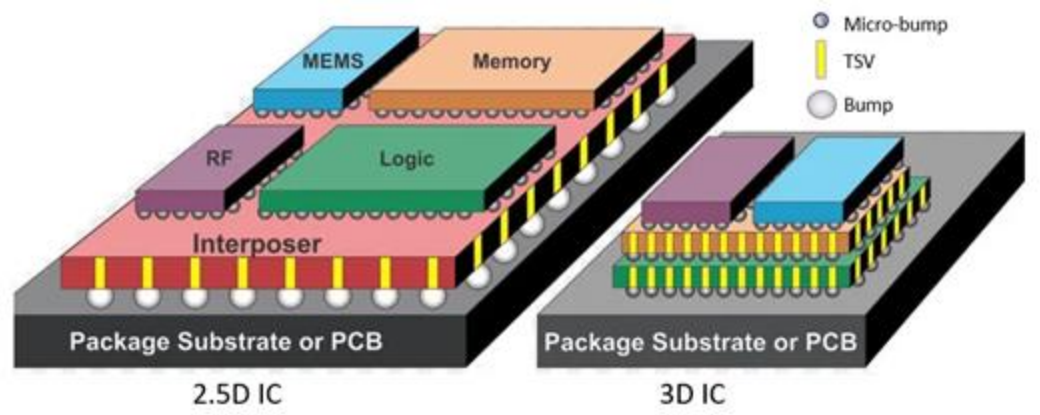
- “It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.“
  - Gordon Moore, 1965 (Founder of Moore’s Law)

What is Heterogeneous Integration?



- Involves combining different types of components, such as logic, memory, sensors, and more, into a single package.
- Provides a way to continue advancing performance when scaling traditional chips becomes too costly or inefficient.
- Enables integration of components built on different process nodes or with different materials.

What is Heterogeneous Integration?



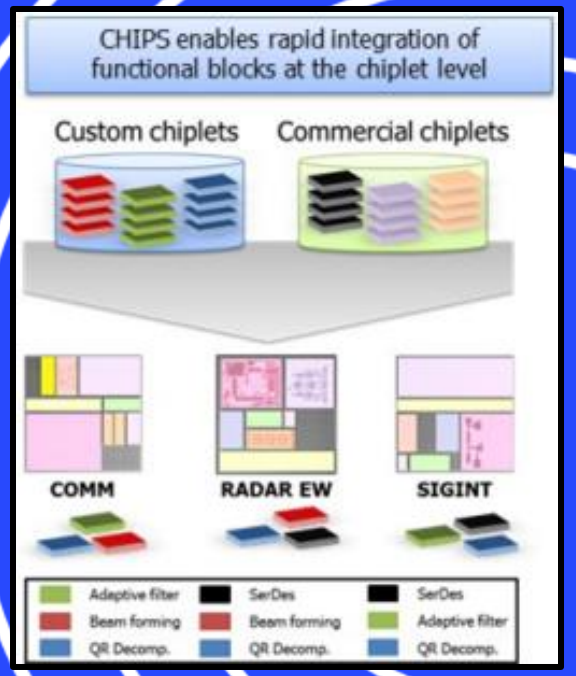
❑ **2.5D Heterogeneous Integration:**

- Uses an interposer (usually silicon) to connect multiple dies side by side.
- Less complex than 3D in terms of heat dissipation and design, but still allows for integration of different process technologies.
- Commonly used in high-performance computing and graphics processors.

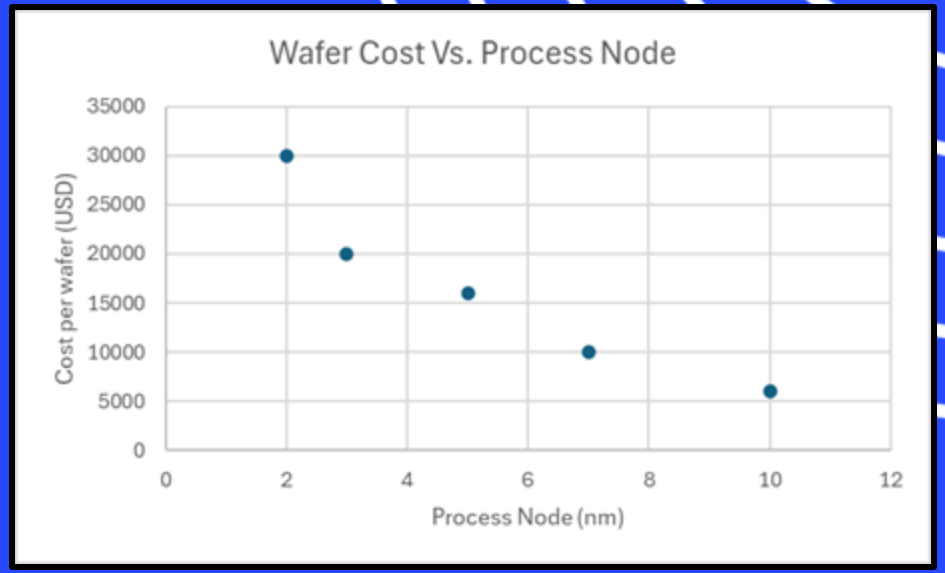
❑ **3D Heterogeneous Integration:**

- Involves stacking multiple dies vertically
- More compact and allows for shorter signal paths, resulting in faster communication between components.
- More challenging in terms of thermal management due to stacked layers, requiring advanced cooling solutions.
- Used in memory stacking (e.g., High Bandwidth Memory or HBM) and advanced logic integration.

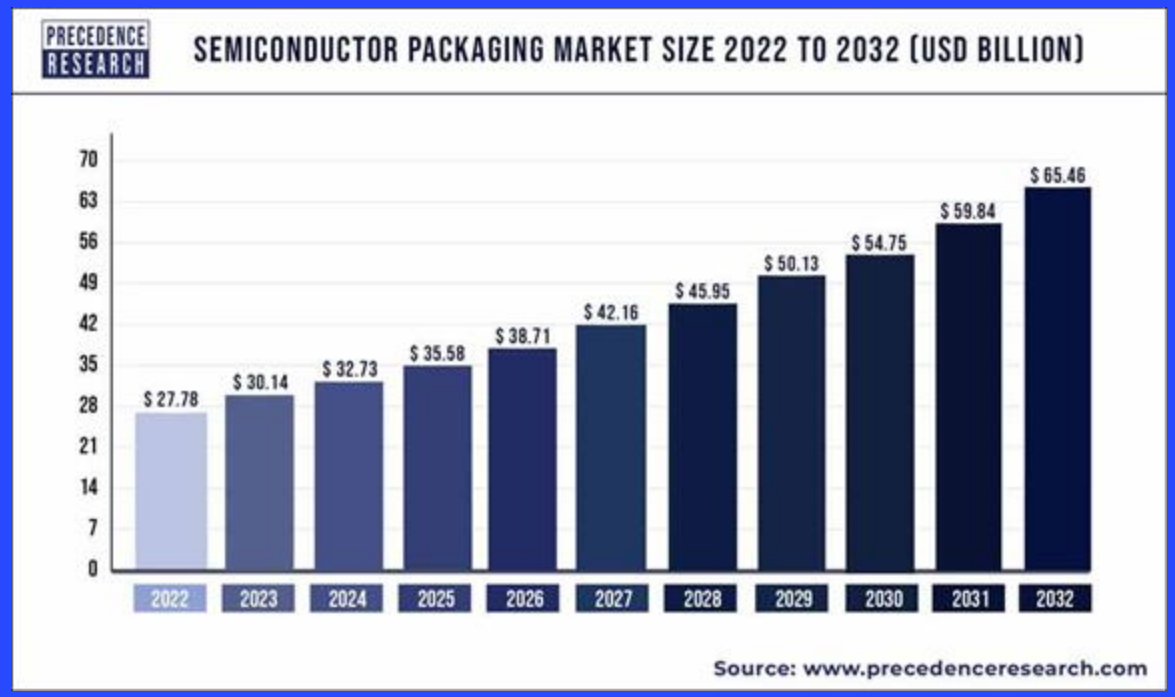
Advantages of Heterogeneous Integration



- Innovative packaging solutions can improve:
  - Time to market for new technology
  - Improve yield / cost effectiveness
  - Improved clock speeds



Packaging Market – Growth Projections



Heterogeneous Integration – Markets Impacted

- High Performance Computing and Data Centers
- Medical, Health and Wearables
- Autonomous Automotive
- Mobile
- Aerospace and Defense
- IoT

Why should you care?

Wow This is fantastic Jonas

I don't care about no "corporate bottom line"

Packaging Impact

Solve multi-million dollar problems with large impact across various industries

See your work in use everywhere you go

Packaging Technical Areas

Test

Supply Chain

Manufacturing

Process

Design

Materials Research

Device Research

Any questions?

GET INVOLVED

ALBANY NANOTECH
TOUR INTEREST FORM

IEEE EPS OFFICER
INTEREST FORM

LINKTREE
(Discord, Website, Insta)

Additional Resources

- **Asianometry: Brief History of Semiconductor Packaging**
  - https://youtu.be/nNpuiJitKwk?si=RfvOTg5pQ2dn27bj
- IBM Research: “What are Chiplets?”
  - https://research.ibm.com/blog/what-are-computer-chiplets
- AMD Chiplet Successes/Future of Het. Int:
  - https://ieeexplore.ieee.org/document/9063103
- IEEE EPS Cite: Executive Summary:
  - https://eps.ieee.org/images/files/HIR_2021/ch01_overview.pdf