



Rensselaer
IEEE Student Branch



**IEEE
ELECTRONICS
PACKAGING
SOCIETY**



Lithography & Patterning

Evan Chen

GBM Attendance



General Updates (1 of 2)

- Distinguished Lecturer Seminar Next Week!
 - Dr. Mukta Farooq (IBM)
 - Heterogeneous Integration and Advanced Packaging for The Chiplet Era
 - Next Monday, October 5th @ 6:00 PM
 - Walker 6113
- Another Distinguished Lecturer!
 - Chris Berry (IBM)
 - Reliability topics for the miniaturization and qualification of Advanced Silicon CMOS Technologies
 - November 2nd
 - More Details to Come!



General Updates (2 of 2)

- PCB Workshop(s!)
 - Sponsored by IEEE EPS/EDS, RPI EHC, and Rensselaer Spaceflight Society
 - ~~PCB Design Basics: 9/25~~
 - Soldering Workshop: 10/7
 - PCB Manufacturing: 10/8-9
- Semiconductor Summit!!!
 - This Wednesday 9/30 from 11am - 5pm



PCB Design Workshop 03

Soldering Workshop

Learn how to solder and assemble your PCB:

- Through-hole soldering
- Best practices for a clean solder
- Practice and refine your skills

Check out the rest of our workshops!

PCB Design Basics	9/25
Soldering Workshop	10/7
PCB Manufacturing	10/8-10/9

RSVP

QR Code

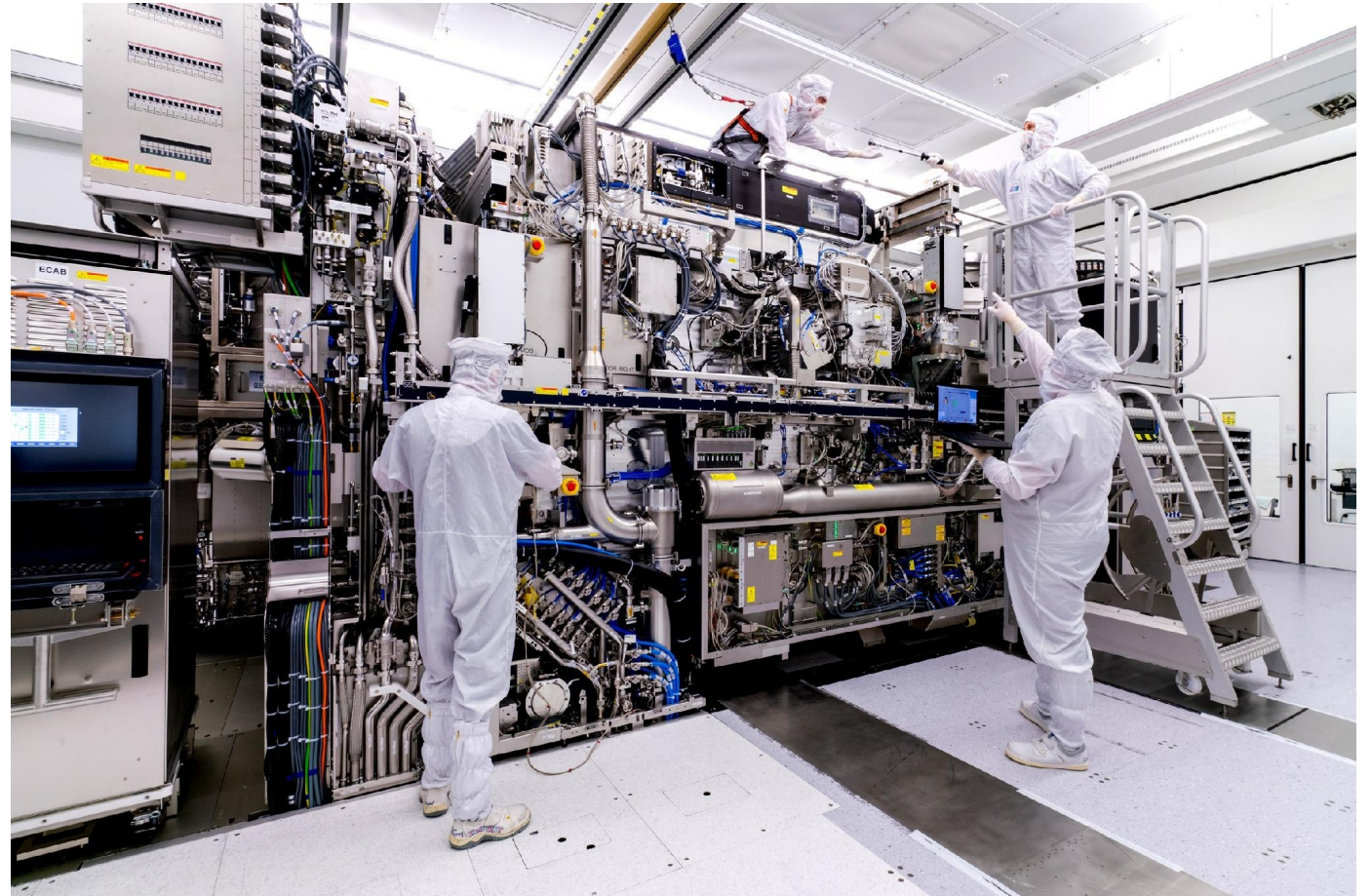
wednesday 4:00-6:00 PM

10.7.26 mercer-x lab

TD: 10/8 blounh@rpi.edu

Overview

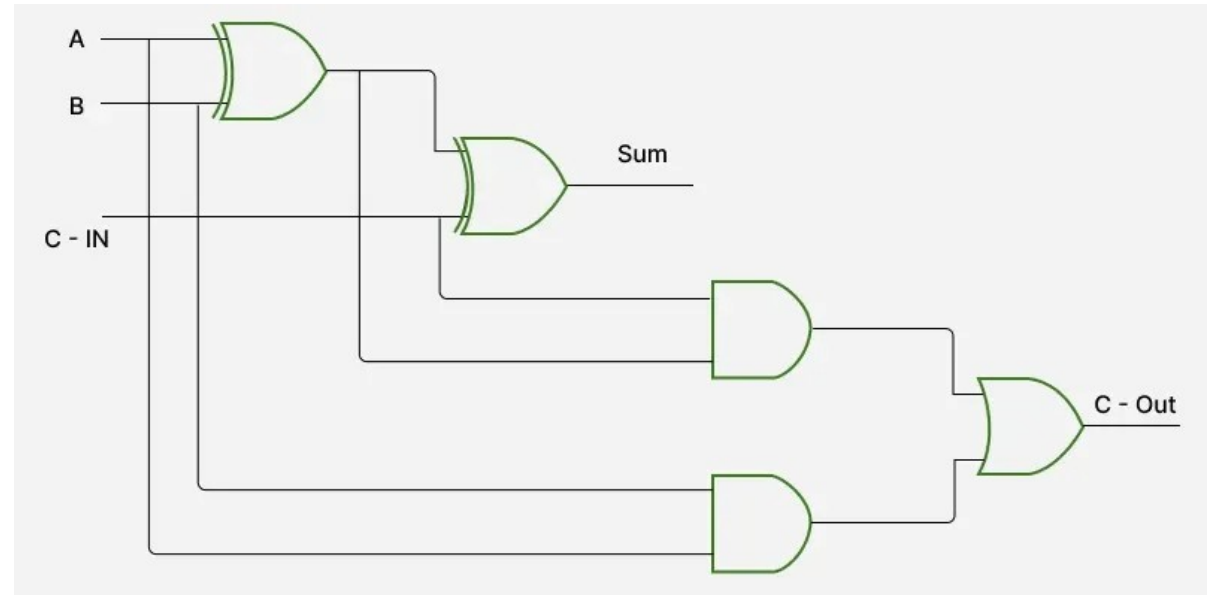
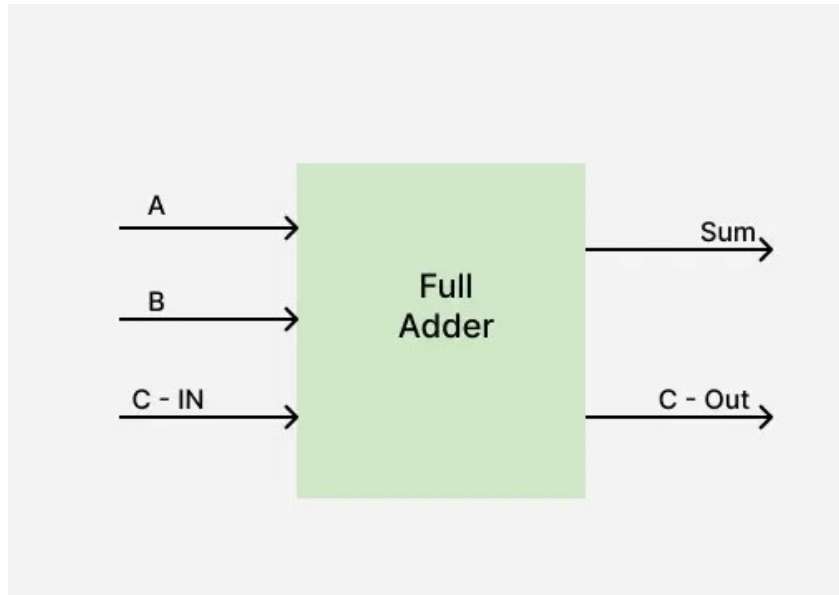
- Motivation for Lithography
- History of Development
- Resolution Enhancement Techniques
- Lithography Types & Settings



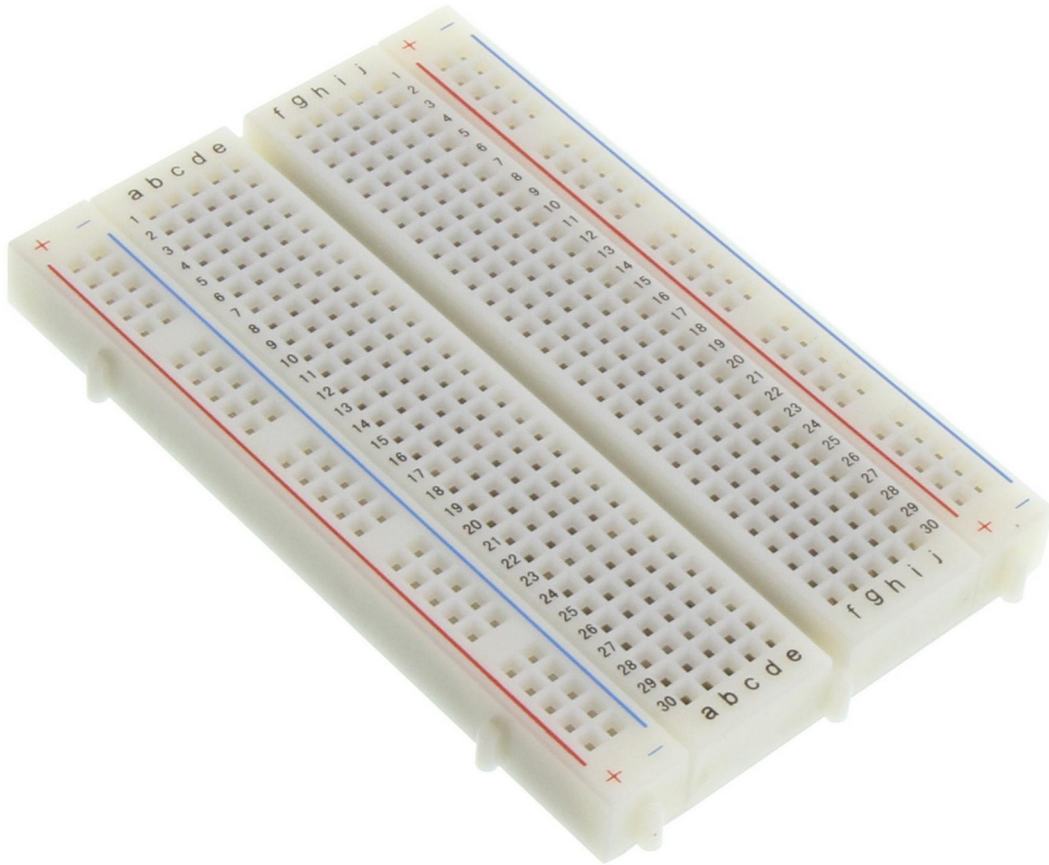
What is Lithography? Why is Lithography? (How is Lithography?)

Let's say you wanted to
build a full adder out of
transistors

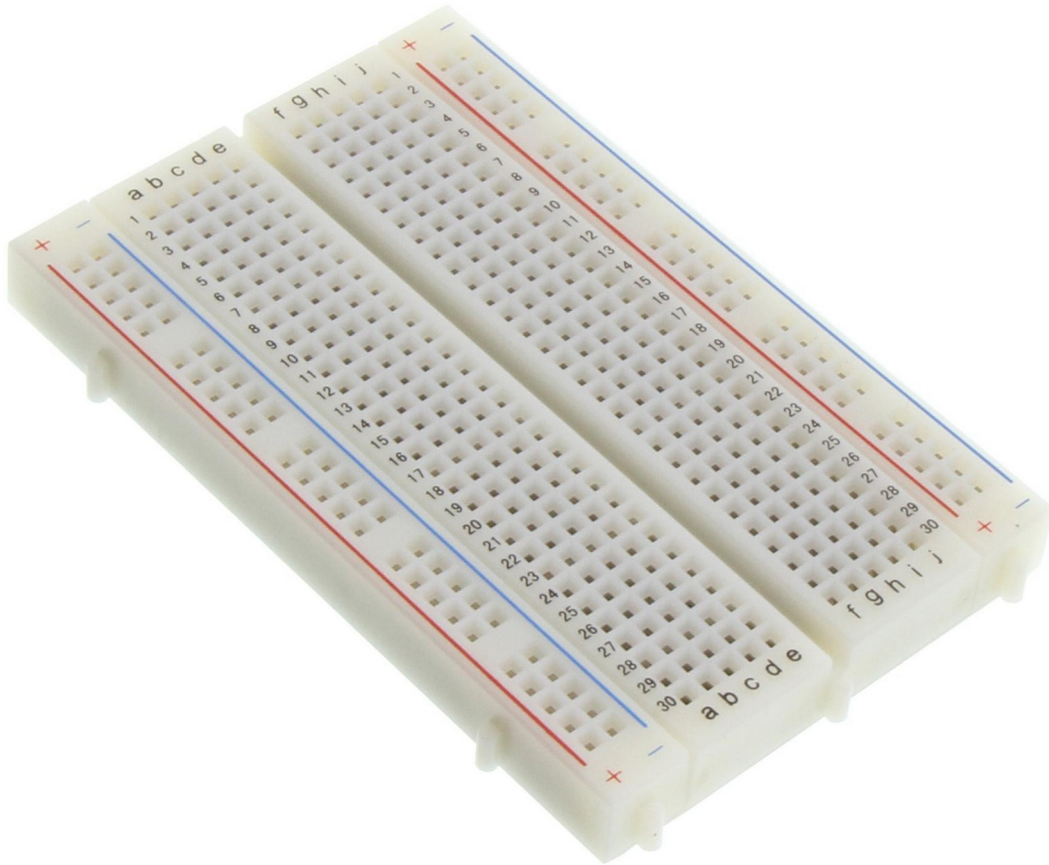
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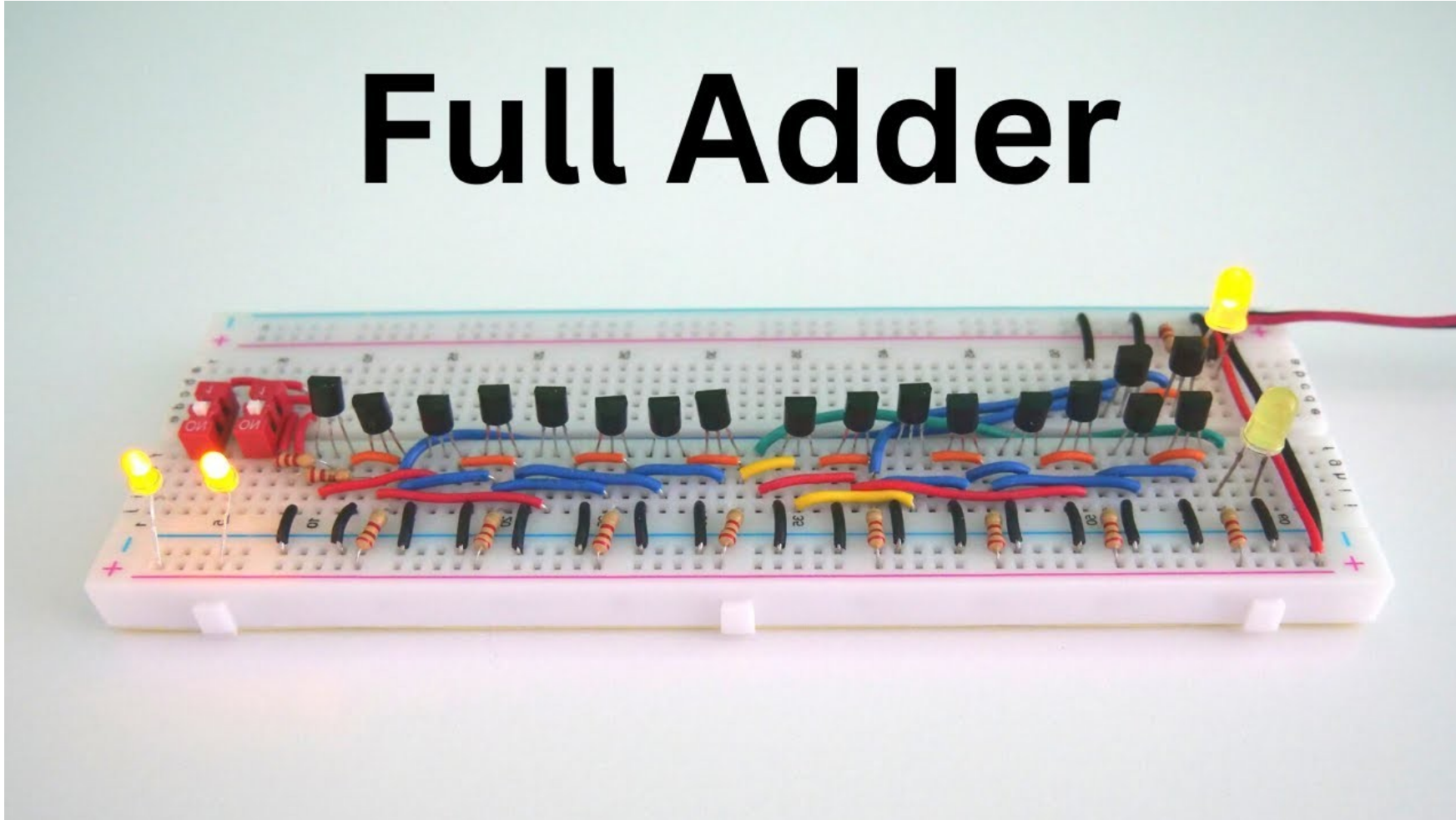


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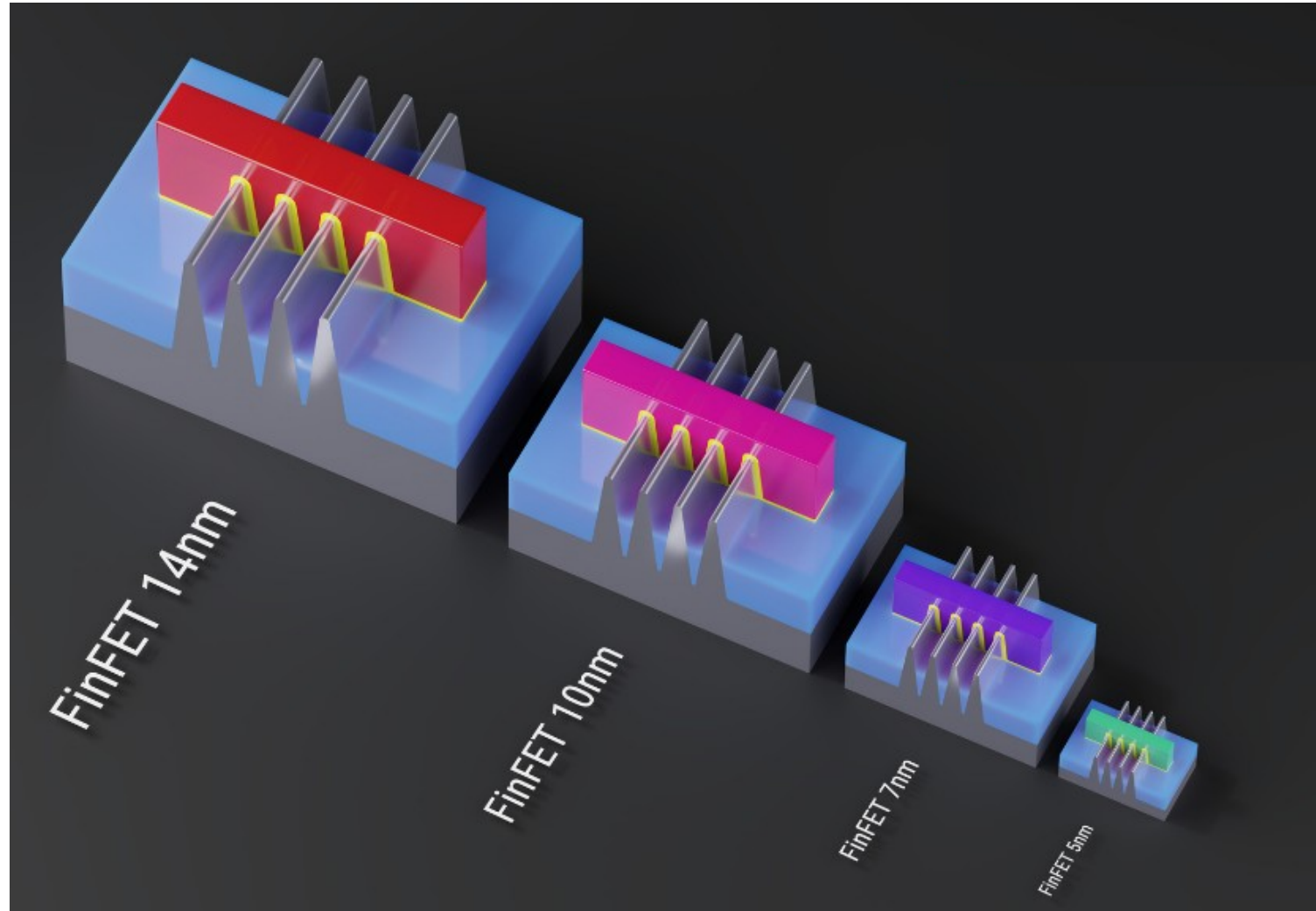


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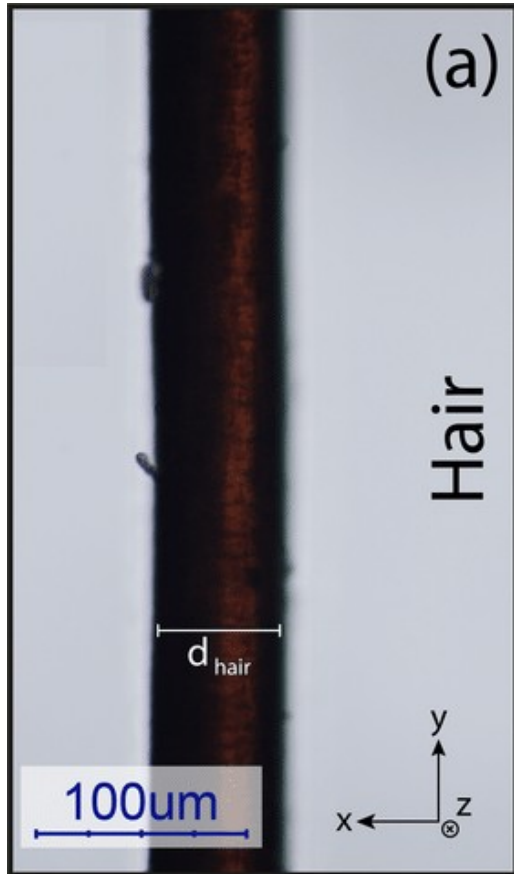
Full Adder



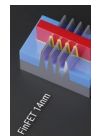
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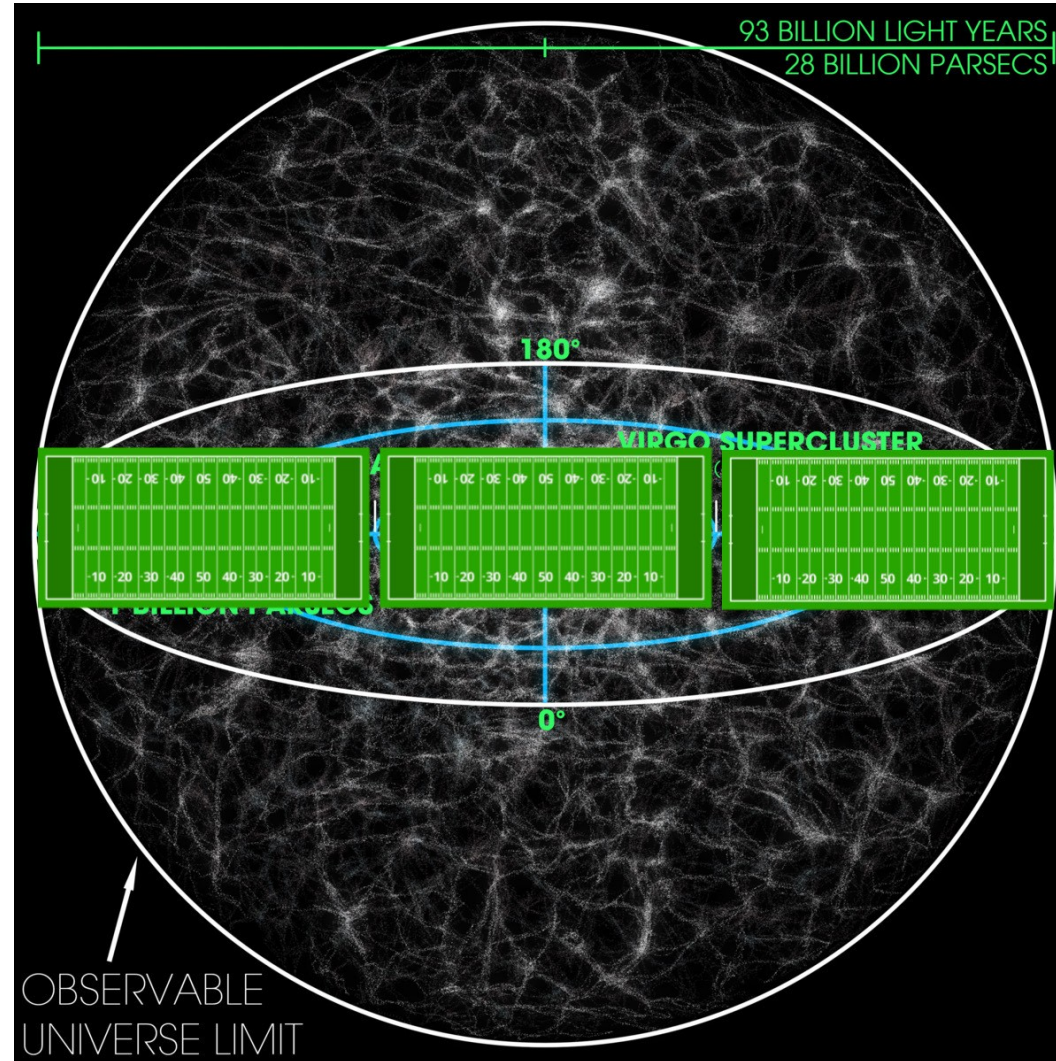
$$60\mu\text{m} = 60,000\text{nm}$$



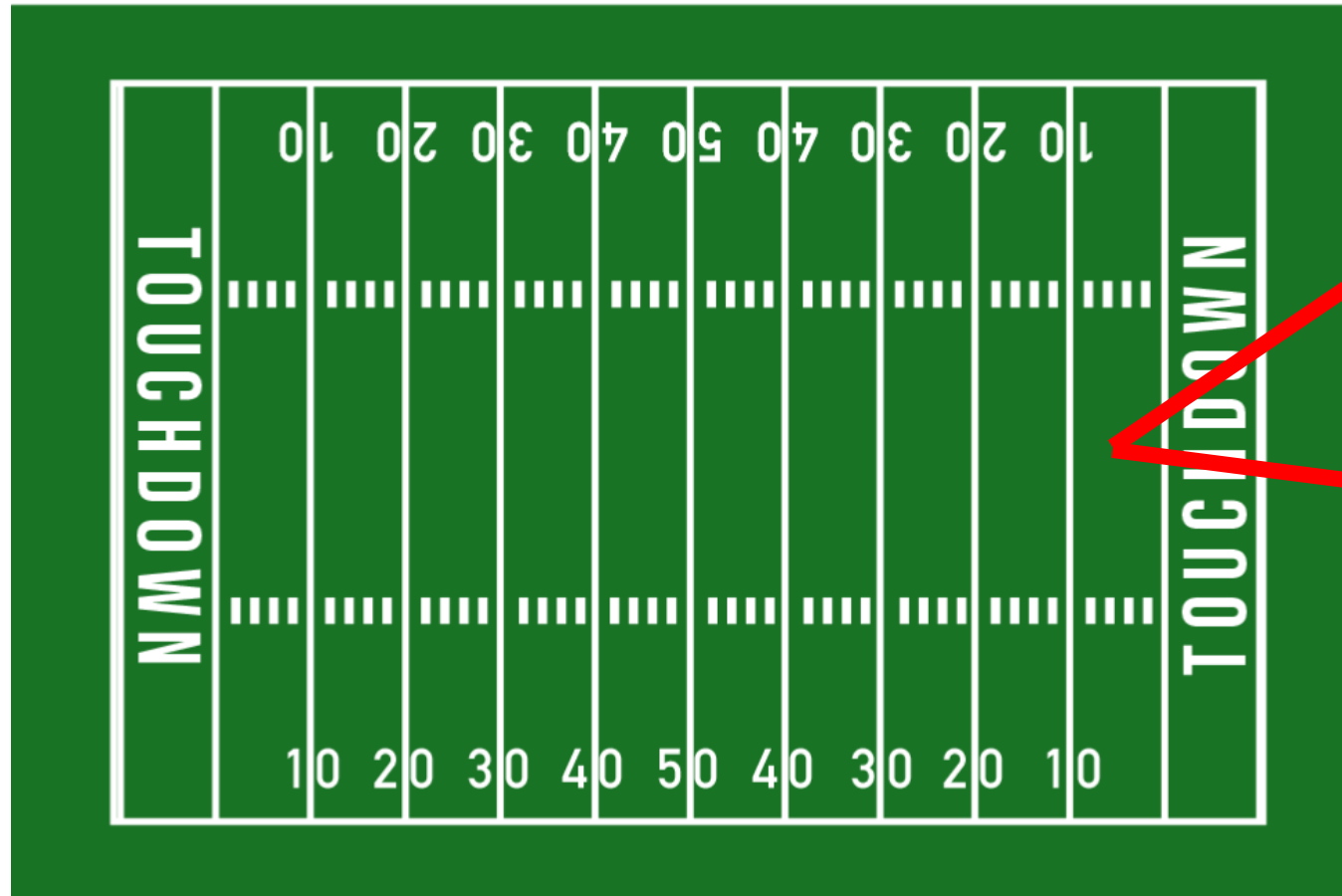
$$14\text{nm}$$

$$\frac{60,000}{14} \approx 4000$$

What is Lithography? Why is Lithography? (How is Lithography?)



What is Lithography? Why is Lithography? (How is Lithography?)



Human hair diameter (60 μ m)



14nm FinFET

What is Lithography? Why is Lithography? (How is Lithography?)

Probably not going to be
able to make 14nm
transistors using hands,
tools, machines, etc...

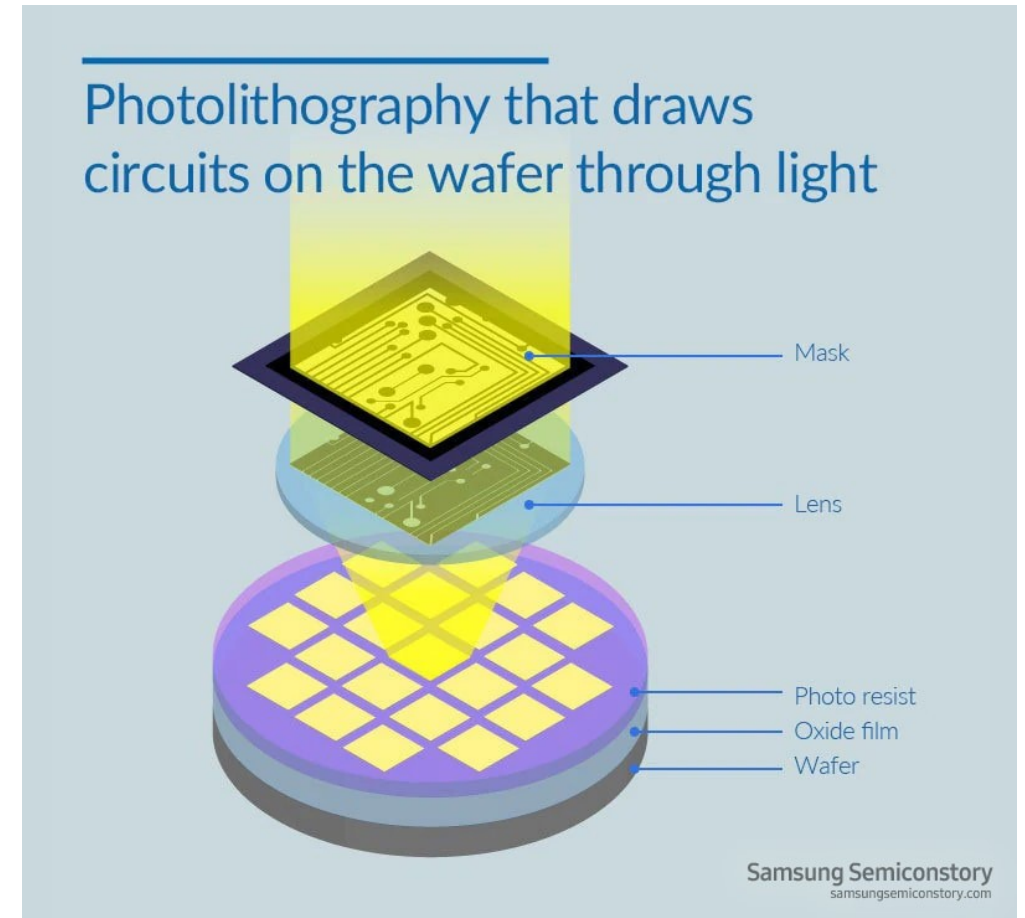
What is Lithography? Why is Lithography? (How is Lithography?)

The solution?

- **LITHOGRAPHY!**
- Basically, we'll design our transistors and circuits using light

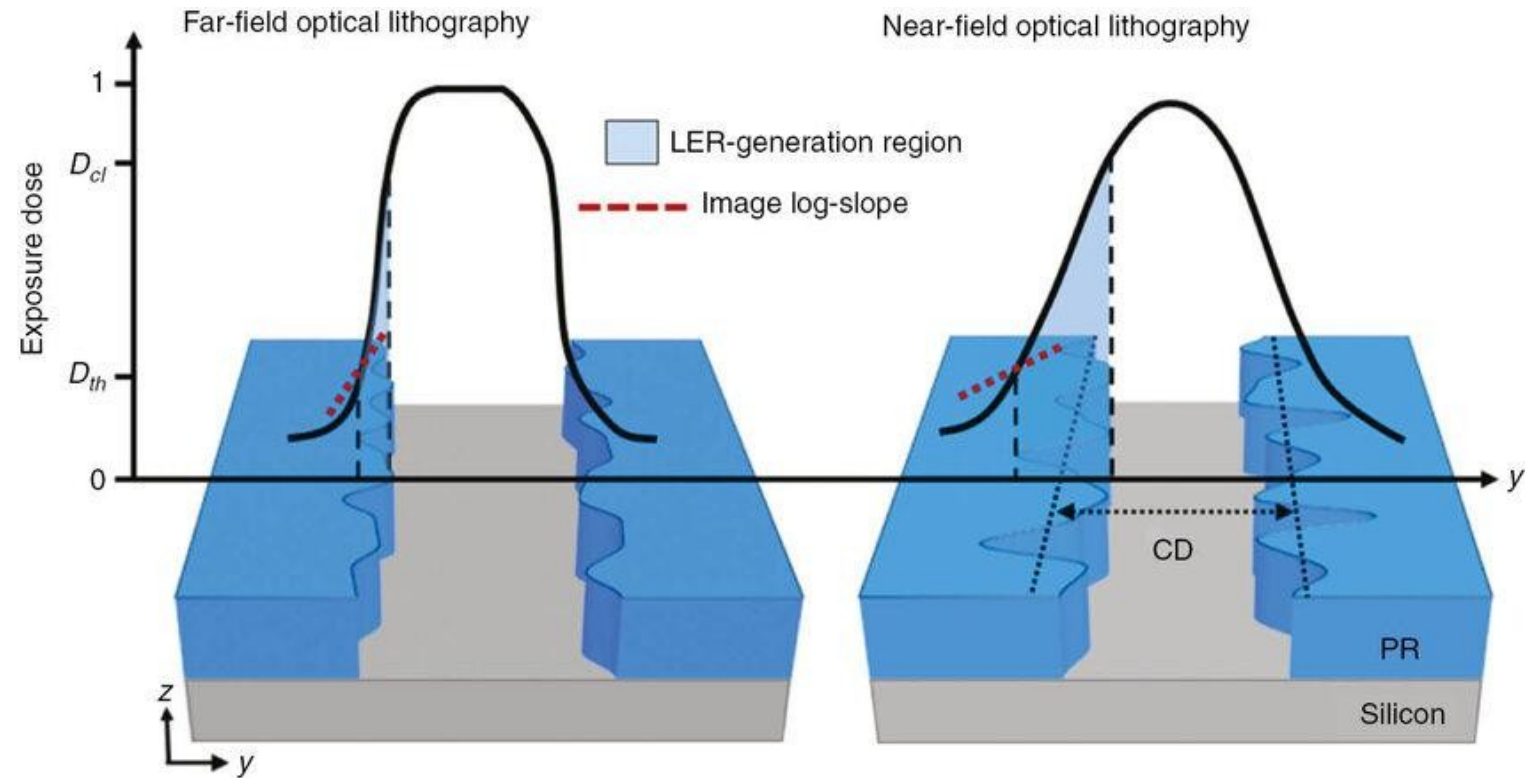
What is Lithography?

- Method of transferring circuit design to silicon wafer
 - Patterns are too small to be transferred physically
 - Light has wavelength in scale $\sim$ nm
 - Followed by less precise “blanket techniques”



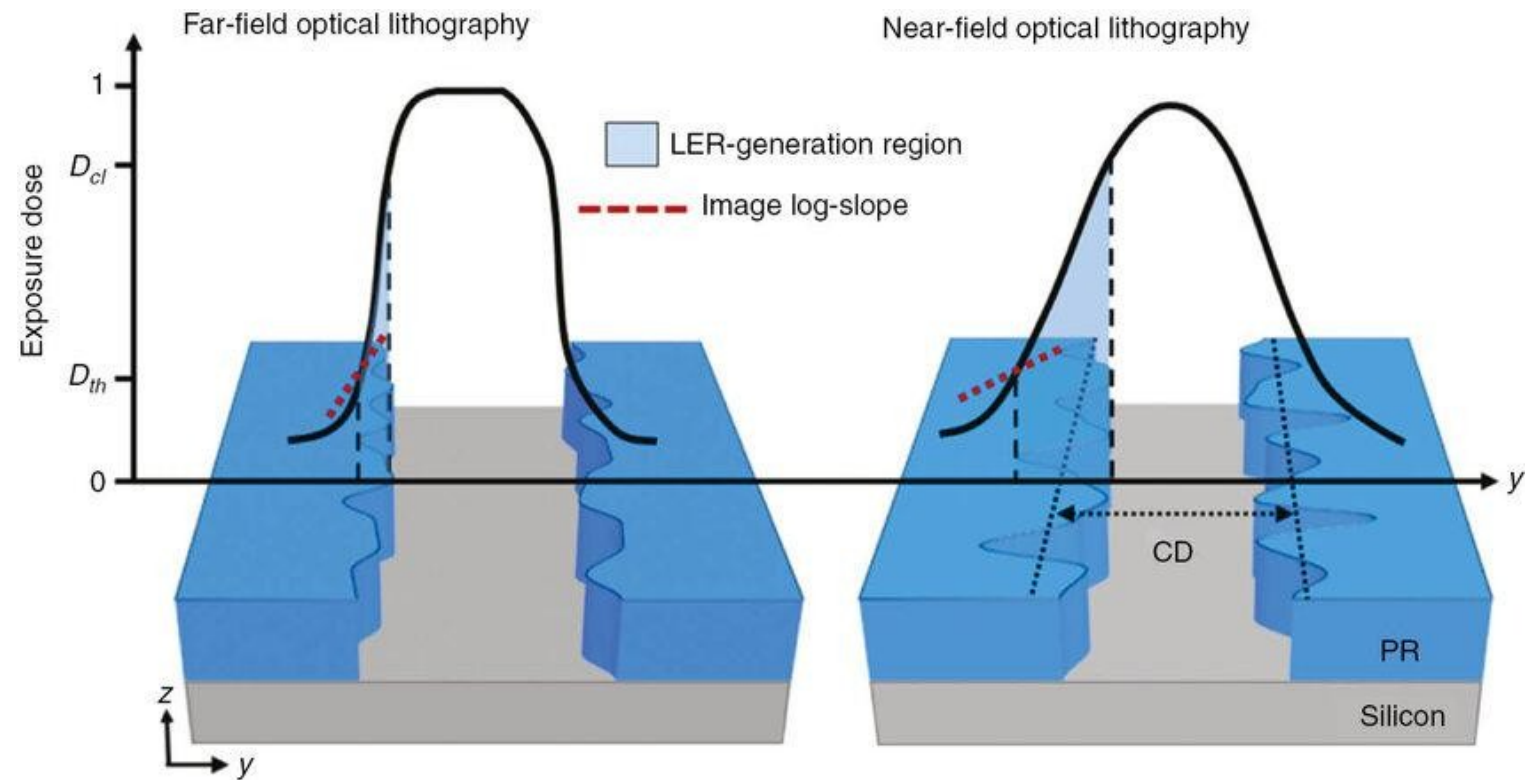
Lithography Over the Years

- What is the goal when optimizing the lithography process?



Lithography Over the Years

- What is the goal when optimizing the lithography process?
 - Better resolution!



Lithography Over the Years– Characteristic Equation

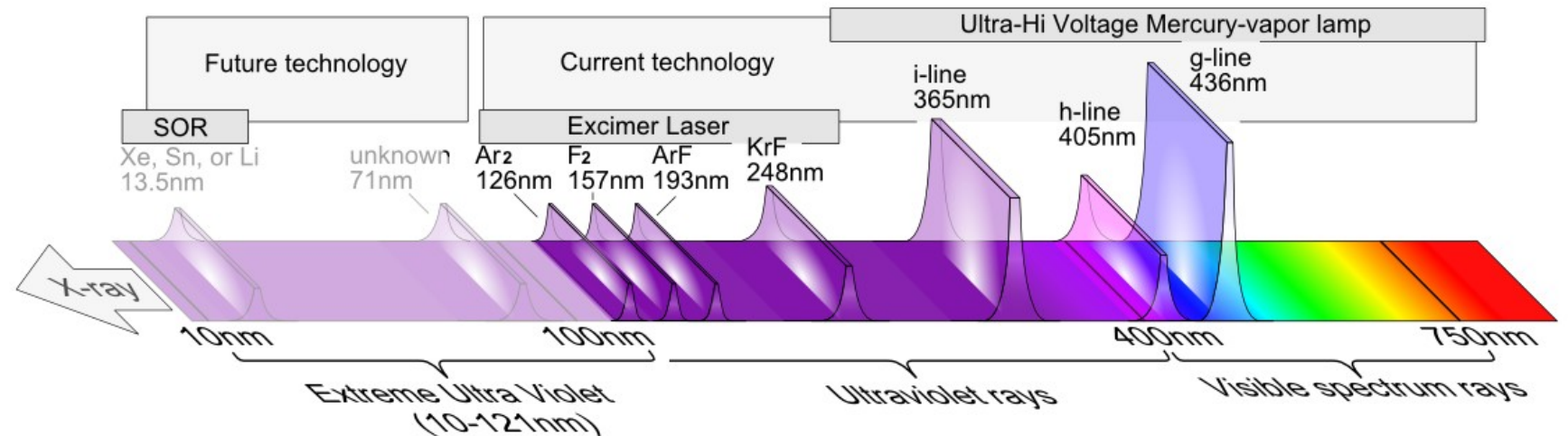
- CD: Critical Dimension (Minimum feature size)
- K1: Process Coefficient
 - Typ. 1, Can go to ~0.5 or lower
- Lambda: Wavelength of incoming light
- NA: Numerical Aperture
 - Typ. 0.5–0.7, can go above 1, min 0.1

$$CD = k_1 \frac{\lambda}{NA}$$

We'll come back to this...

Lithography Over the Years– Wavelengths

- Mercury Lamp (UV)
 - G-line (436nm), H-line (405nm), I-line (365nm)
- Excimer Laser (DUV)
 - KrF (248 nm)
 - ArF (193nm)
- EUV (13.5nm)



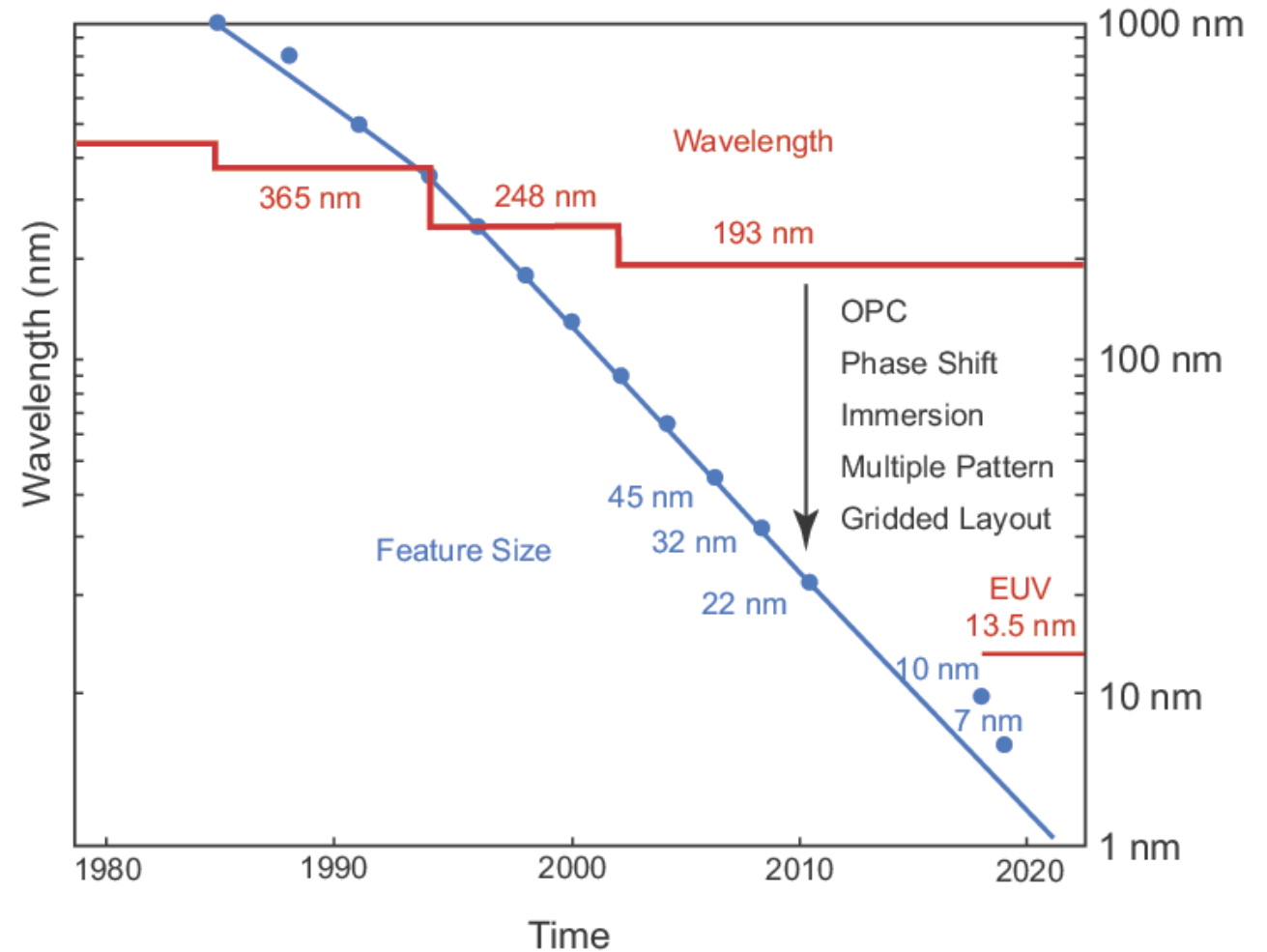
Lithography Over the Years

Before 1990:

- “Like drawing thick lines with a sharp pencil”

After 1990

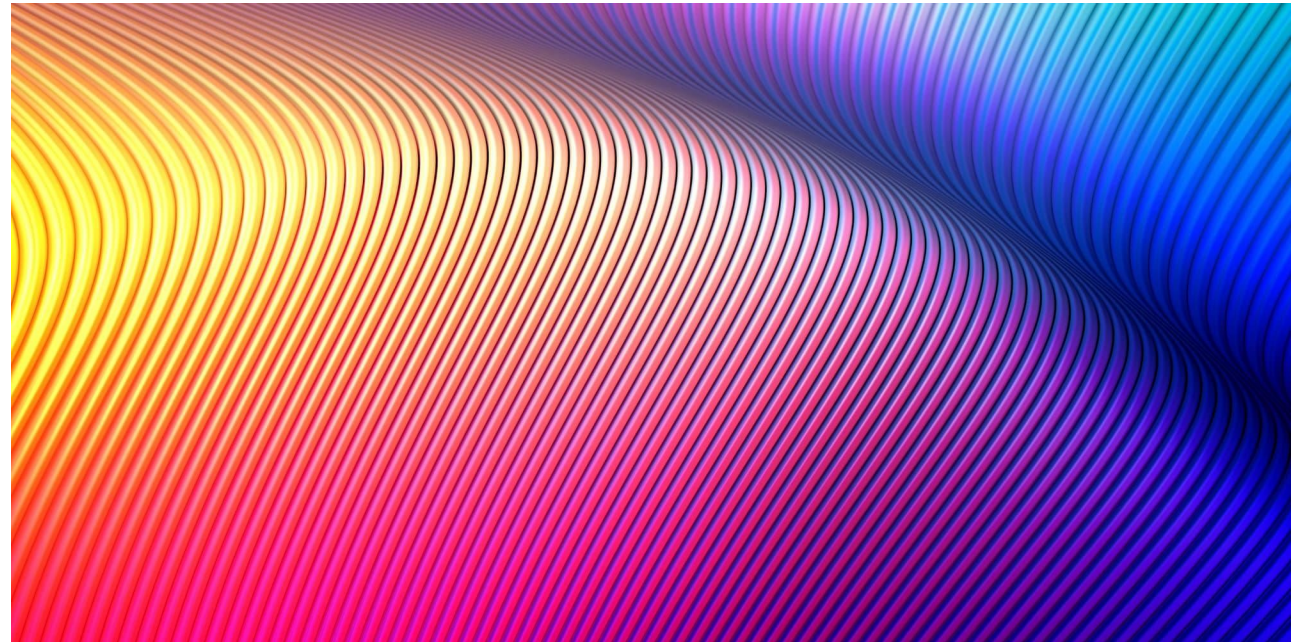
- “Mask Designer’s Nightmare”



Resolution Enhancement Techniques – Brute Force for Moore's Law (k1)

Resolution Enhancement Techniques

- Optical Proximity Correction
- Phase Shift Masks
- Immersion Lithography
- Double Patterning Techniques

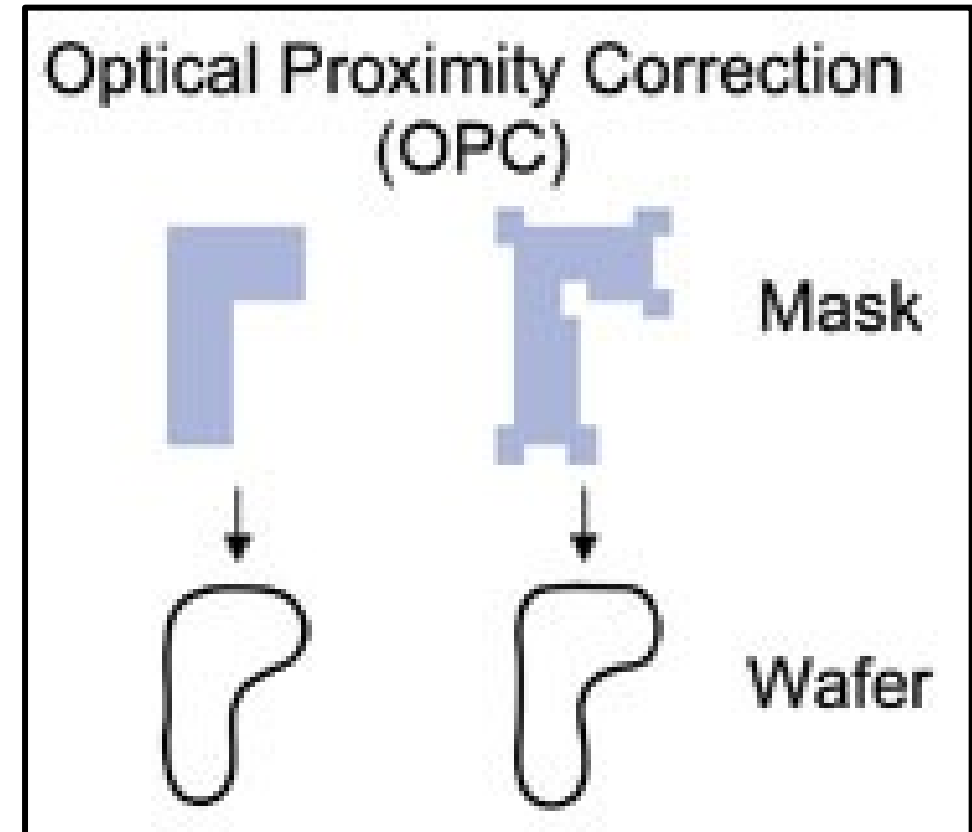


(image unrelated)

Resolution Enhancement Techniques – OPC

Optical Proximity Correction (OPC)

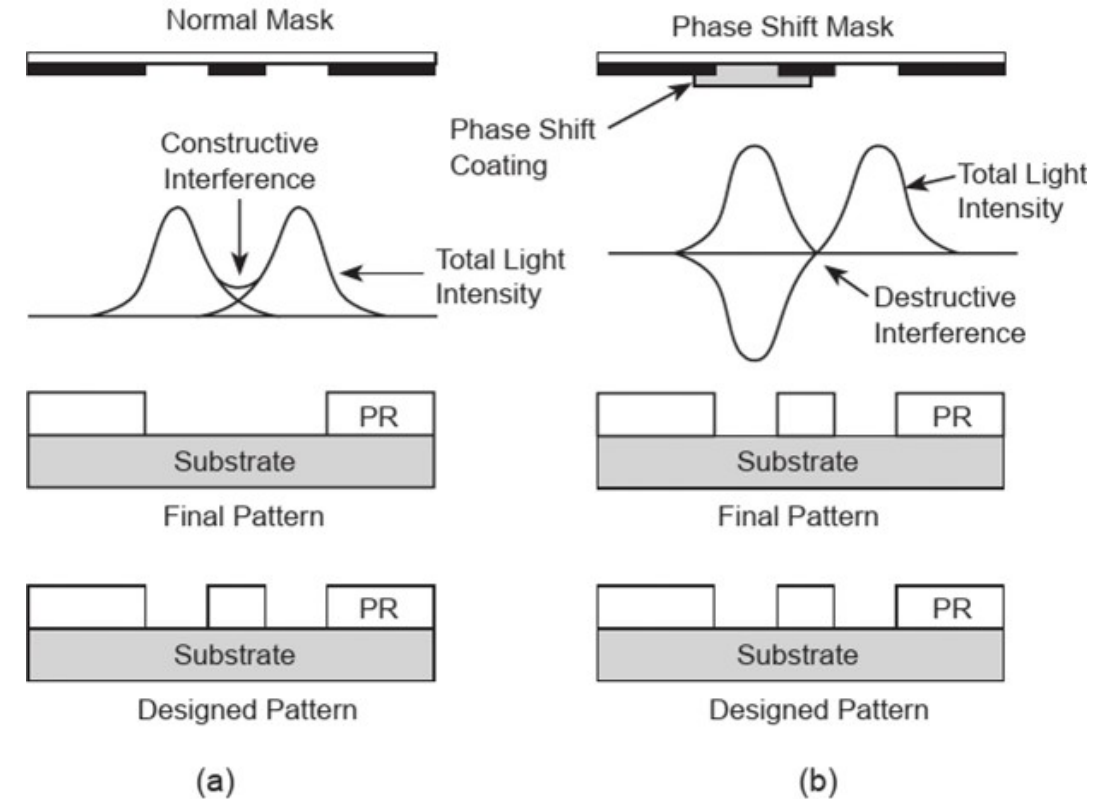
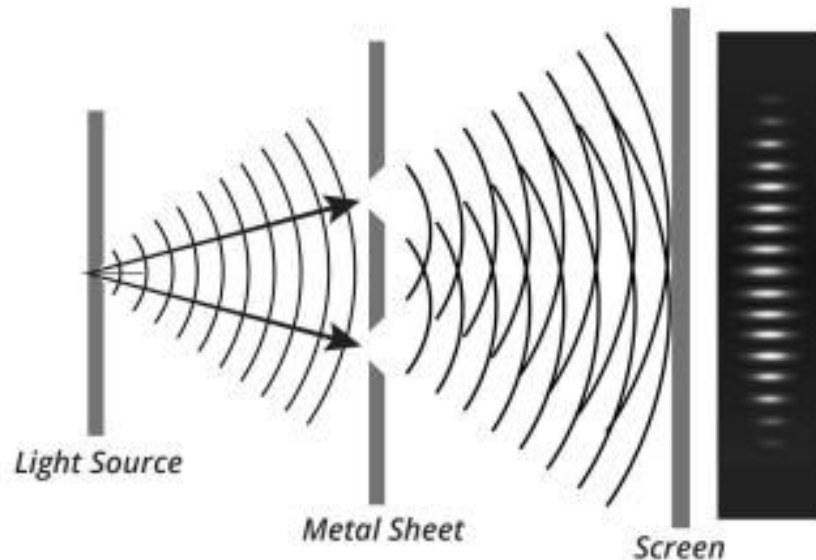
- Constructive/Destructive Interference
 - Introduce serifs/additional patterns so OUTPUT looks correct (mask doesn't)
- VERY interesting field for optics engineering & computer science



Resolution Enhancement Techniques – Phase Shift Masks

Phase Shift Masks

- Control interference for better feature fidelity

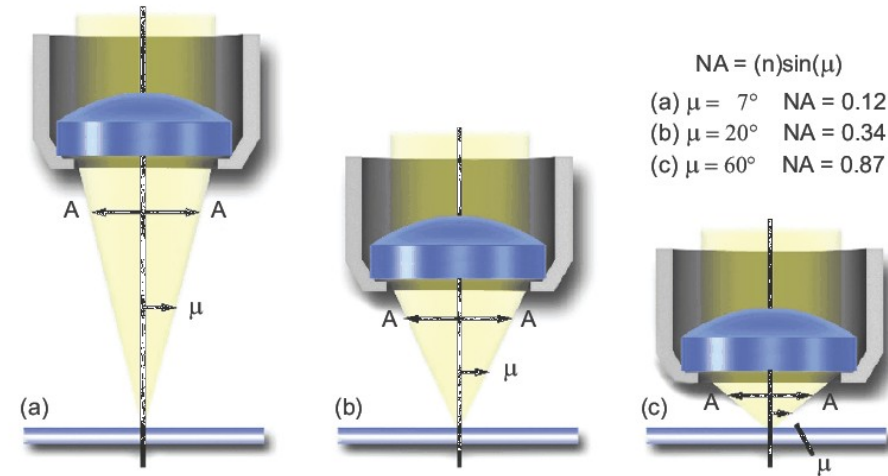


Resolution Enhancement Techniques – Immersion Lithography

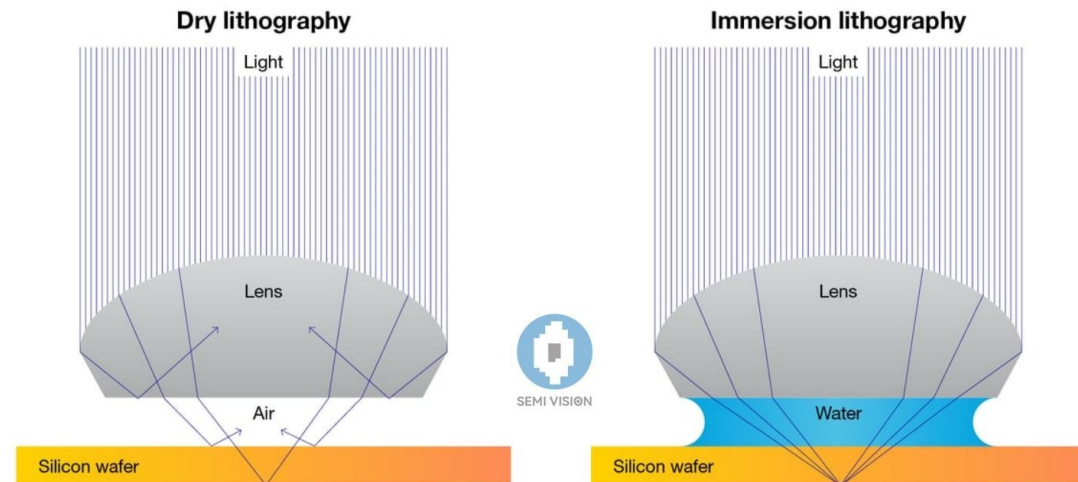
Immersion Lithography

- Increase Numerical Aperture (Sharper Focusing of light)
- $NA = n \sin(\theta_{max})$

Numerical Aperture and Airy Disc Size



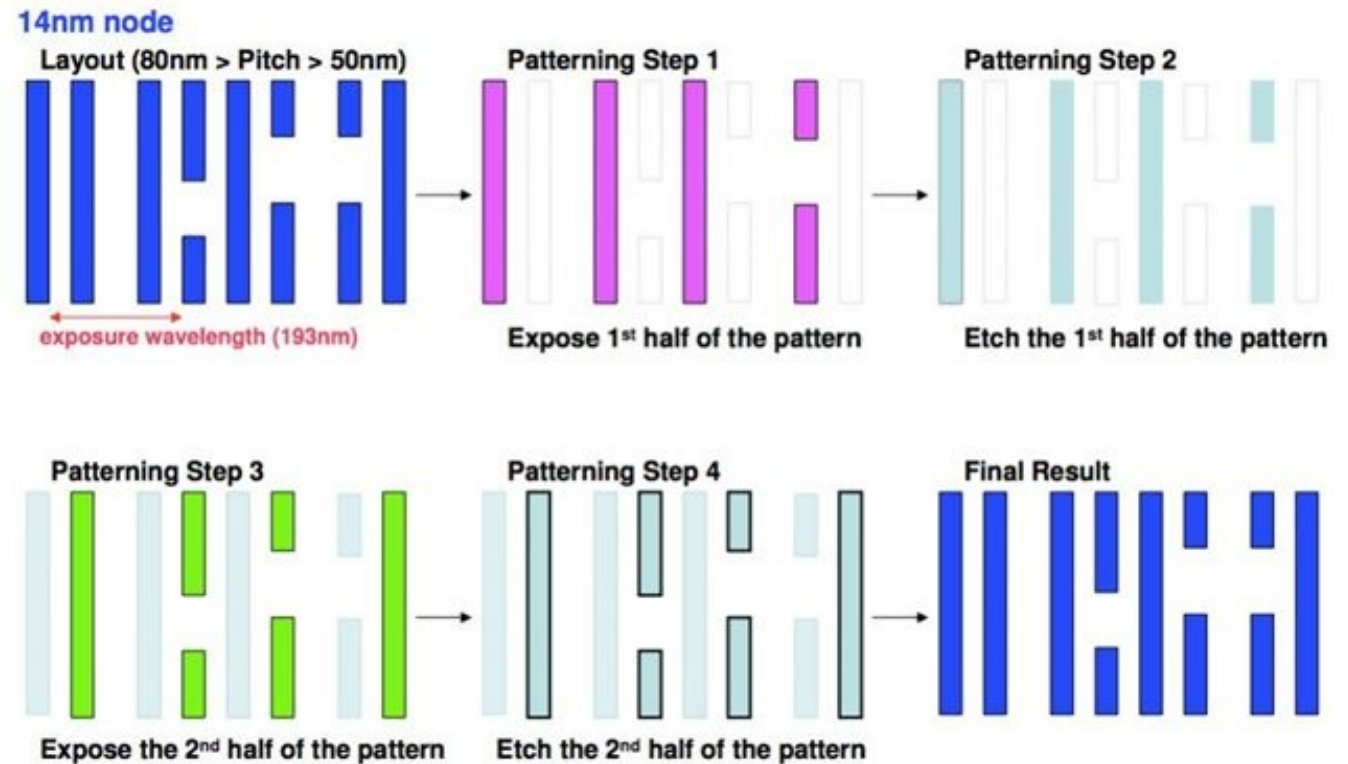
$$CD = k_1 \frac{\lambda}{NA}$$



Resolution Enhancement Techniques – Double Patterning

- Solve interference problem by just making more masks
 - 2x, 4x patterning

POV: Mask designers selling more masks to do the same work



Mask Design

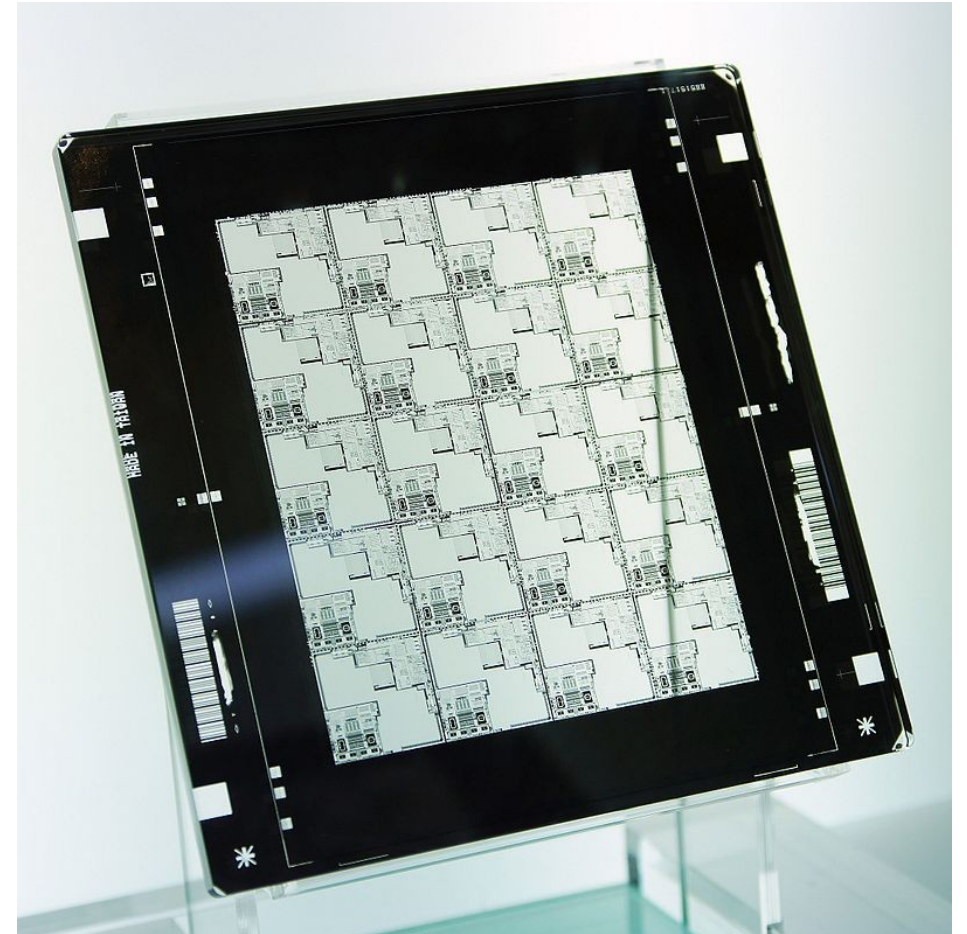
Exposure Area:

- Limited by Reduction Lenses
- ~26x33 mm max

DUV/Older systems:

- Quartz (Fused Silica)
- Chromium
- Can cost ~10-100k

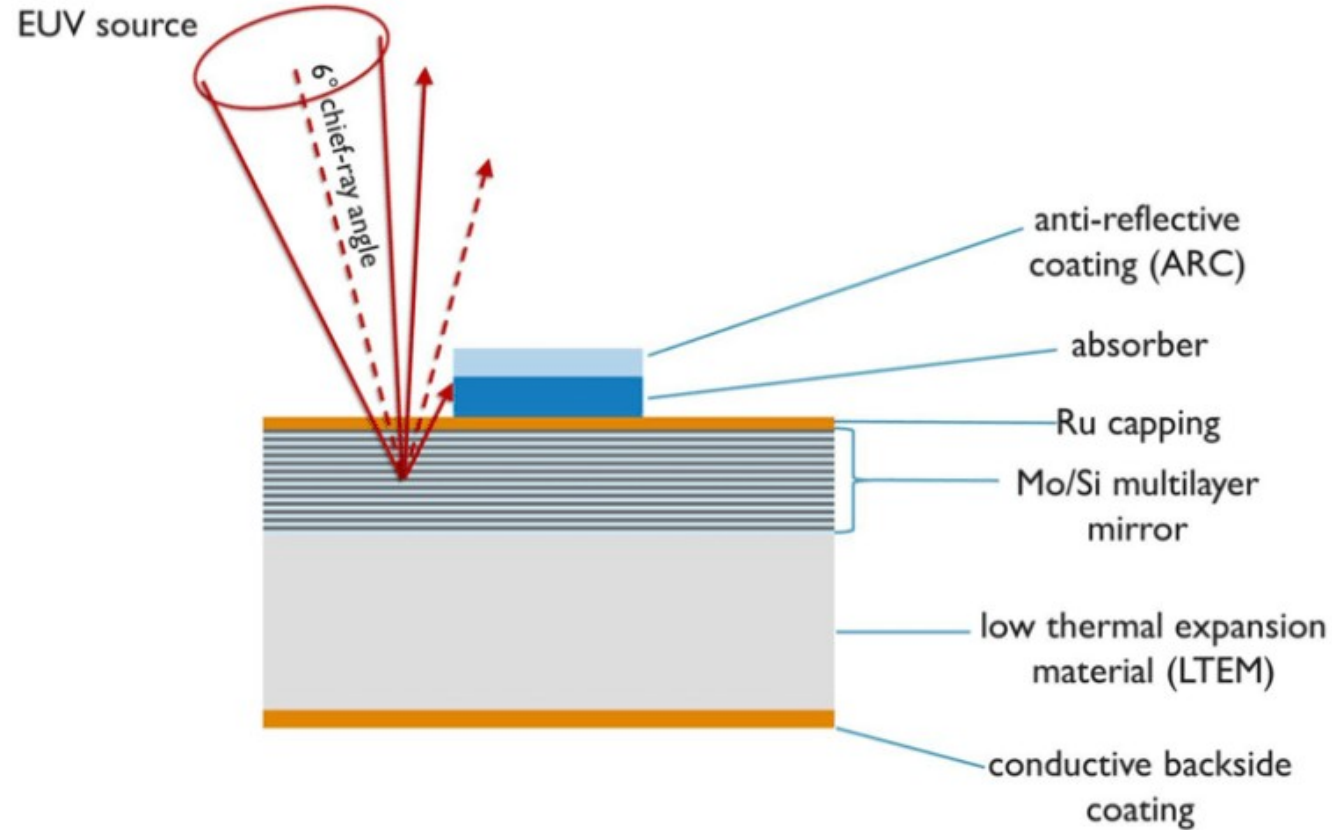
https://youtu.be/9RZreu5z_Gc?si=rI32Z36lvvmAOuUI



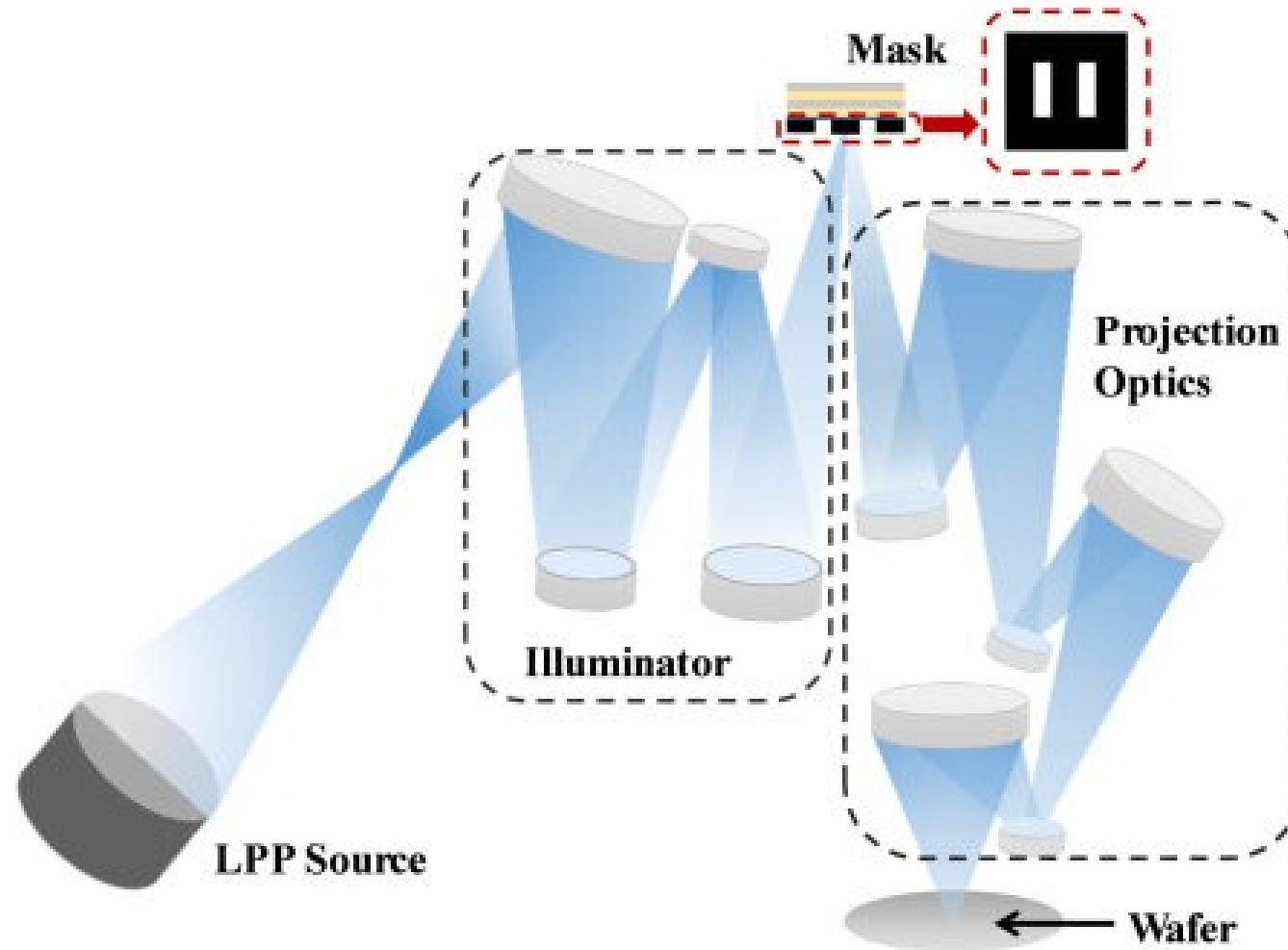
Mask Design (EUV)

Extremely Expensive

- “Mirror mask”
- ~70% of energy is absorbed
 - 11 mirrors $\rightarrow 0.7^{11} = 2\%$ energy transfer
- 50+ layers of Molybdenum + Silicon
- Can cost ~500k each

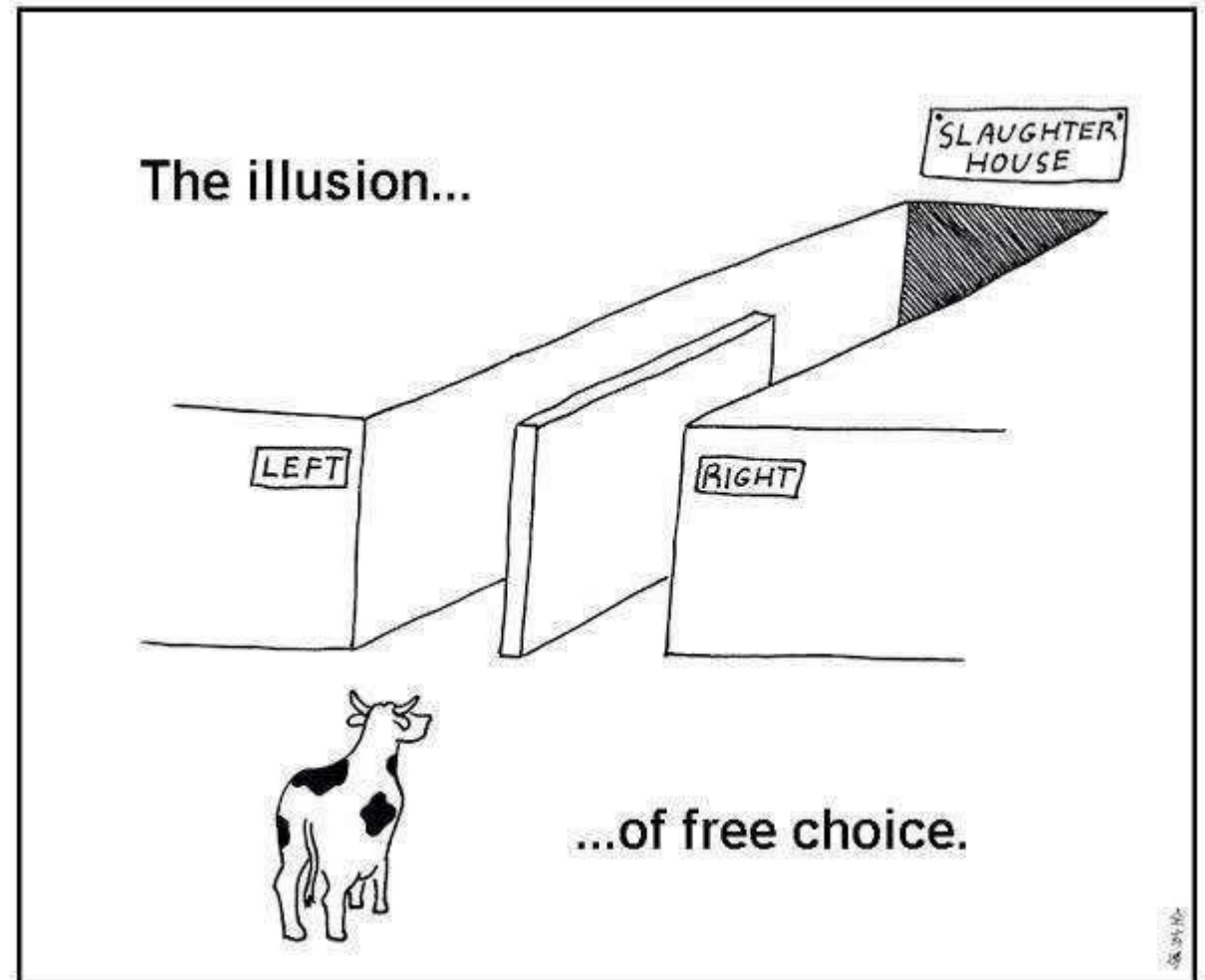


Mask Design (EUV)



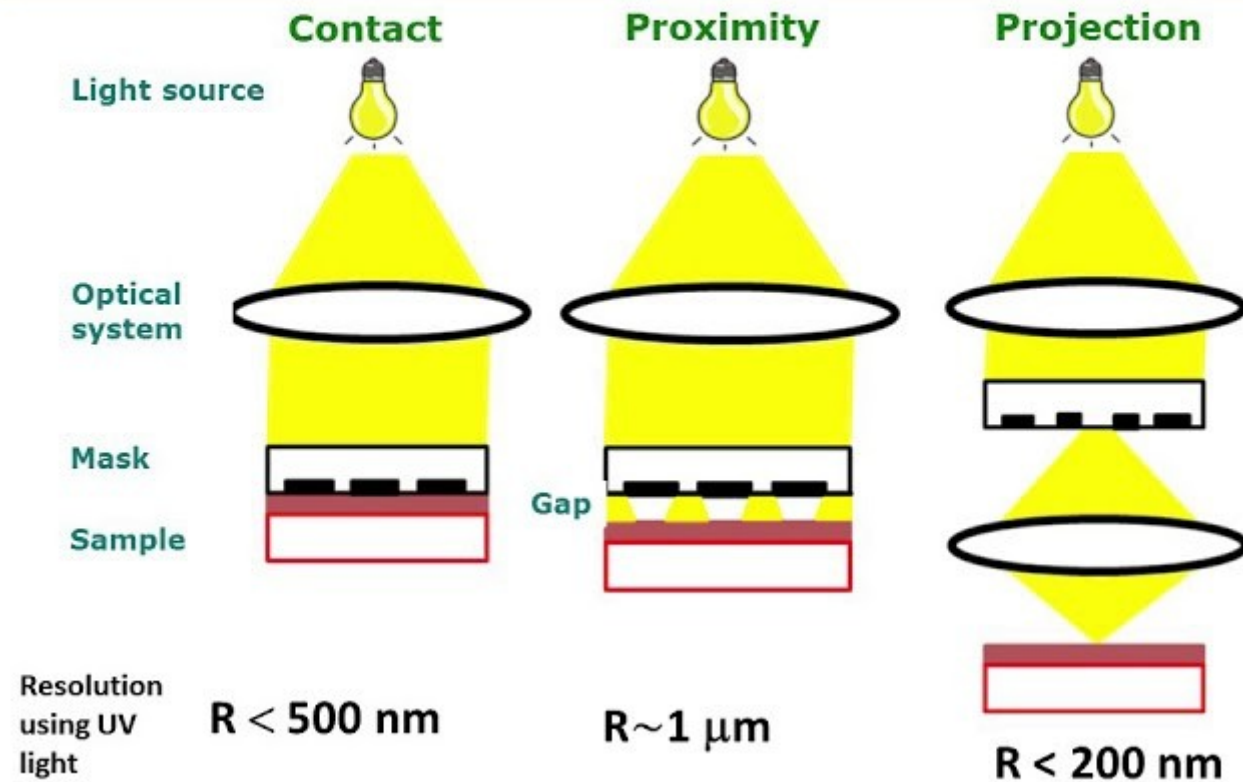
Lithography Types- “Choose your own adventure”

- Contact
- Non-Contact
- Projection
- E-Beam*



Lithography Types- “Choose your own adventure”

Optical lithography: techniques



Lithography Types- Performance Comparison

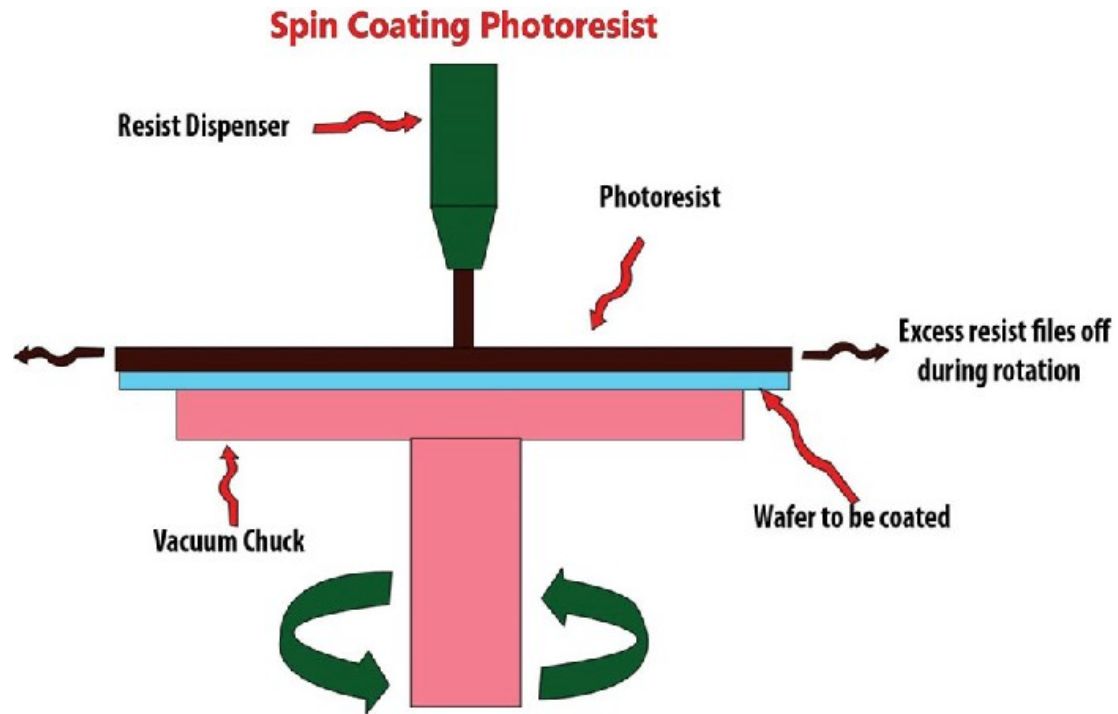
- Each are useful!
 - Which would you use for...
 - Academic (Very low volume)
 - Industry (High Volume)
 - Research

Parameter	Contact	Non-Contact	Projection	E-beam
Cost	Low	Low	High	High
Speed	Med	High	High	Low
Defectivity	Very High	Low	Low	Low
Resolution	Med	Low	High	Very High
Complexity	Low	Med	High	Med

Lithography Procedure

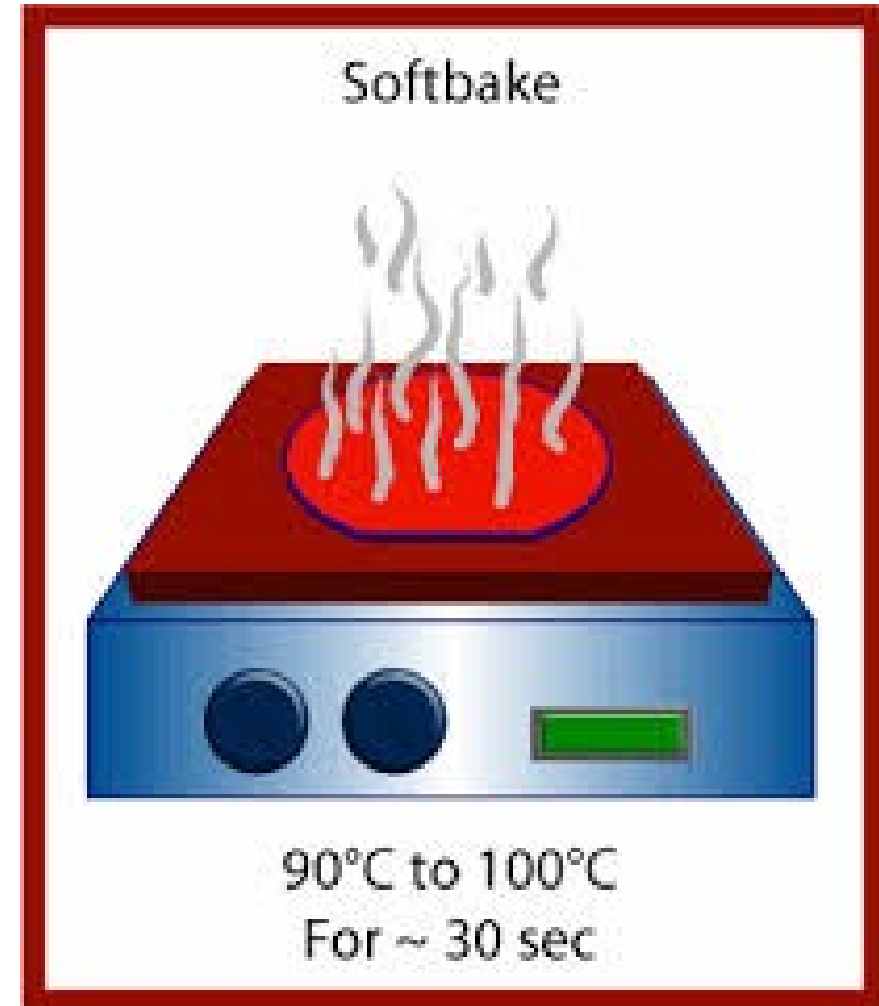
- Spincoat
- Soft-Bake
- Expose
- Post-exposure Bake (Optional)
- Develop
- Hard-Bake

Lithography Procedure- Spincoat



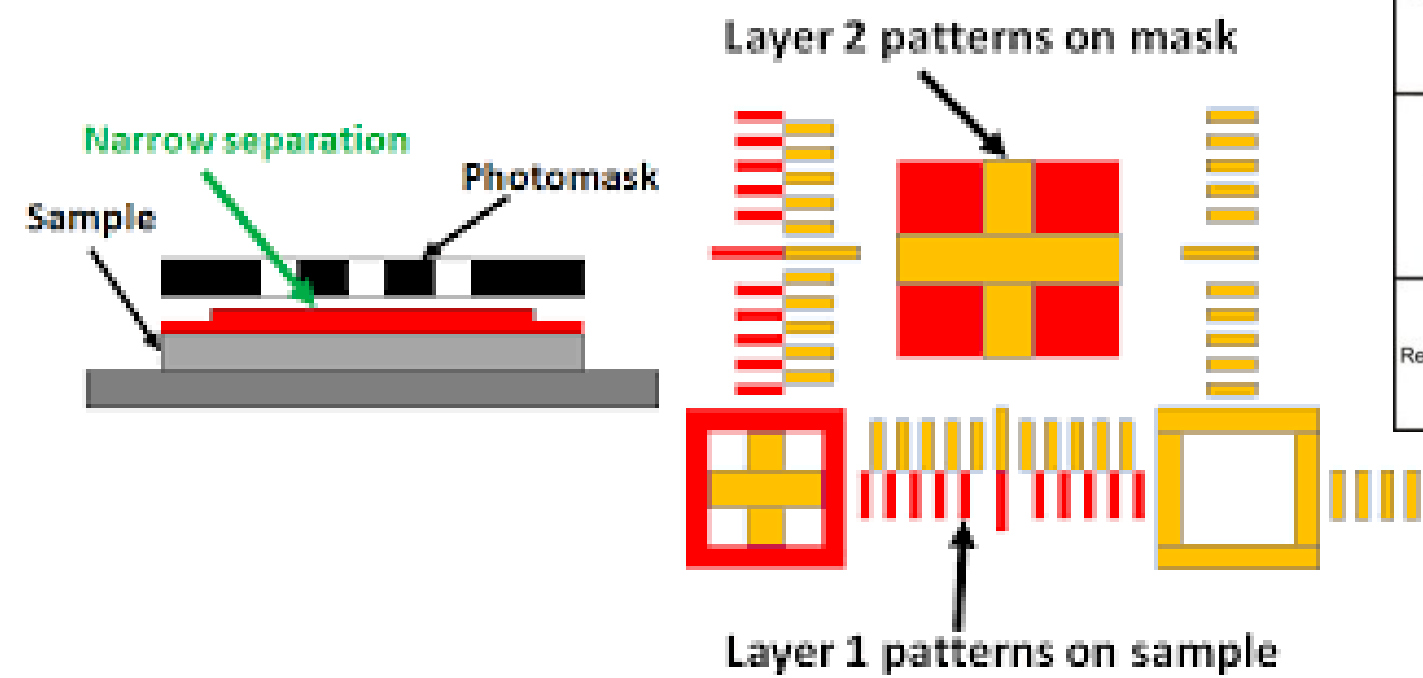
Lithography Procedure– Softbake

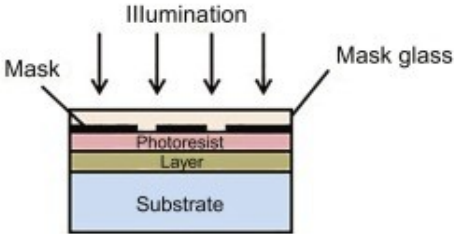
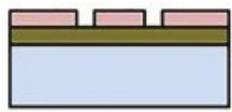
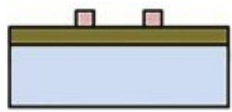
- Solidify photoresist
- Removes solvent
- Can be done with hotplate in research applications
- Integrated in lithography machine for industry applications



Lithography Procedure- Exposure

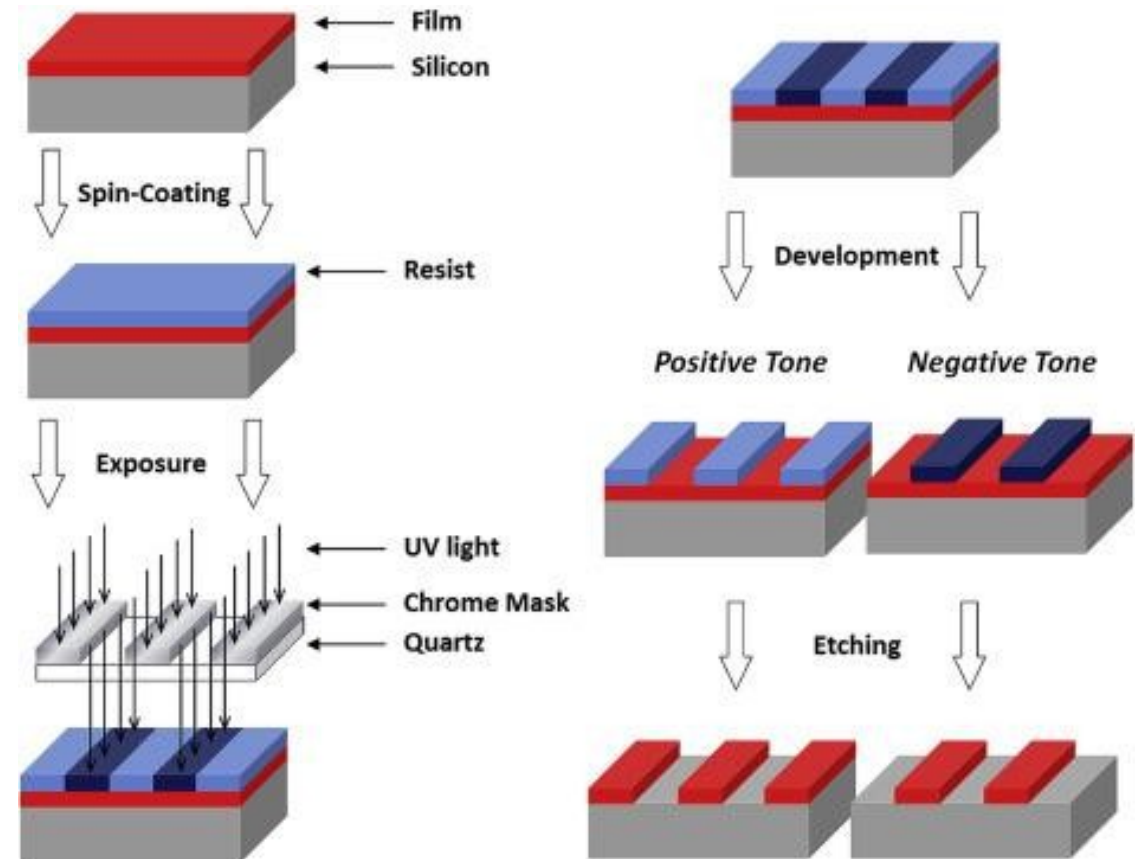
- Align with previous layers of mask
- Use lightsource (EUV, DUV, etc) to bond photoresist



Illumination		
	Positive resist	Negative resist
Development		
		
Etching		
		

Lithography Procedure- Develop

- Dissolves un-bonded photoresist



Lithography Procedure– Modern Systems



https://youtu.be/h_zgURwr6nA?si=Jx0LdQDefZiJwbs1



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The End

Thanks for listening!

GBM Attendance



Kahoot Time!

