Deposition Techniques

Additive Manufacturing for Semiconductors

Jonas Kendra

GBM Attendance

General Updates

- GlobalFoundries Tours
- Cool Courses!
  - ECSE 4250: Integrated Circuit Process and Design
  - ECSE/ENGR/ISCI 4961/6961 – Advanced Materials, Metrology, and Equipment for Semiconductor Manufacturing
- Mini-Colloquium is happening!
  - April 18th
    - Pizza
    - Speakers
    - Fun

GlobalFoundries Tour

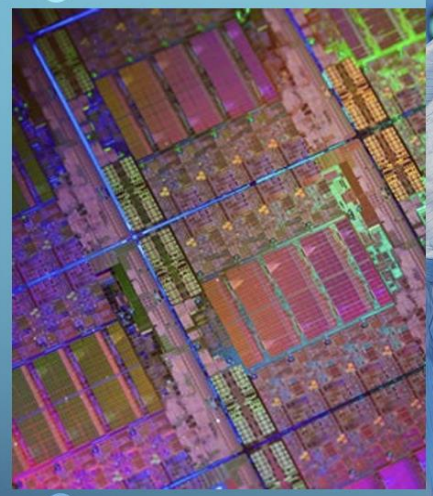
GlobalFoundries Fab 8

- GlobalFoundries Headquarters
- 30 minutes from Troy
- Get to go into fab and see fab equipment in action
- When: Wed April 9th, ??am - ??pm

Early Interest Form!

ECSE 4250 - Integrated Circuit Process and Design

ECSE 4250 | INTEGRATED CIRCUIT PROCESS & DESIGN



Do you want to be a part of the exiting Chips world?
Do you want to learn about the IC Fabrication?
Register to ECSE 4250 in Fall 2025!

Workhorses of the computing world are the Integrated Circuits.

Chip demand is increasing even more with latest AI, machine learning and communications.

If you want to work in chip fabrication or just understand the fabrication principles to be a better IC designer, this course will cover the latest IC device manufacturing processes.

You will learn the latest Synopsys simulation tools.

You will also have a chance to visit the RPI cleanroom and Albany Nanotech facilities.

Prereq:
ECSE 2210 Microelectronics Technology or instructor's permission.

Any questions: Dr. Muhsin Celik, celiks@rpi.edu, JEC 7026

ECSE/ENGR/ISCI 4961/6961 – Adv Mats, Metro, and Eqpt Semi Mfg

Semiconductor Workforce Development Course, Fall 2025

ECSE/ENGR/ISCI 4961/6961 - Adv Mats Metro Eqpt SEMI Mfg

- A required core course for a new M.S. in Semiconductor Technology

https://news.rpi.edu/2024/02/29/rensselaer-polytechnic-institute-develops-new-courses-semiconductors-partnership

Materials, Metrology, Equipment, Data Analytics and Infrastructure Enable Semiconductor CHIP Manufacturing That's Changing the World

Semiconductor manufacturing has become the most sophisticated manufacturing process in human history, drawing on many disciplines incl. **Chemical, Electrical, Material, Mechanical, and Industrial Engineering,** plus **Chemistry, Physics, and Computer Science**.

This pilot course, co-taught with a team of 20+ leading industry experts, will introduce, and provide deep insight into, the technological advances in Materials, Metrology, Equipment, Automation, Data Analytics & Infrastructures that enable the semiconductor manufacturing with astonishing increase in performance and functionality and reduction in energy, size and cost.

ECSE/ENGR/ISCI 4961/6961 – Adv Mats Metro Eqpt SEMI Mfg, M/R: 4:00-5:20PM, Fall 2025.

For more information: https://rpi.box.com/v/MME4SemiMfg-Syllabus-F25

Who May Enroll in This Course: This course is open to all **juniors, seniors & graduate** students across the campus, regardless of electrical engineering background; particularly, students who wish to explore career opportunities in computer chip manufacturing and the vast industry of semiconductor materials, metrology, equipment, automation and data analytics, may enroll in this course.

CHIPS for AMERICA

Workforce Development: The United States needs >50,000 **new** semiconductor engineers in the next five years for the new factories and research labs, a number far exceeding current graduation rates nationwide.

Rensselaer FORWARD

20+ Lecturers from 10 Semiconductor Companies.

General Updates

- Stuff
- Things

Overview

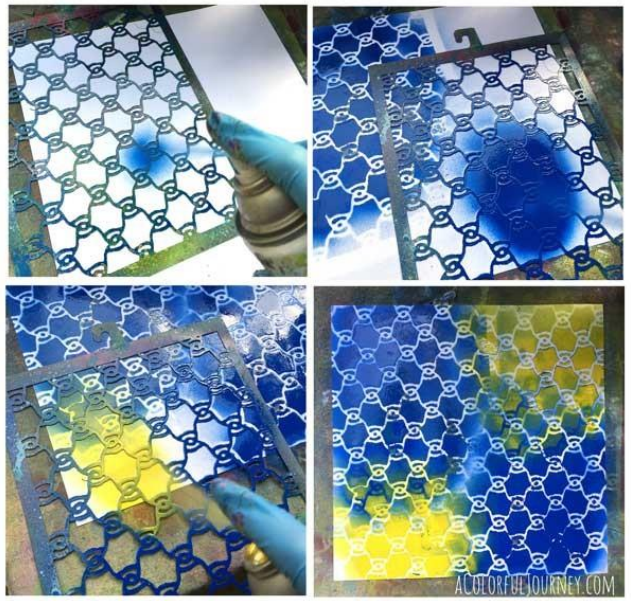
- Review of fabrication Techniques
- Spincoating
- Oxidation
- Physical Vapor Deposition
- Chemical Vapor Deposition
- Atomic Layer Deposition
- Electroplating

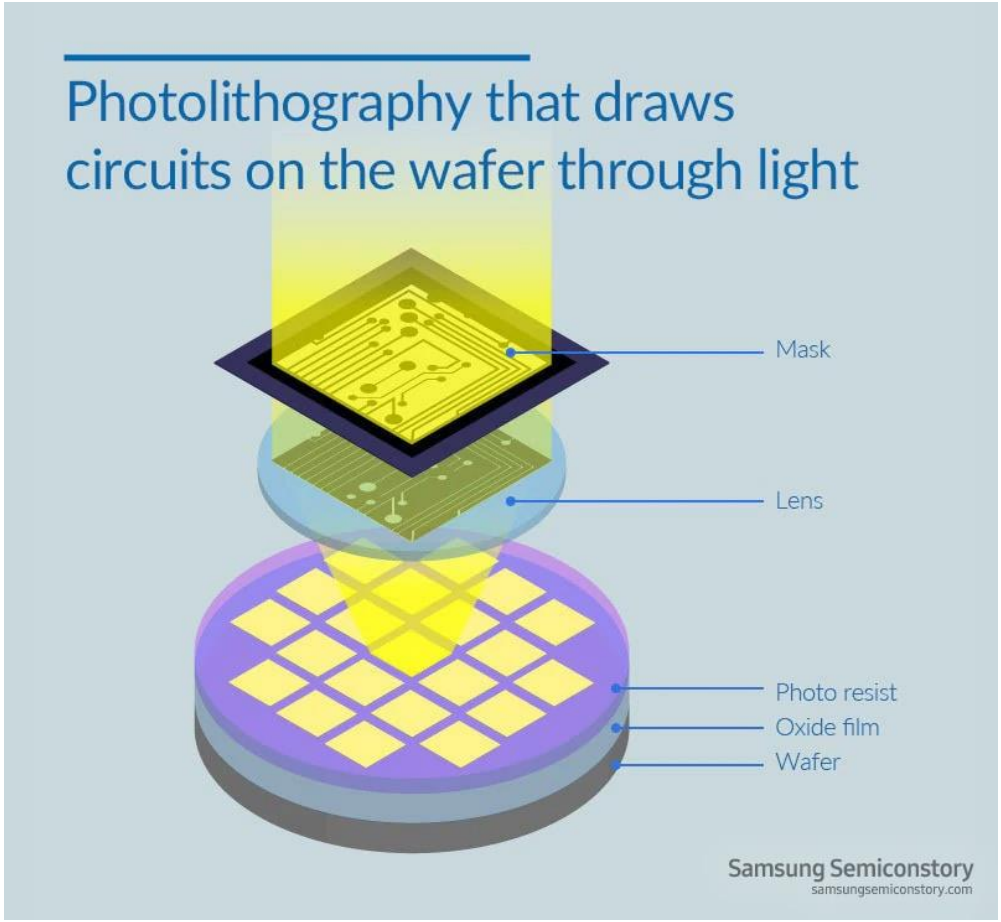
Fabrication Techniques

- Lithography (Framing)
- Implantation (Modification)
- Deposition (Additive)
  - Oxidation
  - Plating
- Etching (Subtractive)
  - Wet, Dry

Fabrication Techniques- Lithography

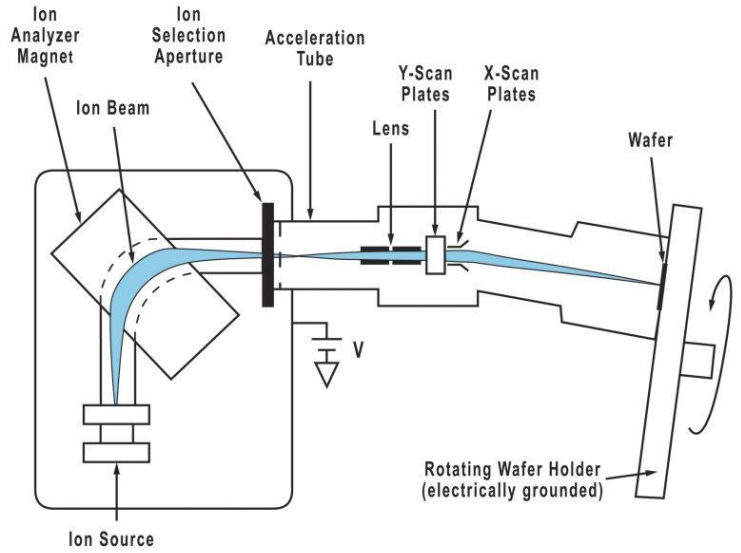
- Technique used to define where you want a pattern to stick
- In Semiconductor industry, involves wavelengths of light reacting with a chemical below
- New material can be added on top, or this can be seen as a stencil where material is removed

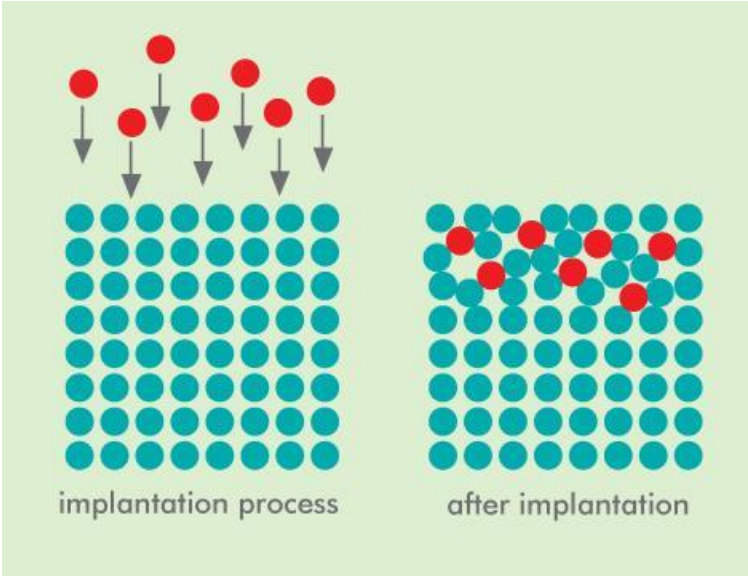




Fabrication Techniques- Implantation

- Used to modify properties of the wafer underneath
- In Silicon, dopants may result in excess electrons or holes (N, P-type)
- Slight changes in concentration results in large change in electrical conductivity (~100x)
- Always causes damage to substrate- must be repaired with an anneal step





Fabrication Techniques- Deposition

- Additive technique for wafer fabrication
- 3 (main) types
  - Oxidation
  - Deposition
    - Many sub-categories:
      - CVD, LPCVD, PVD, PECVD…
  - Electroplating

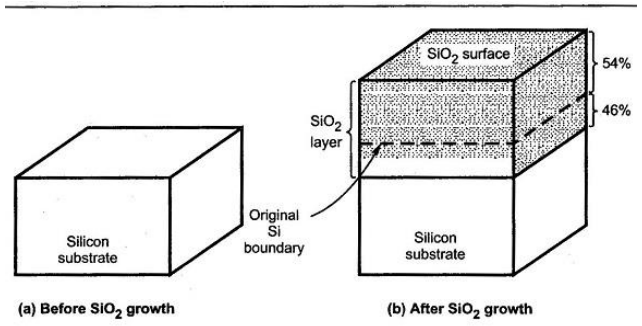
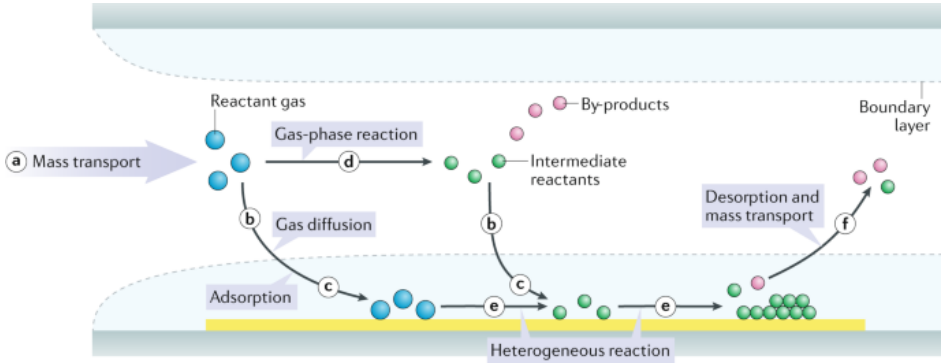
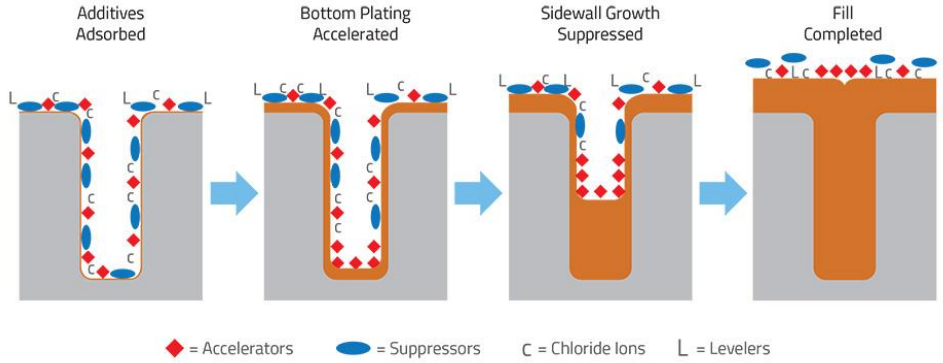


Fig. 1.4 Thermal Oxidation





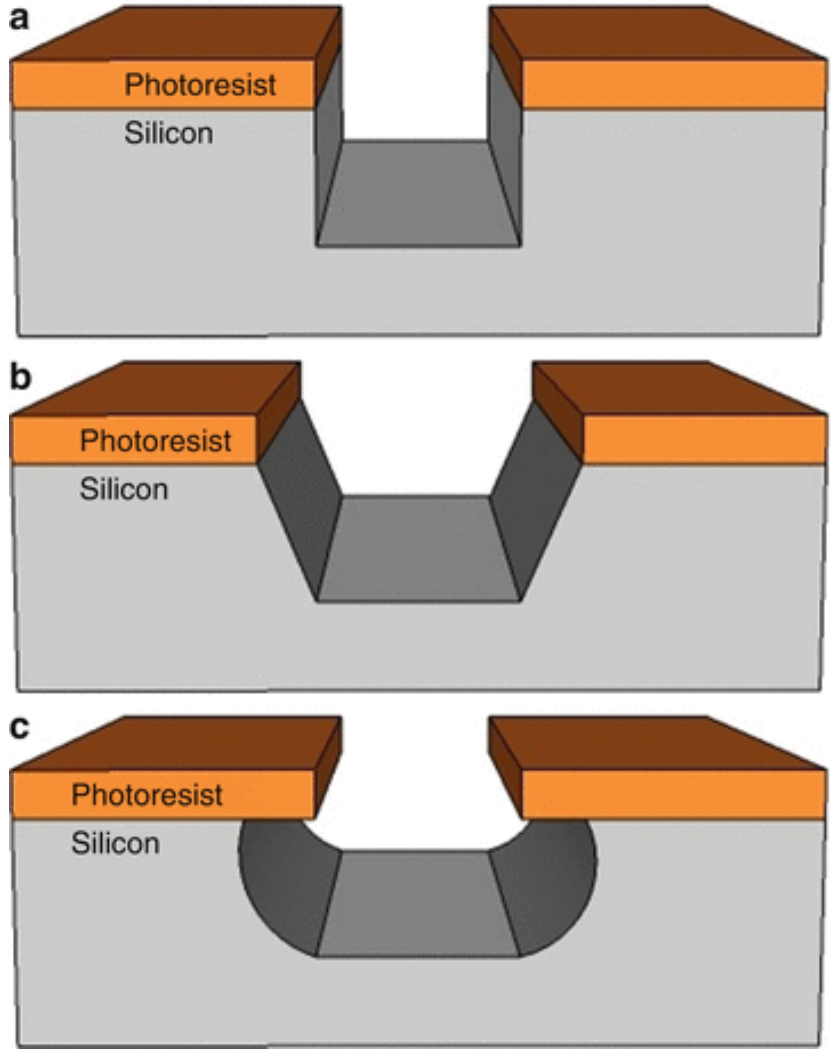
Fabrication Techniques- Etching

Two important characteristics

- Selectivity: How quickly one material is etched relative to another
- Anisotropy Ratio: How quickly material is consumed in a certain direction versus another

Two main types

- Wet Etching (Typically with acids/other wet chemistry)
- Dry Etching (Typ. Reactive Ion Etching)

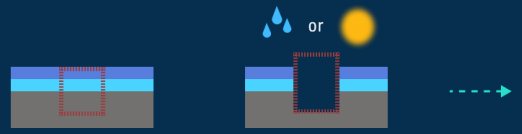


Fabrication Techniques- Etching

TOPSEIKO

Etching process overview

Etching is a crucial process in semiconductor manufacturing used to create patterns and structures. It involves selectively removing material to define circuitry and features. Etching is classified into **wet** and **dry** methods.



Wet etching is a chemical-based process where the substrate is immersed in a chemical solution called an etchant. It dissolves or etches away the exposed material uniformly in all directions. Wet etching is suitable for isotropic etching.

Dry etching is a physical-based process using plasma, a highly ionized gas. The substrate is placed in a vacuum chamber, and plasma generated using reactive gases chemically reacts with the material, removing the exposed portions. Dry etching offers precise control and anisotropic etching.

Dry etching techniques include reactive ion etching (RIE), plasma etching, and ion beam etching. These techniques allow for precise and intricate patterning required in advanced semiconductor devices. Dry etching is commonly used for achieving high-resolution patterns.

Both wet and dry etching play vital roles in semiconductor manufacturing. Wet etching is cost-effective and used for large-area patterning. Dry etching provides better control and precision for complex and fine-scale patterning.

COST EFFECTIVE / SPEED = WET ETCHING (ISOTROPIC)

PRECISION / CONTROL = DRY ETCHING (ANISOTROPIC or ISOTROPIC)

The choice between wet and dry etching depends on specific requirements. Wet etching is advantageous for simplicity and cost-effectiveness, while dry etching offers greater control and precision. The appropriate etching method is selected based on pattern resolution, device complexity, and production cost considerations. Etching enables the creation of intricate circuitry and structures in semiconductor manufacturing.

Why so many techniques

- Cost
- Throughput
- Processing Temperature (Why?)
- Film Quality (What does this mean?)

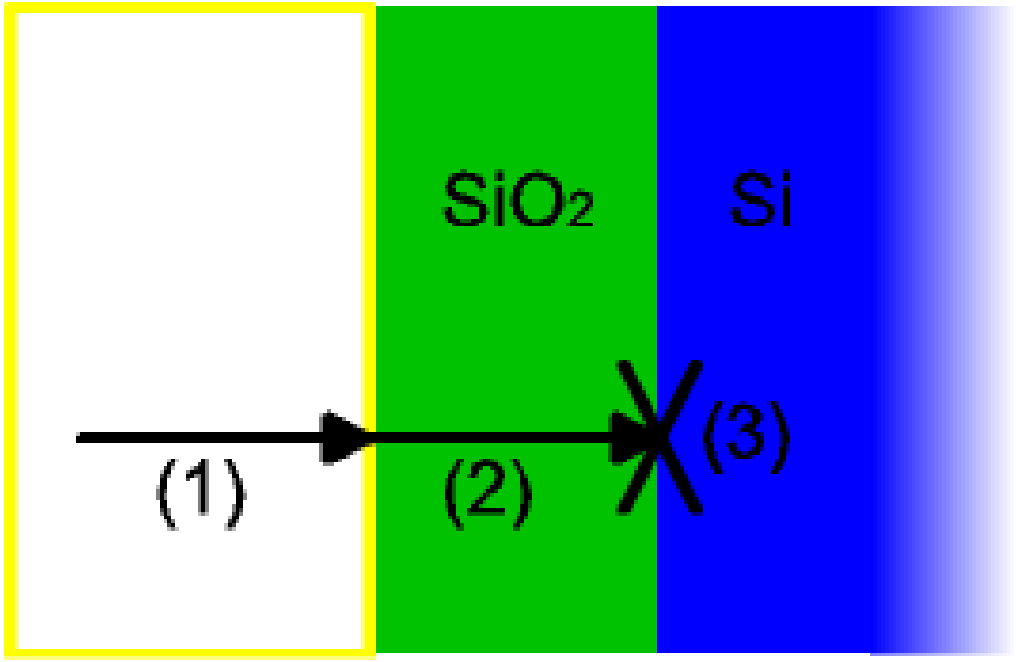
Spincoating

- Very frequent in lithography
- Must control substrate spin speed, fluid viscosity, fluid temp, etc.
- Can be very wasteful- Roughly 80% of material is flung off (non salvageable)
- Can be hardened afterwards with a hot plate, removing liquid from the wafer

Solar Cell Spincoating

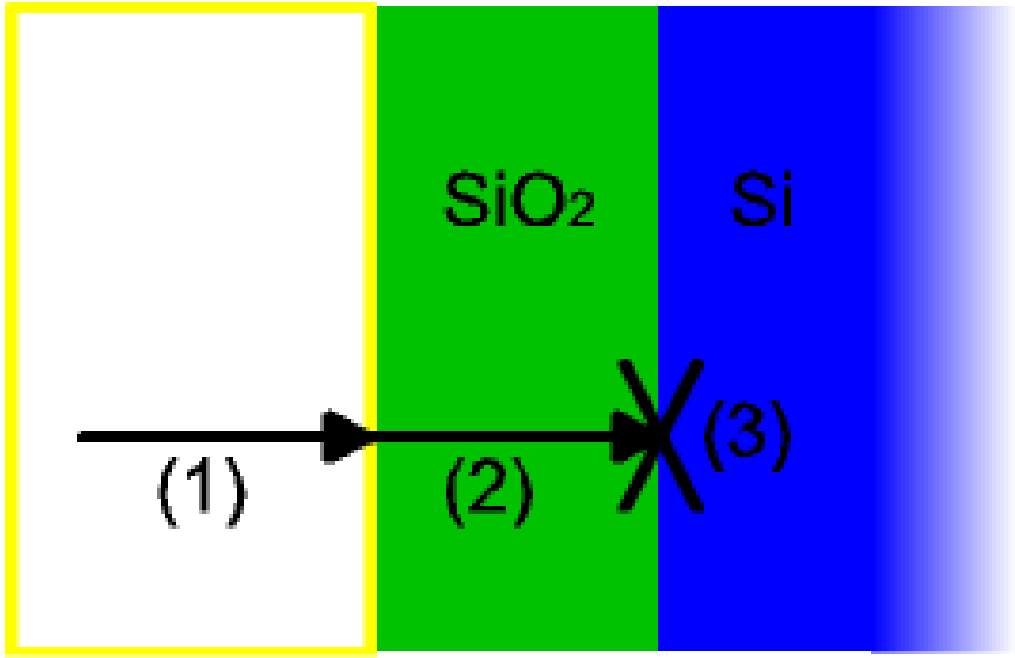
Starting Simple(?)- Oxidation

- Deal-Grove Model
  - -What does it mean to be “Rate limiting”
  - -Imagine a flow through a manufacturing plant…
- Region 1: Gas flow rate (Diffusion to surface)
- Region 2: Diffusion of medium across SiO2
- Region 3: Chemical Reaction rate w/Silicon



Starting Simple- Oxidation

- Region 1: Gas flow rate (Diffusion to surface)
  - -Volumetric Flow rate
  - -Pressure
- Region 2: Diffusion of medium across SiO2
  - -Temperature
  - -Medium of transport (What does this mean?)
  - -Crystal Orientation of Silicon
  - -Thickness of SiO2
- Region 3: Chemical Reaction rate w/Silicon
  - -Temperature
  - -Crystal Orientation of Silicon



$$J_{\text{gas}} = h_g(C_g - C_s)$$

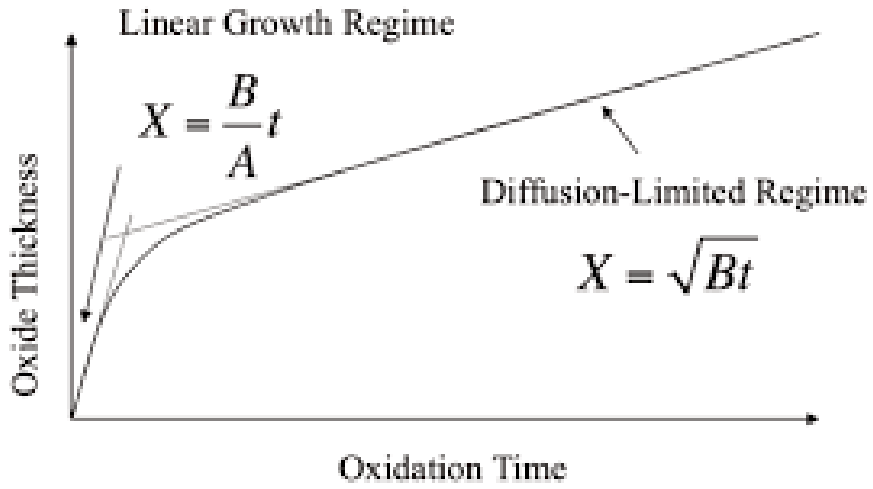
$$J_{\text{oxide}} = D_{\text{ox}}\frac{C_s - C_i}{x}$$

$$J_{\text{reacting}} = k_i C_i$$

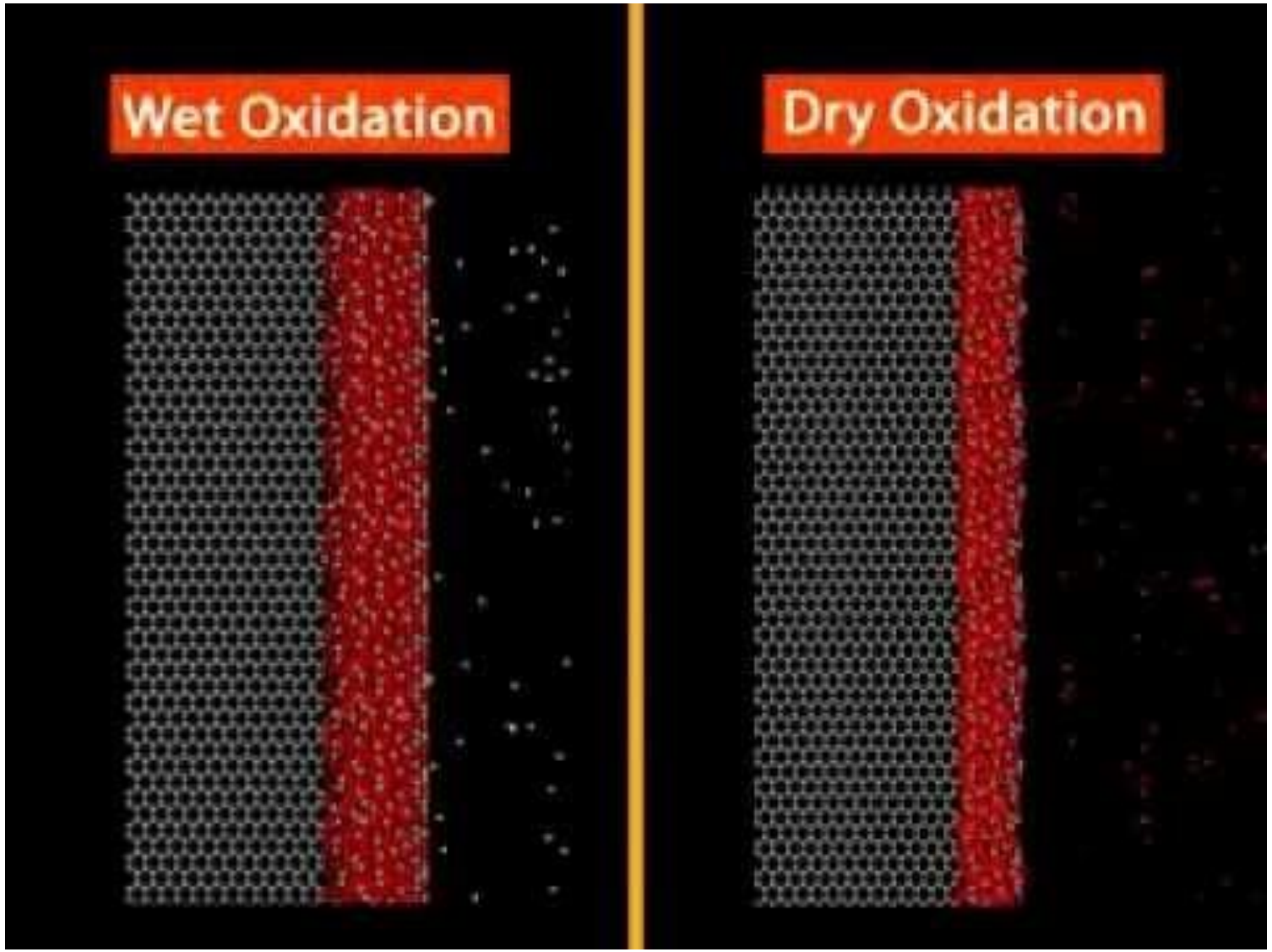
Starting Simple- Oxidation (Values at 1050C)

$$(x_0^{\,2}/B) + x_0/(B/A)) = t + tau$$

Parameter	Wet (H2O)	Dry (O2)
Linear Rate Constant (B/A), um/min	$2.95E6 * e^{(-2.05/k*T)}$	$1.04E5 * e^{(-2.0/k*T)}$
Parabolic Rate Constant (B), um^2 /min	$7 * e^{(-0.78/k*T)}$	$12.87 * e^{(-1.23/k*T)}$

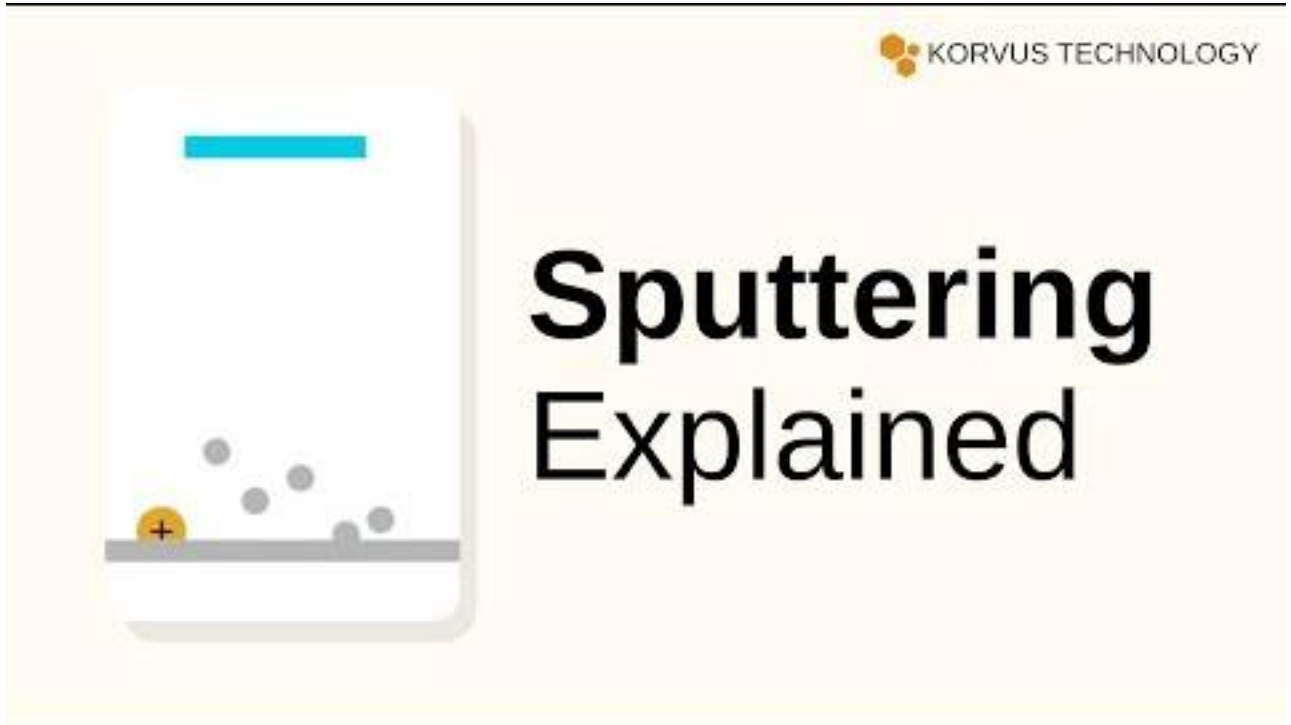


Starting Simple- Oxidation



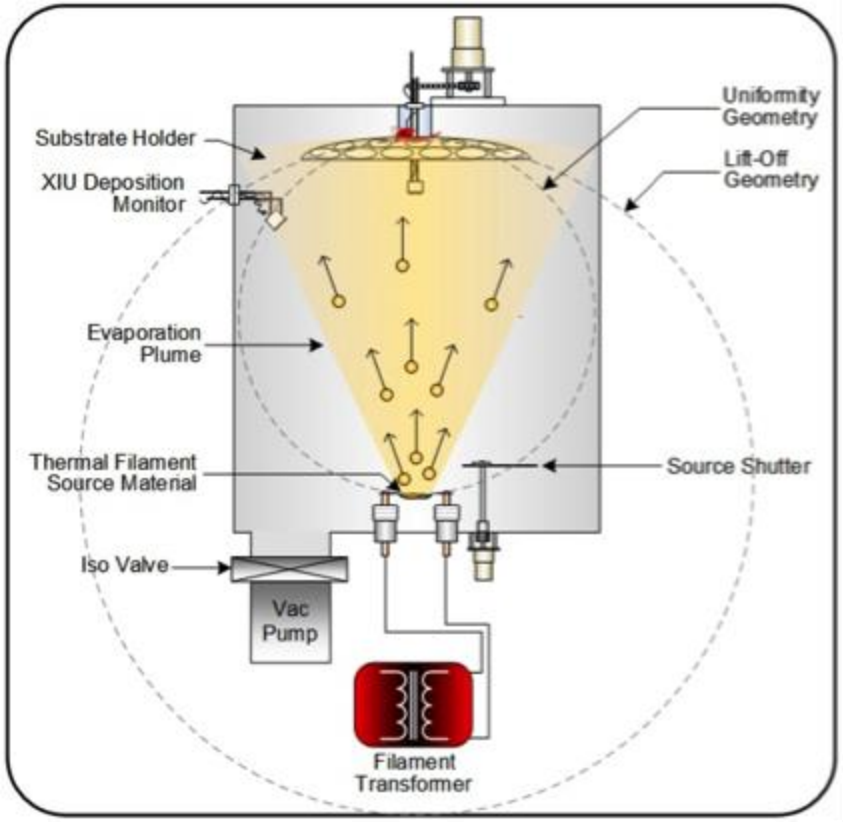
Physical Vapor Deposition (Sputtering)

- Similar to how Spray Paint works:
  -Spray small particles onto a surface.
  They'll stick to a surface and each other
- Process is greatly enhanced when performed in a plasma
- Quality is typically mediocre (at best)
- Thickness agnostic!
- Performed at low temperatures!
- Moderately speed
- Moderate Throughput (single wafer at a time)



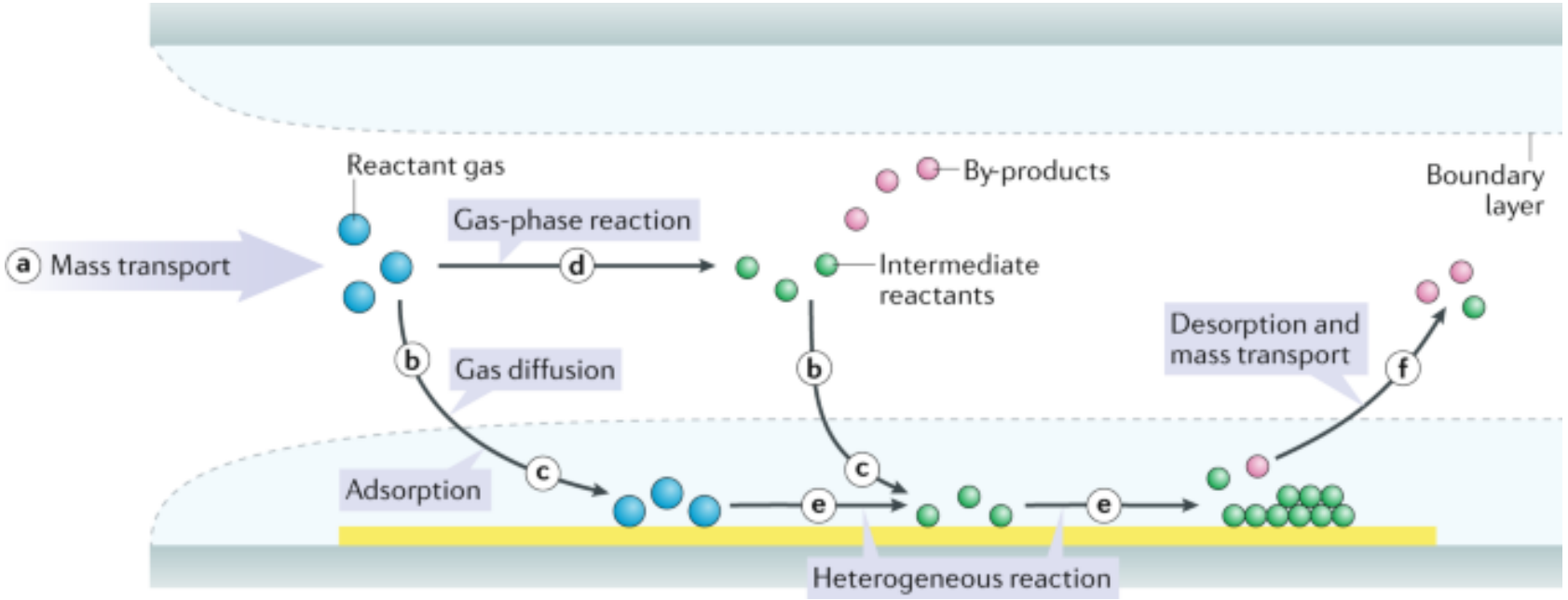
Physical Vapor Deposition (Thermal Evaporation)

- As simple as boiling and condensing…
  - Relatively low cost, but low quality films
- Imagine steam condensing on top of a pot of boiling water…



Chemical Vapor Deposition: Higher Uniformity at cost of efficiency

- CVD
- LPCVD
- PECVD
- MOCVD??
- ALD??? (More on this later)



Chemical Vapor Deposition: Higher Uniformity at cost of efficiency

- Complex gases are put in chamber w/ wafers
- Gases, or precursors, must be selected such that they react with the surface
- After reaction, byproducts are “outgassed”
- Shown Below: TEOS (Common precursor for SiO2)
  -Much faster than thermal growth

$$SiCl_4 + 4\ EtOH \rightarrow Si(OEt)_4 + 4\ HCl$$

$$Si(OC_2H_5)_4 + 2\ H_2O \rightarrow SiO_2 + 4\ C_2H_5OH$$

Chemical Vapor Deposition Processes Compared

Type	CVD	LPCVD	PECVD
Operating Temp	High (700-1100C)	Med (600-900C)	Low (100-400C)
Deposition Rate	High	Low-Med	Med
Uniformity	Medium	High	Med-High
Throughput	Very High	High	Low-Med (small batch)
Operating Cost	Low	Med	High
Equipment Cost	Low	Med	High

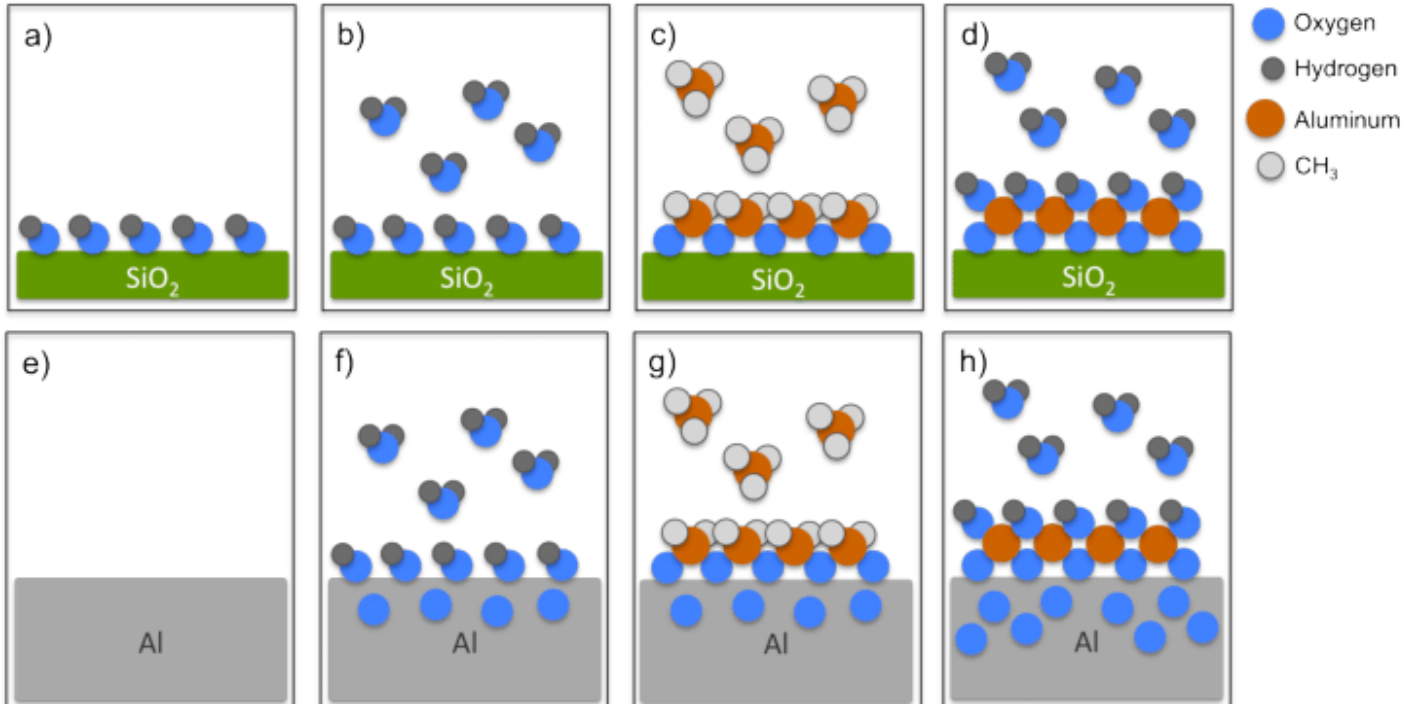
What is MOCVD?

- Metal-Organic Chemical Vapor Deposition
  -Crucial for growth in complex semiconductors (E.g. GaAs)
- Typically not used for Silicon
- Similar to ALD, enables epitaxial growth of GaAs via III-V Semiconductors
  - Can be used for GaAs lasers (Optical interconnects)

$$\mathrm{TMGa} + \mathrm{AsH_3} \rightarrow \mathrm{GaAs\ (solid)} + \mathrm{byproducts}$$

Atomic Layer Deposition

- Just a more complex form of CVD…
- More expensive due to wasted gases
- System controls need to be extremely good



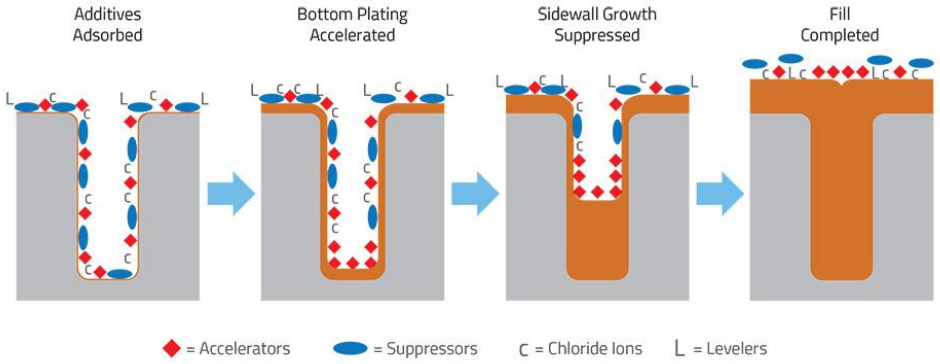
Atomic Layer Deposition

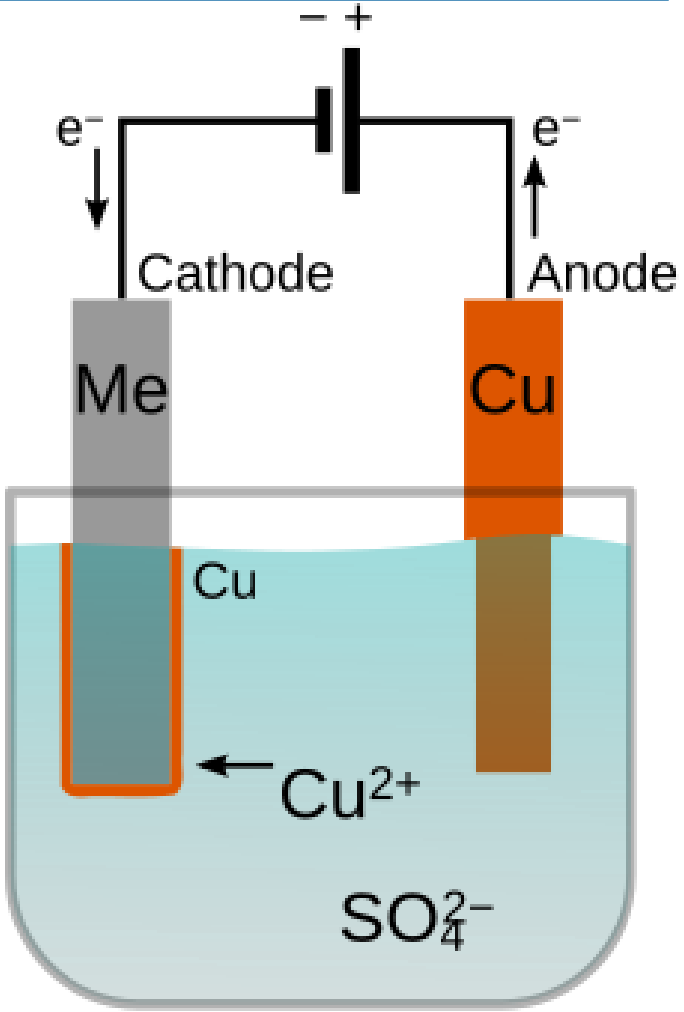
- https://www.atomiclimits.com/alddatabase/

GeO_x	$Ge(NMe_2)_4$	H_2O		Hultqvist *et al.* ADD
GeS	$Ge(\eta_2$ -((N^{t}Bu)CHMeCHMe(N^{t}Bu)))	H_2S		Kim *et al.* ADD
GeSb	$GeCl_2{\cdot}(C_4H_8O_2)$	$Sb(SiEt_3)_3$		Pore *et al.* Kim *et al.* ADD
GeSe	$Ge(N(SiMe_3)_2)_2$	$Se(SiMe_3)_2$	MeOH	Yoo *et al.* ADD
	$Ge(N(SiMe_3)_2)_2$	$Se(SiMe_3)_2$		Yoo *et al.* ADD
	$HGeCl_3$	$Se(SiMe_3)_2$		Kim *et al.* Park *et al.* ADD
GeS_x	$Ge(OEt)_4$	H_2S plasma		Ryu *et al.* ADD
	$GeCl_4$	H_2S plasma		Kim *et al.* ADD
GeTe	$Ge(guan)(NMe_2)$	$Te(SiMe_3)_2 + NH_3$		Park *et al.* ADD
	$Ge(N(SiMe_3)_2)_2$	$Te(SiMe_3)_2$	MeOH	Gwon *et al.* ADD
	$GeCl_2{\cdot}(C_4H_8O_2)$	$(SiEt_3)_2Te$		Pore *et al.* Ritala *et al.* Knapas *et al.* and 1 more VIEW ALL
	$GeCl_3H$	$Te(SiMe_3)_2$		Gwon *et al.* ADD
$GeTe_2$	$Ge(OEt)_4$	$Te(SiMe_3)_2$		Eom *et al.* ADD

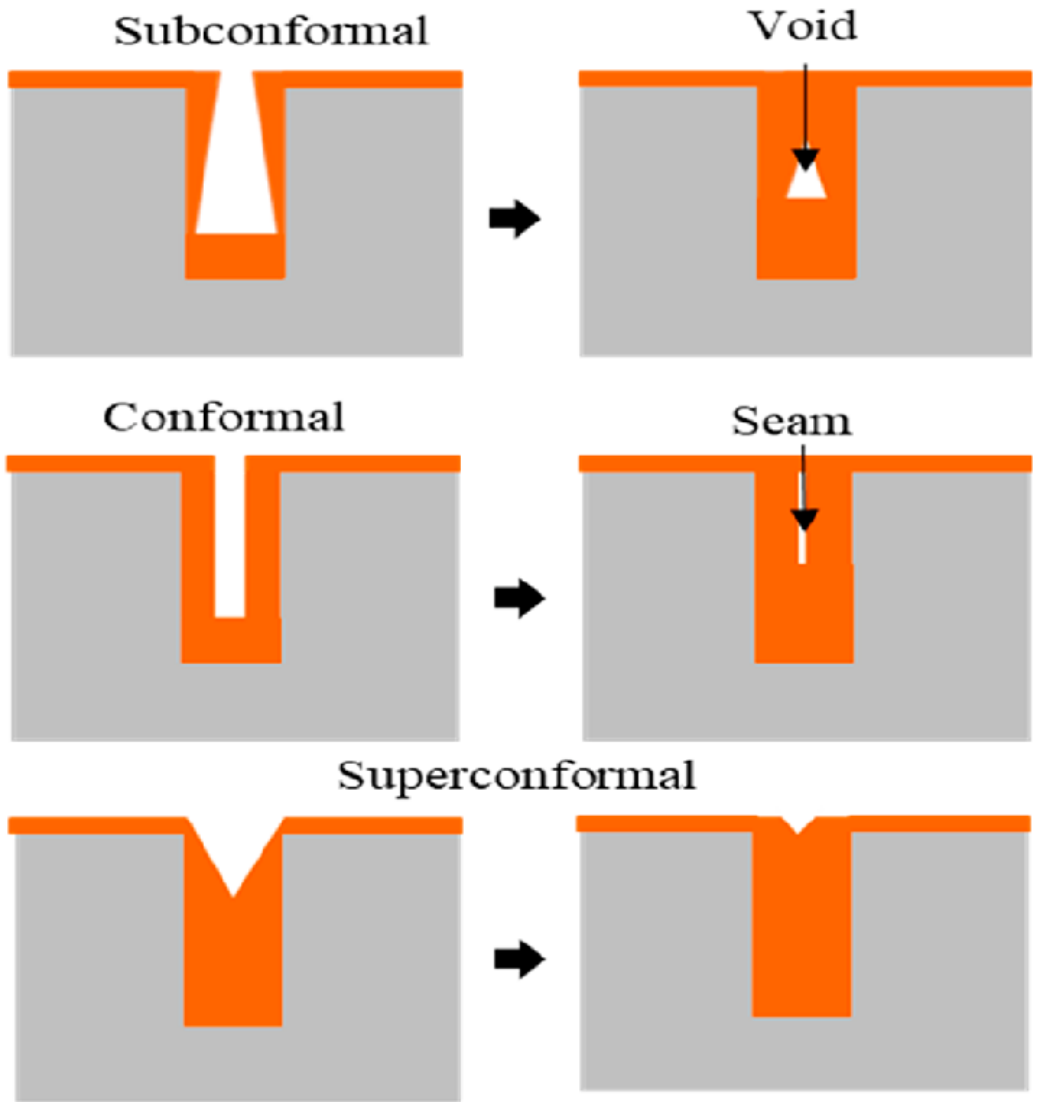
Electroplating

- Extremely common for depositing metal layers
- Utilize “Suppressors” and “Accelerator” materials to control growth rates, particularly in trenches
  - Accelerator: PolyEthylene Glycol (PEG)
  - Suppressor: 3-sulfapropyl disulfide





Electroplating



The End

Thanks for listening!

GBM Attendance