# Fine Pitch Flip Chip Technology

Eric D. Perfecto, IBM Research
EPS Distinguished Lecturer
Eric.Perfecto.us@IEEE.org

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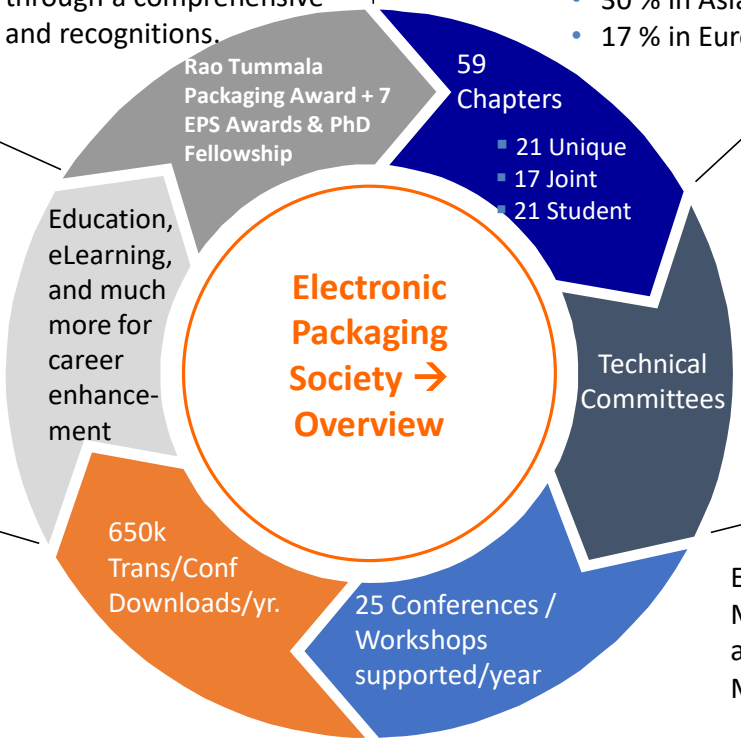


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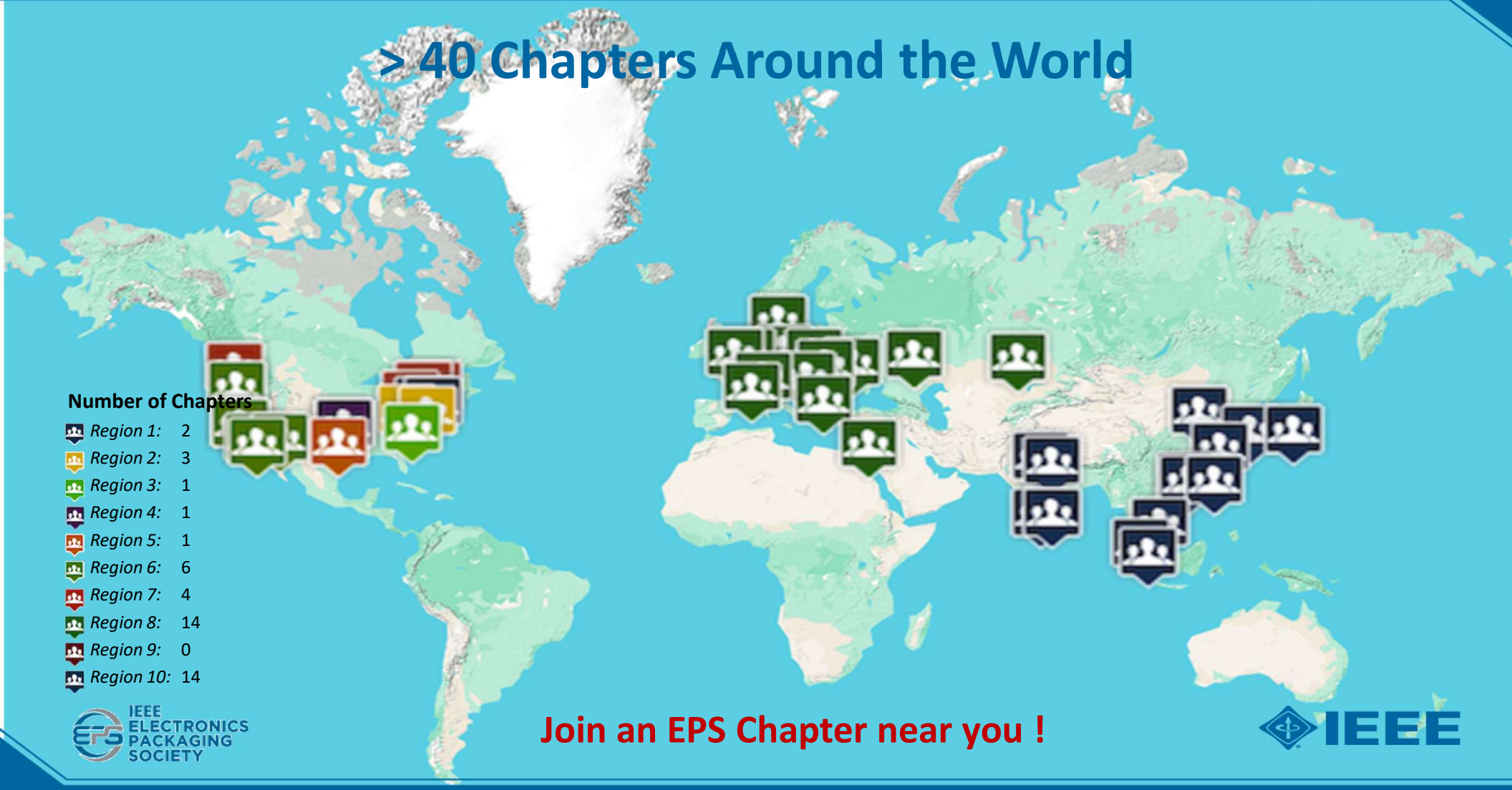


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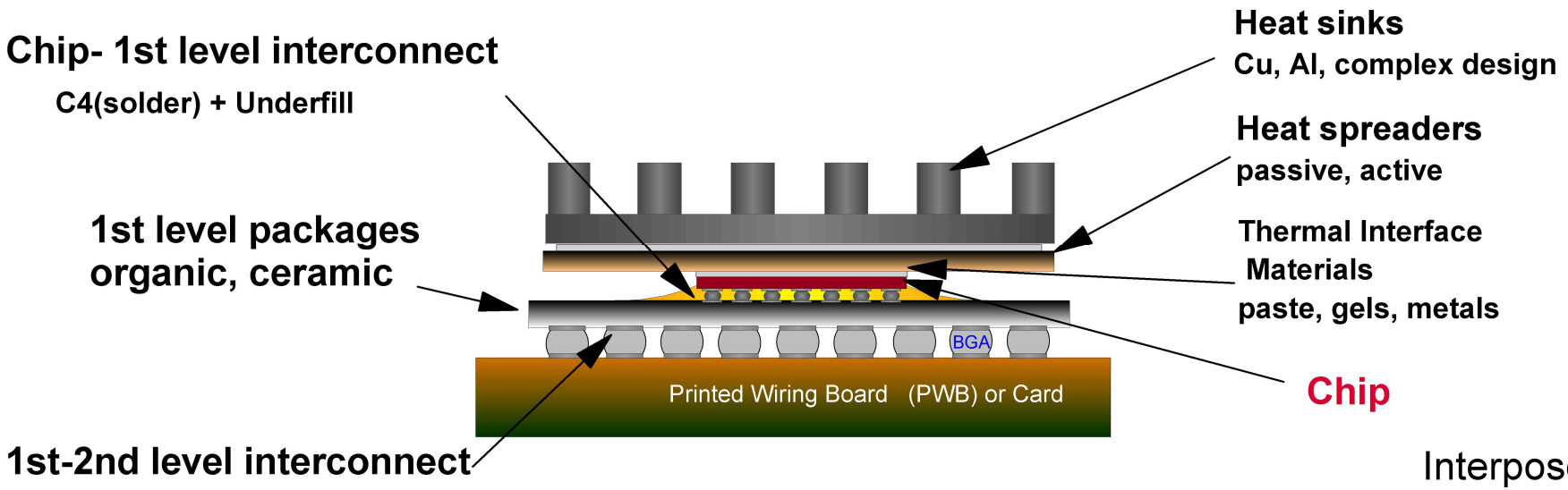
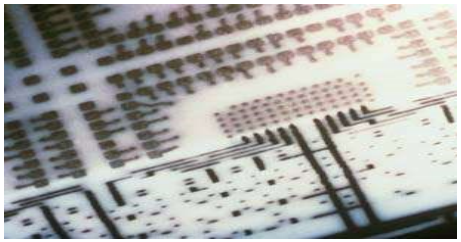
# 1st & 2nd Level Packaging Technology Elements

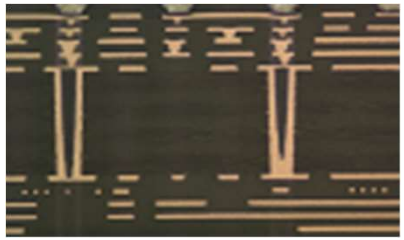



**Chip Carrier Options:**

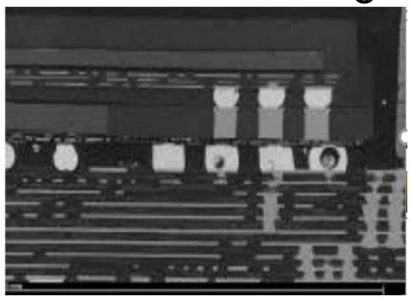
Ceramic



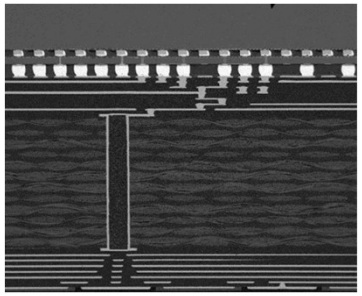
Laminates



Wafer Level Pkg



Interposer + Laminate



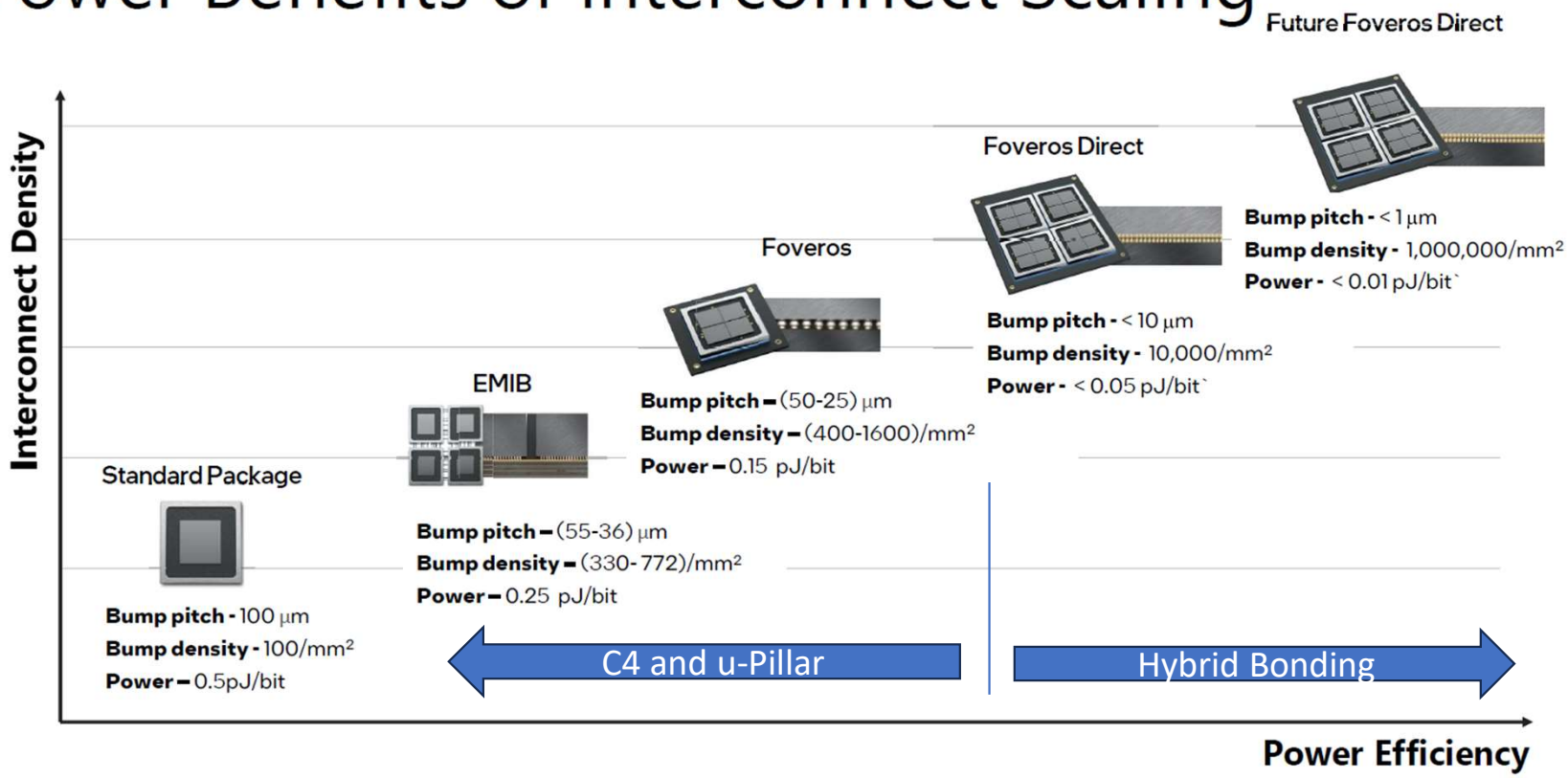
## Agenda

- Part 1: u-Pillar Design and Fabrication
- Part 2: u-Pillar Assembly Processes and Applications
- Part 3: Applications: Assembly / Structure Options

# Part 1: u-Pillar Design and Fabrication

# Impact of Pitch Reduction

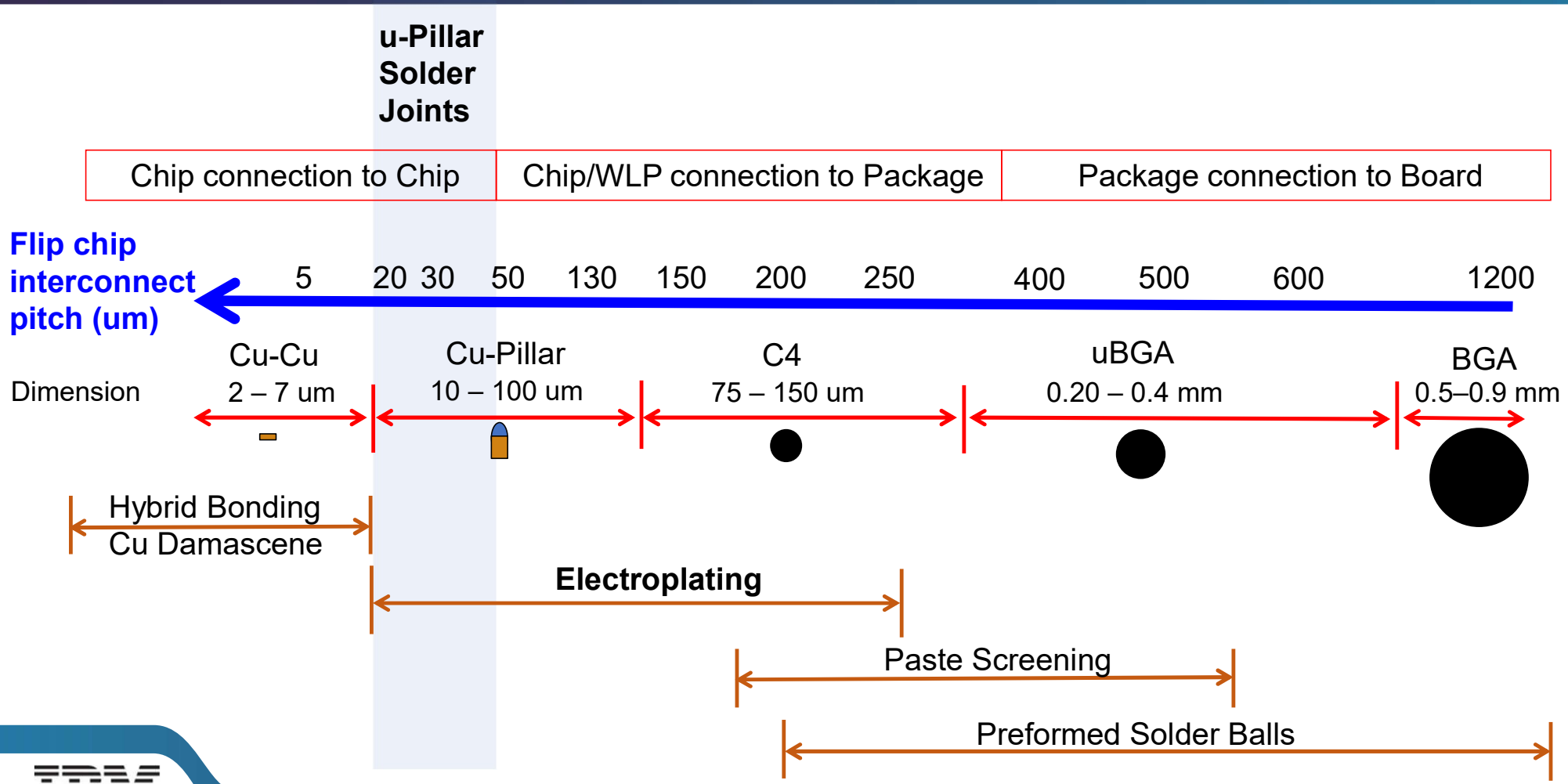
## Power Benefits of Interconnect Scaling




Source: Intel Internal Projections

Presented at ECTC 2024 HIR Session

# Packaging Interconnect



# Cu Pillar Technology

## Lead Free Solder Bump Assembly

- Large Pitch (> 110um with exceptions)
- Historically Large Die, now all sizes
- Bump Shape is not Customized
- Use **Mass Reflow Assembly**
- All application

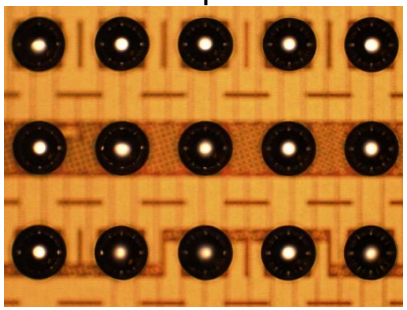
## Cu Pillar Bump Assembly

- High-density bump / pitch (55 - 100um)
- Some customized bump shape
- Mass Reflow or Thermal Compression Assembly
- On High-end with Si on Si or WLFO
- Allows for **Capillary underfill**

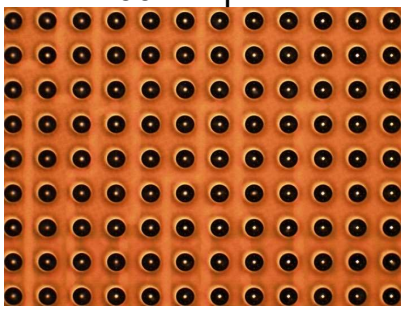
## u-Pillar Bump Assembly

- Very high-density bump / pitch (15 – 40um)
- Mostly Smaller Die but no Limited to it
- **Fluxless Thermal Compression** Assembly or NCP
- On High-end with Si on Si or WLFO w/Bridge

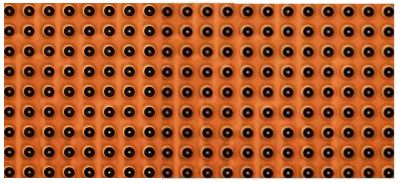
C4: 150 um pitch

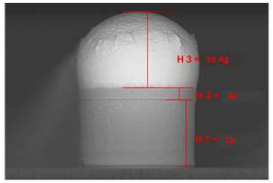


Pillar: 60 um pitch



u-Pillar: 30 um pitch

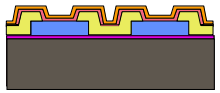
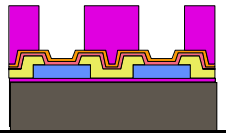
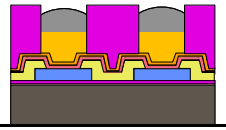
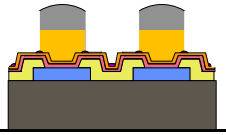
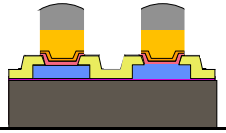
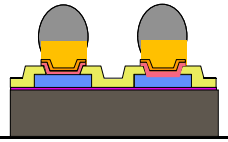


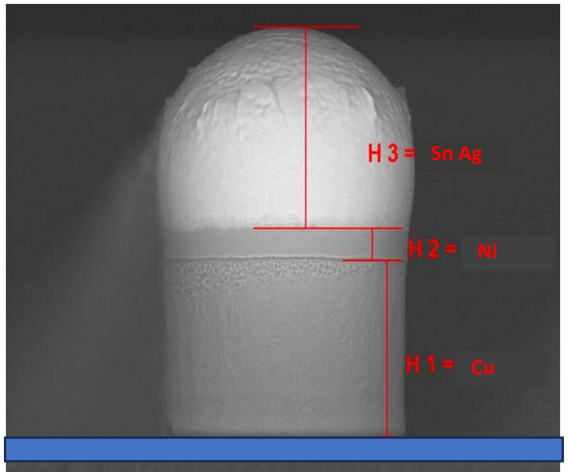
u-Pillar: 2011 ➔ Future

u-Pillar: 30 um pitch

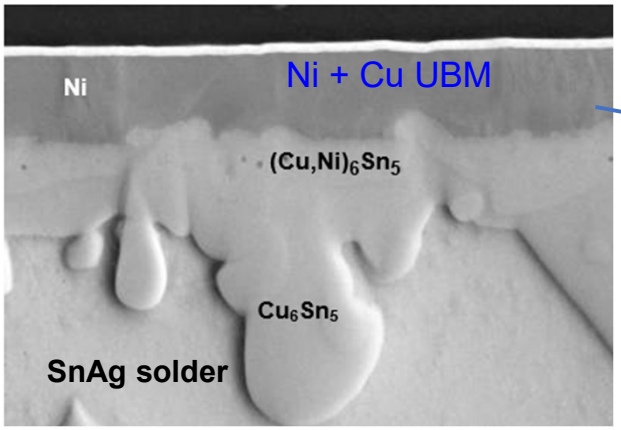
# Pattern Electroplating Process

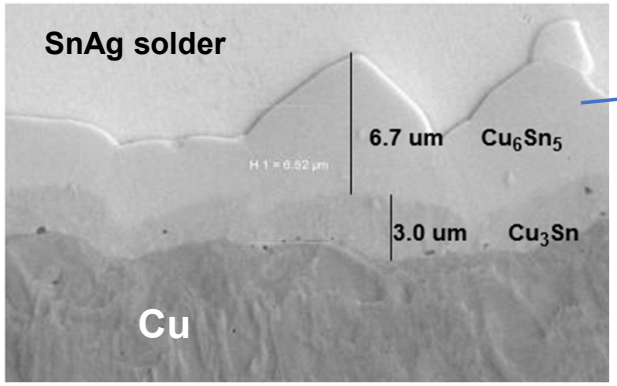
| Electroplated Pb-free Process | |
|---|---|
| Bake/ Sputter Clean / Sputter Seed<br>TiW / Cu or Ti / Cu |  |
| Spin Resist Apply<br>+ Expose + Develop<br>+ O2 Plasma |  |
| Cu Pillar / SnAg or Ni / SnAg<br>Cu / Ni / Cu / SnAg |  |
| Resist Strip: Aqueous or Solvent |  |
| Cu Etch<br>TiW or Ti Etch<br>+ O2 Plasma |  |
| Reflow<br>- Flux / Belt Furnace / Clean<br>or Formic Acid Reflow (Fluxless) |  |

Cu-Pillar – Post Reflow

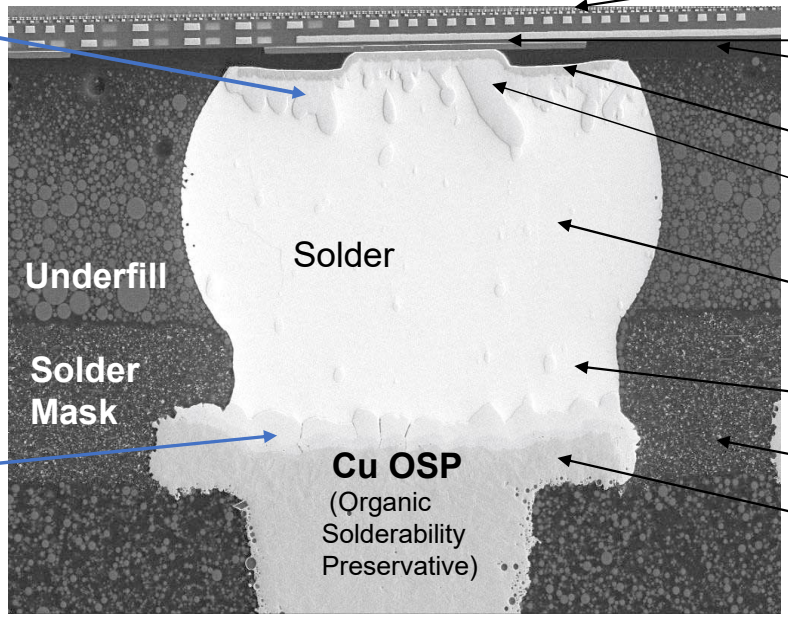


# Solder Connection and Intermetallic




**C4 = Controlled Collapse Chip Connection**




BEOL Chip Wiring

Far BEOL (Al +PSPI)

Polymer Cushion

**Under Bump Metallurgy**

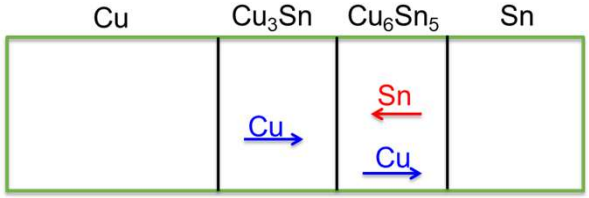
Intermetallic

**C4 Solder**

Laminate pre-solder

Solder mask

Laminate Pad/wiring



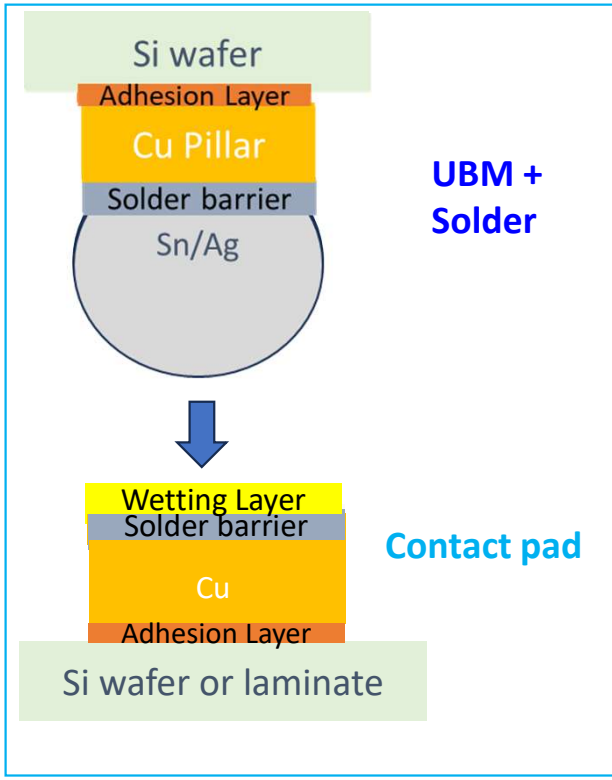

With Ni UBM the formed IMC is $Ni_3Sn_4$

# Under Bump Metallurgy (UBM) Function

- UBM provides the connection between the device and the solder, and between the solder and the chip carrier.

- UBM layers unique functions
  - **Adhesion Layer** – Provides adhesion to Polyimide and $SiO_2$/SiN:
    - Ti, TiW, Cr (+ Cu seed layer)
  - **Current Carry Layer** – Distributes the current from via to solder
    - Cu (Pillar)
  - **Solder Barrier Layer** – Creates the solder metallurgical connection:
    - Ni, NiFe, Co, CoFe, NiCo, CoW or just Cu-Pillar
  - **Wetting Layer (contact pad)** – Provides solder wetting
    - Au, Pd/Au, Sn, Cu (on Ni UBM) or just Cu-Pillar

- Main fabrication Methods: Barriers:
  - **Pattern electroplating** Ni, Cu, CoX, NiX
  - **Electroless Deposition** Ni(P)



# Issue in Flip Chip Fabrication

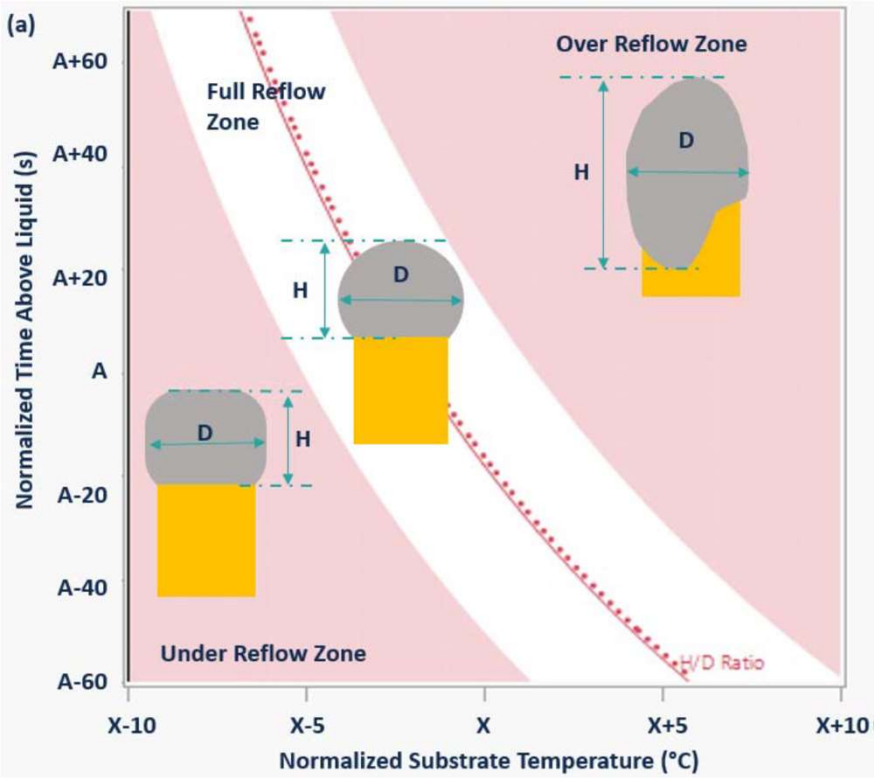
u-Pillar structure requires optimization to address the following issues:

- Sidewall wetting during reflow and assembly
- Sn Whiskers
- IMC voids:
  - Kirkendall voids
  - Volume reduction voids
- Ag3Sn Plates

# Fluxless Reflow and Solder Wicking (Sidewall Wetting)

**Fluxless reflow process**:

➔Heat to T1 (160 – 190C)
➔Vacuum Chamber
➔ Introduce Formic Acid
➔ Vacuum Chamber
➔ Backfill with N2
➔ Heat to T2
➔ Cool to RT




Fluxless reflow is the preferred method so that time at melting temperature is minimized.

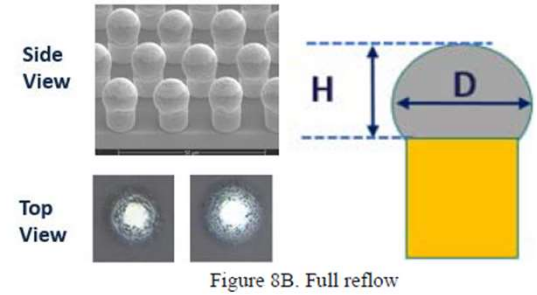


Figure 8B. Full reflow

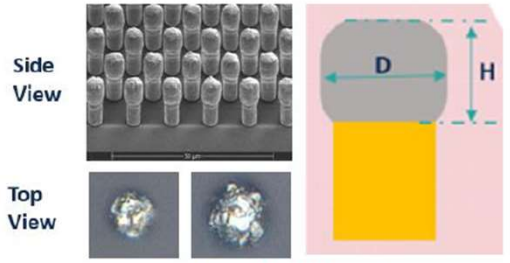


Figure 8C. Under Reflow

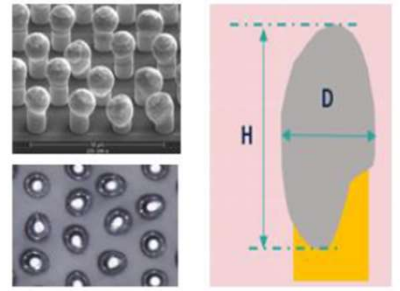


Figure 8D. Over reflow

*L. Jing, et.al, "Impact of Process Parameters on Vacuum Fluxless Solder Reflow," 2023 ECTC*

# Sn Whiskers in Sn/Cu System

Sn Whiskers are more common on small volume solder components and not on traditional C4.

First observed on surface mount technology where Cu leadframes are joined a layer of solder on the printed circuit boards. This thin eutectic Sn–Cu or matte Sn surface layer enhanced wetting during joining.

Spontaneous Sn whiskers requires both stress generation and stress relaxation. Grain boundary precipitates of $Cu_6Sn_5$ induce a volume increase and compressive stress in Sn. The relaxation occurs by the removal of atomic layers of Sn normal to the stress. These Sn atoms can diffuse along grain boundaries to the root of a stress-free whisker to feed its growth

Grain boundary fluid flow model predicts the rate of Sn whisker growth.

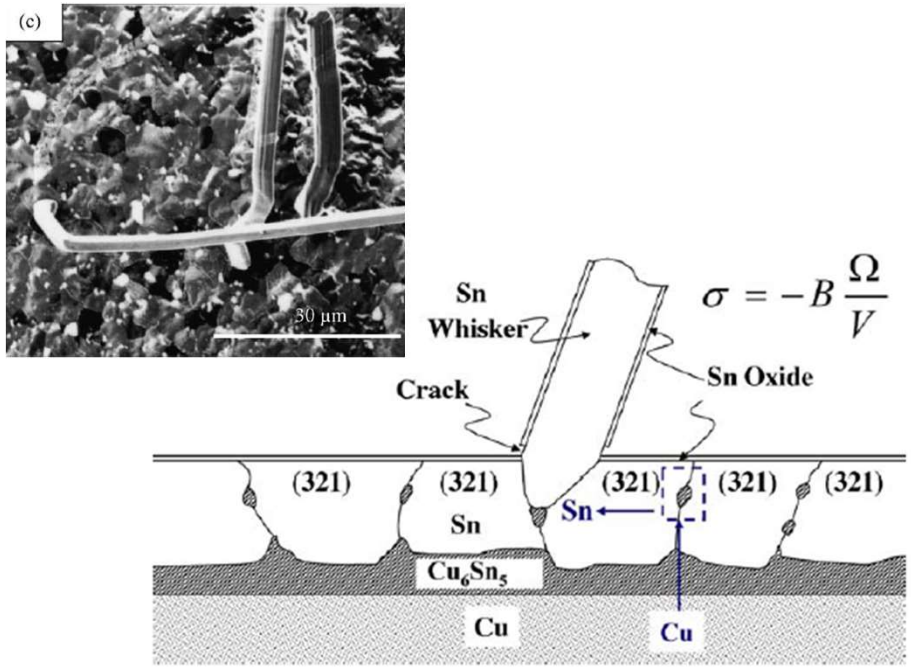
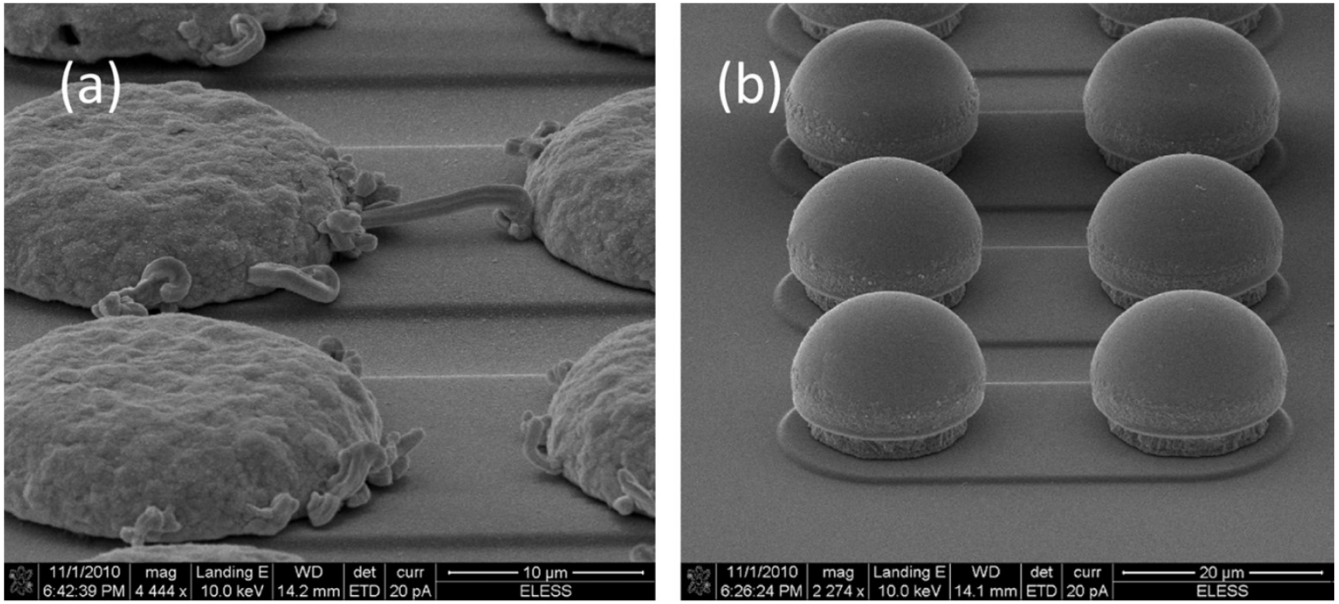



Fig. 5. Schematic diagram of the cross-section of a whisker on a layer of eutectic Sn–Cu finish which contains the $Cu_6Sn_5$ precipitates. The surface of the finish and the whisker has oxide, except the root of the whisker where the oxide is broken. From the broken surface, vacancies can diffuse in and enables Sn atoms to diffuse. The diffusion of Cu into the volume $V$ will expand the volume and generate a compressive stress.

*K.N. Tu, J.C.M. Li / Materials Science and Engineering A 409 (2005) 131–139*

# No Sn Whiskers in Ni UBM




(a) SEM image of a Sn whisker between two Cu bumps having a top layer of Sn, the whisker is a short. (b) shows no Sn whisker when a Ni layer was added between the Cu bump and the top layer of Sn.

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*K.N. Tu, Y. Liu / Materials Science & Engineering R 136 (2019) 1–12*

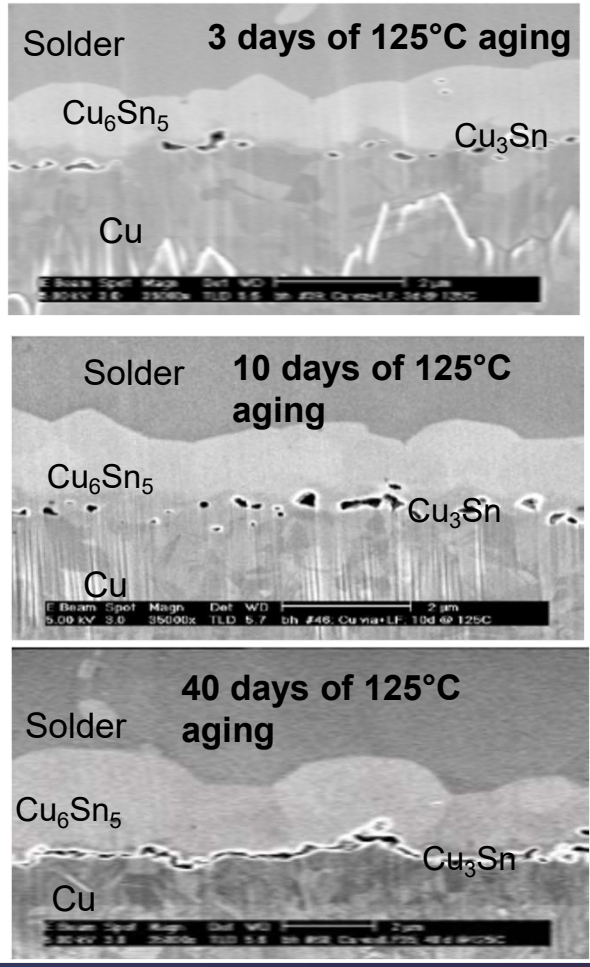
# Kirkendall Voids and Other Voids

**Kirkendall Voids - Mechanism 1:**

- At joining $Cu_6Sn_5$ intermetallic crystallizes, along Cu layer, stopping further dissolution of Cu.
- Also, a thin intermetallic layer $Cu_3Sn$ forms between Cu and $Cu_6Sn_5$.
- During thermal aging, atomic vacancies are left by Cu atoms migration from the Cu side – which are not filled by the Sn atoms.
- These vacancies coalesce into the so called Kirkendall voids at Cu - $Cu_3Sn$ interface, and in $Cu_3Sn$ compound layer.

**Impurities - Mechanism 2:**

- Impurities in the plated Cu migrate to the Cu grain boundary and upon IMC formation generate voids. This can be aggravated by increased Cu current density at plating




*Tz-Cheng Chiu, et. al., 2004 ECTC*

# Kirkendall Voids Mitigation Strategies

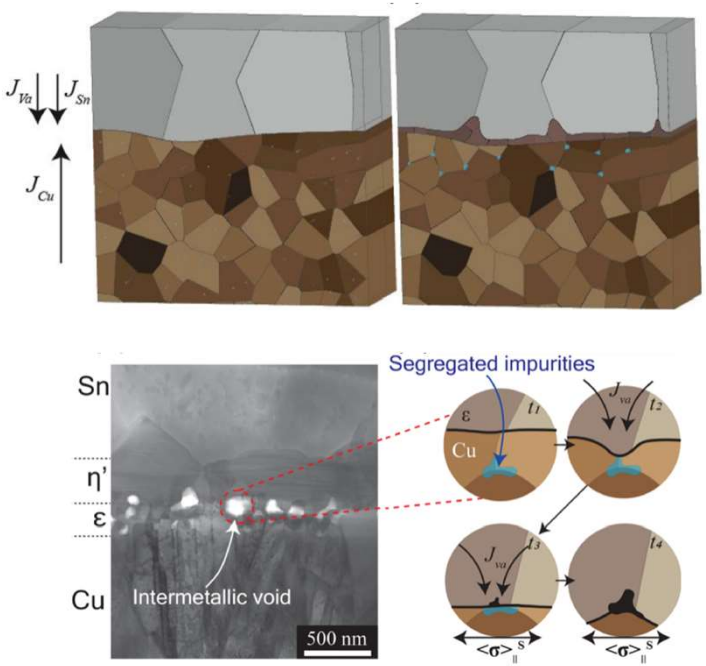
Interfacial Kirkendall voids can be mitigated by various methods:

1. Inhibiting the growth of the interface $Cu_3Sn$ layer, and even eliminating the $Cu_3Sn$ phase, such as Zn, Pd, Fe or Ag solder additives.

2. Eliminating/reducing impurity elements (such as S) by adding sulfide-forming elements, such as Zn, Mn, Cr or Fe in the Cu plating chemistry.

3. Reducing the Sn interdiffusion at Cu interface through Cu nanotwin
 - by reducing Cu deposition rates

4. Replacing terminal metal from Cu to Ni, eliminating the $Cu_3Sn$ and $Cu_6Sn_5$ IMC formation.




*Ross, 2019*

*J. Wang, et. At, J Advanced Joining Processes 6 (2022), Forming mechanism and growth of Kirkendall voids of Sn/Cu joints for electronic packaging*

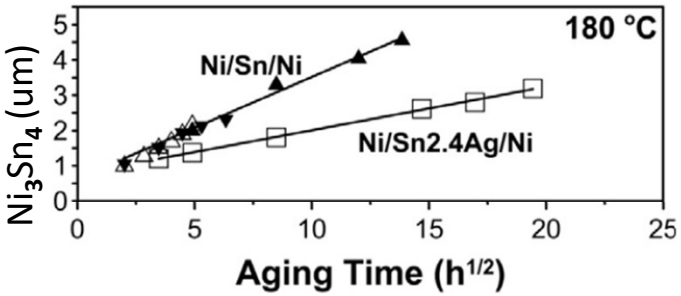
# Elimination of voids in Ni / Sn / Ni System

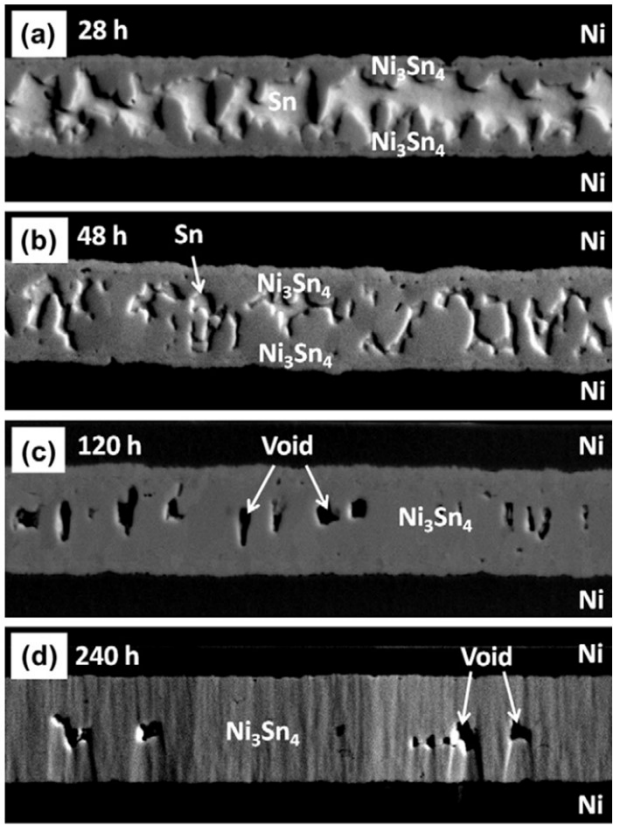
**Mechanism:**

- Volume reduction voids during the $Ni_3Sn_4$ IMC formation concentrate at the bonding interface.

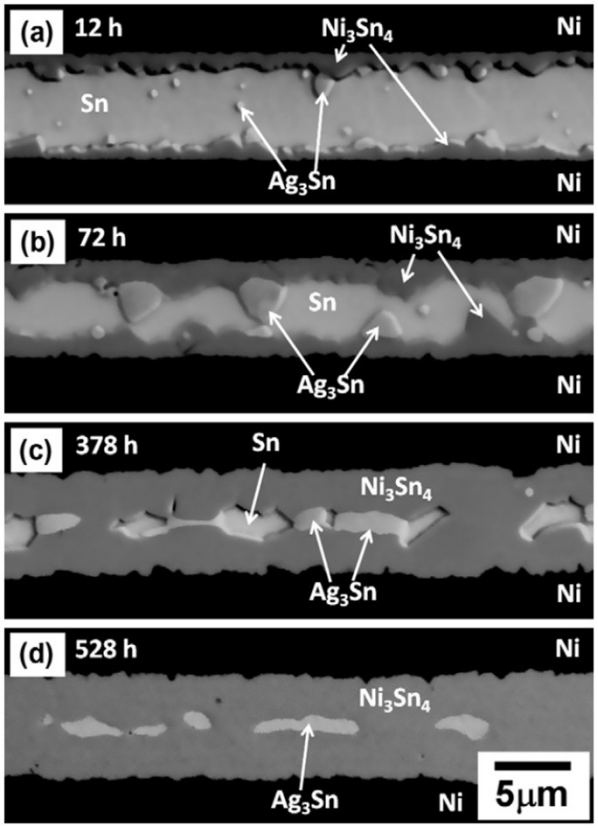
**Solution:**

- Adding Ag in the solder slows the IMC formation allowing $Ag_3Sn$ to aggregate at the bonding interface.




Ni/Sn(7 um)/Ni




Ni/Sn2.4Ag(7 um)/Ni

H.Y. Chuang, *et al,* Elimination of voids in reactions between Ni and Sn, Scripta Materialia 66 (2012)

# $Ag_3Sn$ Plates at Reflow on Flip Chip

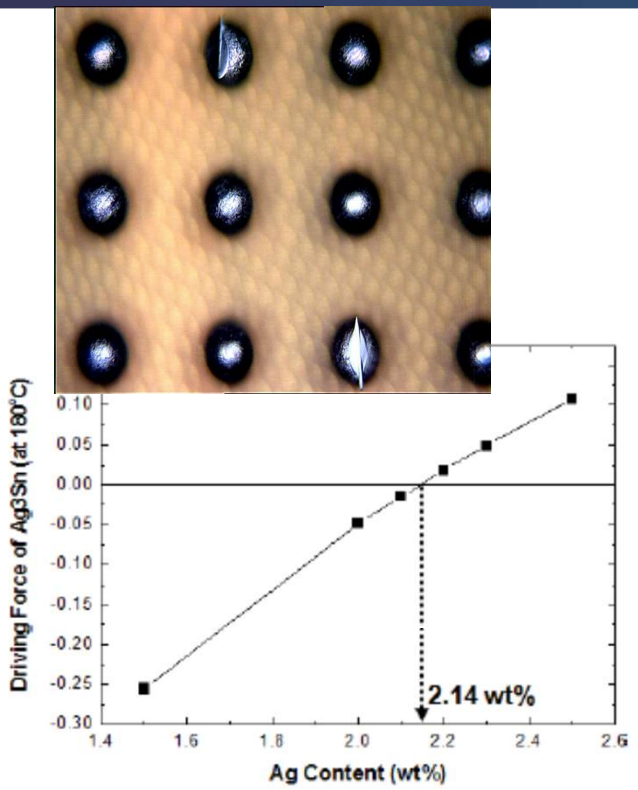



**Figure 6. The calculated driving force of $Ag_3Sn$ IMCs in the supersaturated liquid at 180°C as a function of the Ag content in the liquid.**

- $Ag_3Sn$ plates tend to first form next to the base $Cu_6Sn_5$ probably aided by the energy released during IMC formation.
- Rapid formation of $Ag_3Sn$ attains saturation during solid state reaction with no further growth on subsequent thermal processes.
- However, upon further reflows, the $Ag_3Sn$ plates will migrate towards the solder surface

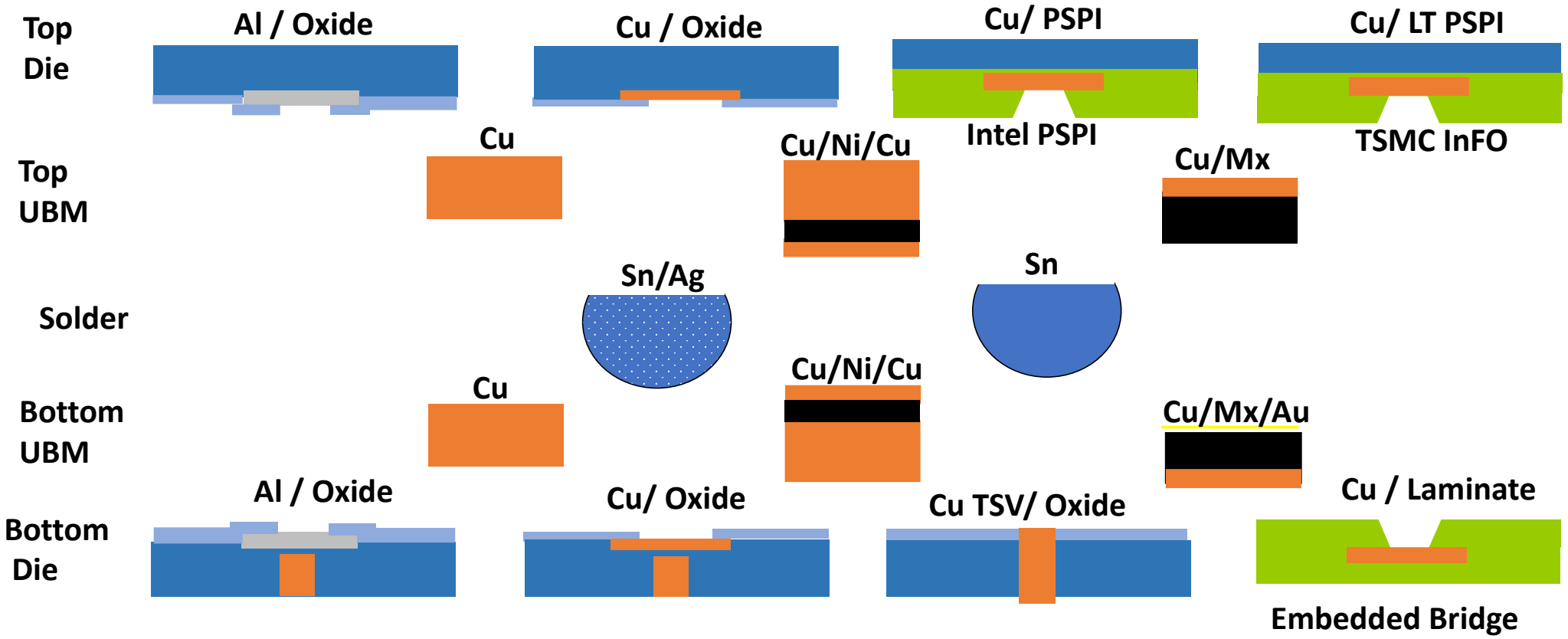
**Two options on reducing the $Ag_3Sn$ plates:**

1) Keep max %Ag to less than 2.1% in Sn
2) Increase the reflow cooling rate

*Moon Gi Cho, et. al., 2012 IMAPS*

# Part 2: u-Pillar Assembly Concepts and Chip Joining Issues

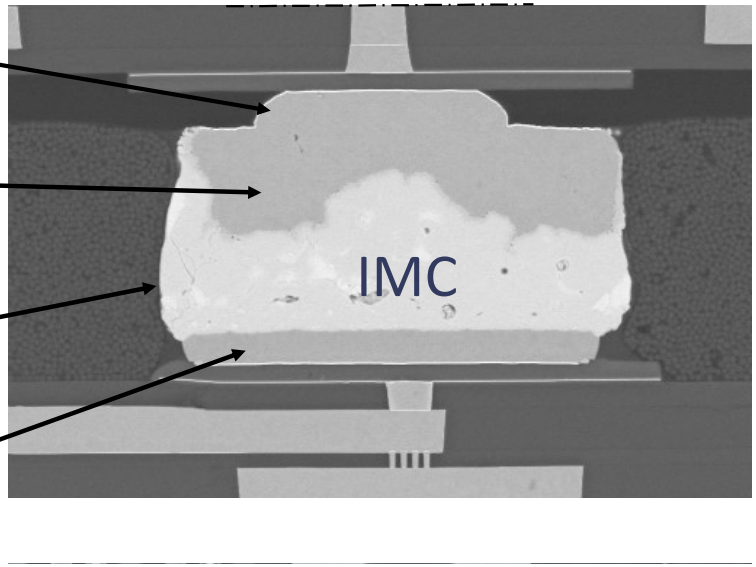
# u-Pillar Interconnects: Si-to-Si Structure Options



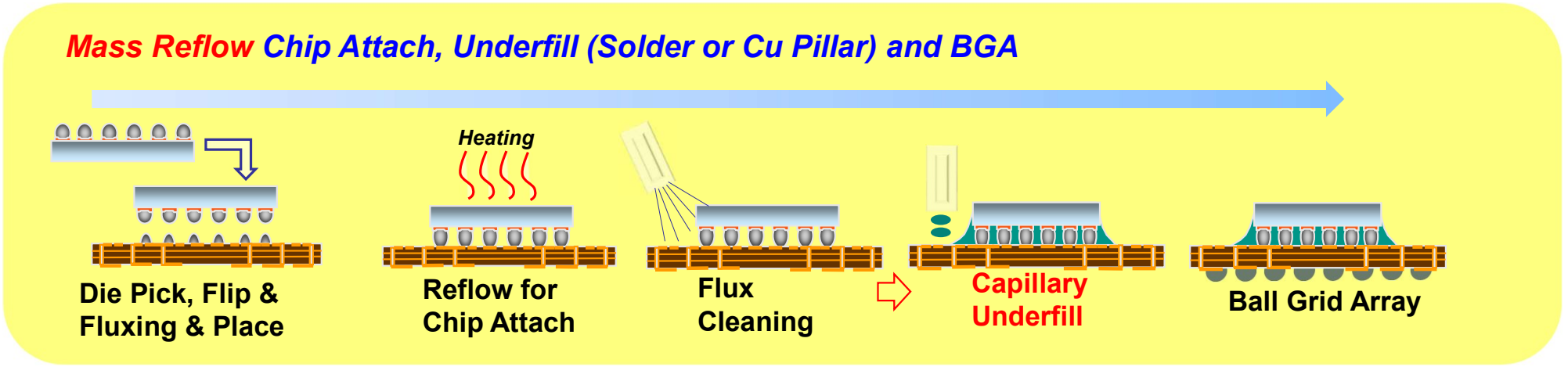

Mx = Ni, NiFe, Co, CoFe, NiCo - Goal is to minimize the IMC thickness

# Pillar Joining (to Interposer) Elements

- **FBEOL**
  - Al vs BEOL Cu
  - PSPI vs SiO2/SiN
- **Top Chip**
  - Cu Pillar
  - UBM: Ni vs Ni/Cu vs Cu
  - Solder volume control
- **BA**
  - Thermal Compression Bonding (TCB)
  - Flux and flux clean, or Fluxless
  - Solder ➔ IMC
  - Underfill material (% fillers)
- **Bottom pad**
  - Ni/Au vs Ni/Cu vs Cu-Pillar
  - F2B vs F2F



# Traditional Flip Chip Assembly




**Package > Chip**
**The package is built independent of the chip**

## FC-BGA

- FC-BGA initially had one chip and some capacitors but has evolved to multi-chip applications enabling **System-in-Package (SiP)**.
- Underfill allows for mechanical integrity of the solder interconnect (Chip/Laminate : CTE 2.7/16ppm).

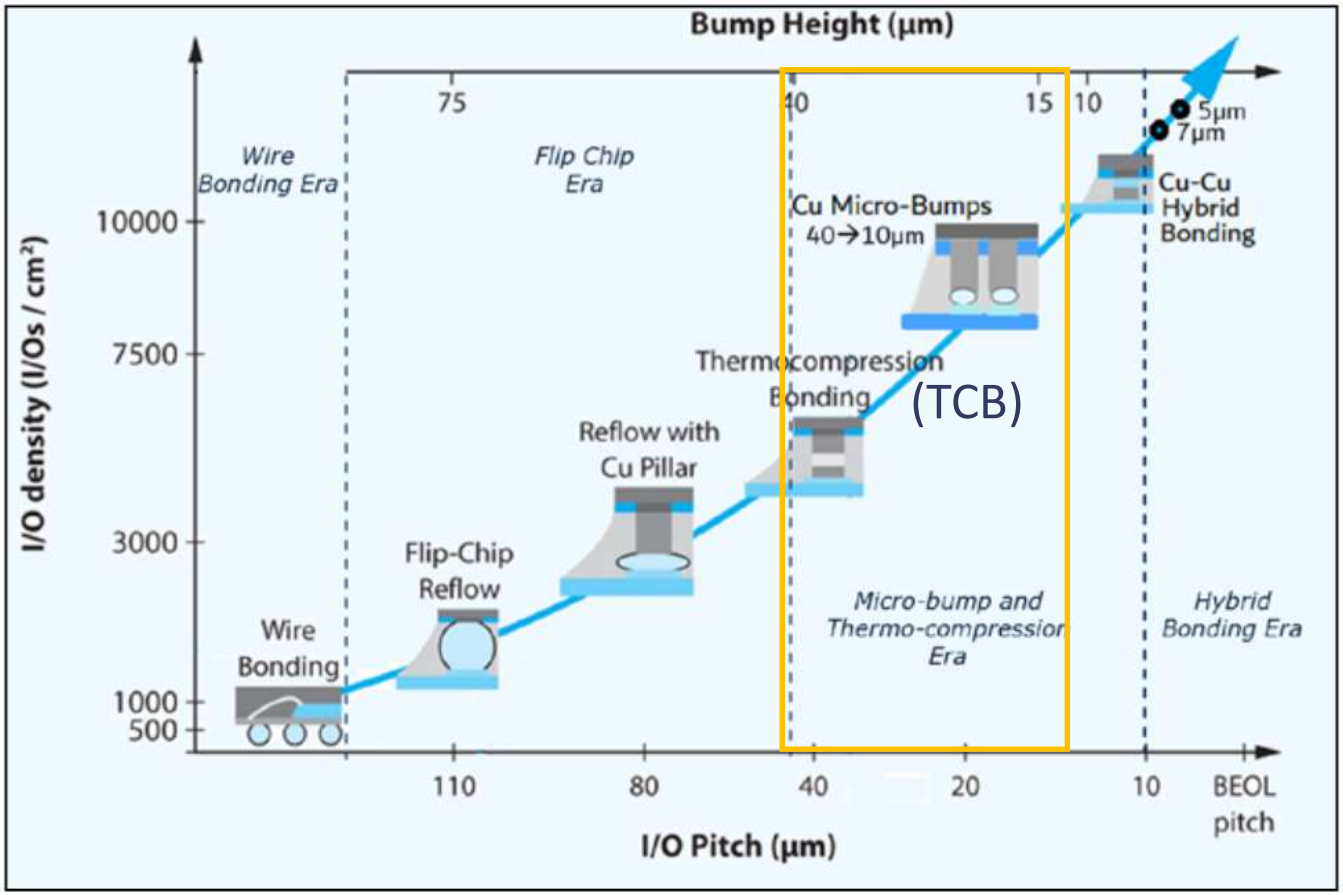
*S. Wen, Flip Chip Interconnect Course, 2023 ECTC*

# The Thermal Compression Bond (TCB) Era

**TCB Era:**

- Chip to Laminate
- Chip to Chip
- Chip to Interposer
  - Chip to wafer
  - Chip to RDL
- Chip to Bridge
  - WLFO
  - EMIB

TCB is needed for improved fine-pitch chip alignment

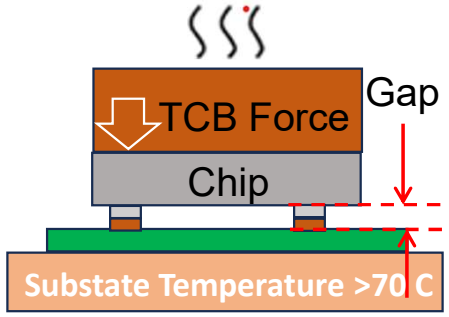


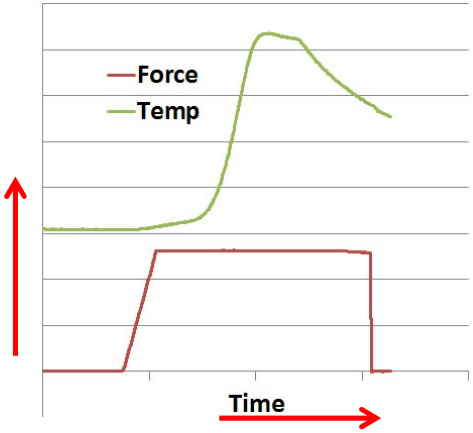

*Rao Tummala, et. al, 2023 March • April Chip Scale Review*

# TCB Process Control Parameters

TCB significantly improves alignment and reduces the die joining stresses since the laminate cooling occurs from relatively low temperature.

TCB Head temperature > 300C

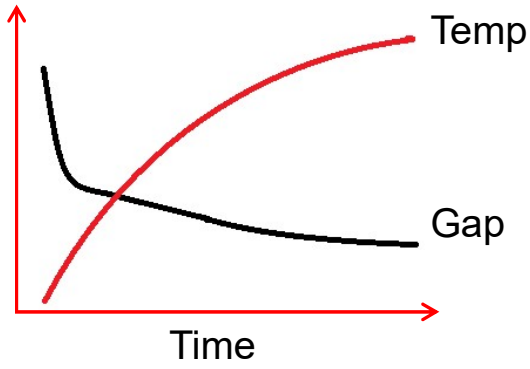


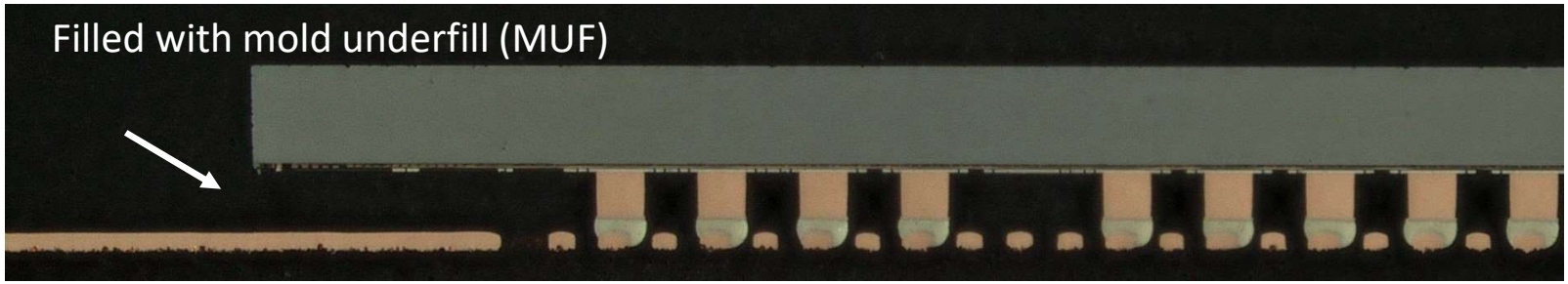

**(1) Force** control: set the pressing force as the control parameter to achieve needed joint profile. Pressure change indicated melting of solder.

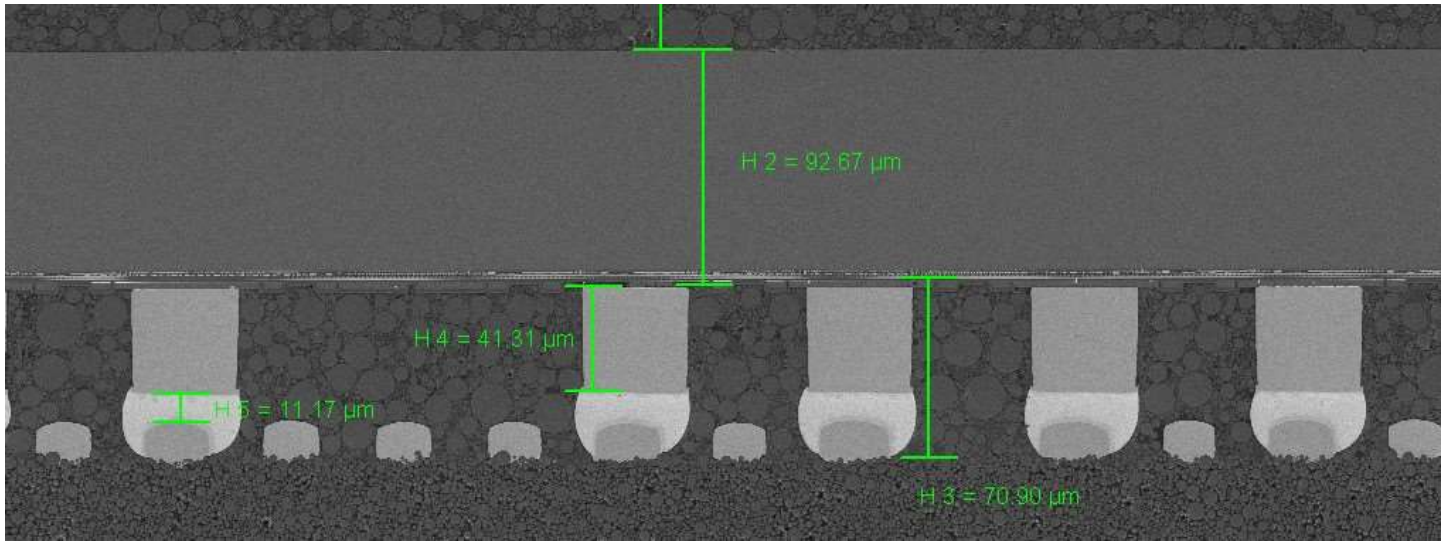
**(2) Gap** control: set the joint height as the control parameter

**(3) Temperature** profile is one of the key factors.



# Example: TCB with Cu Pillar Bond-on-Line (Laminate)



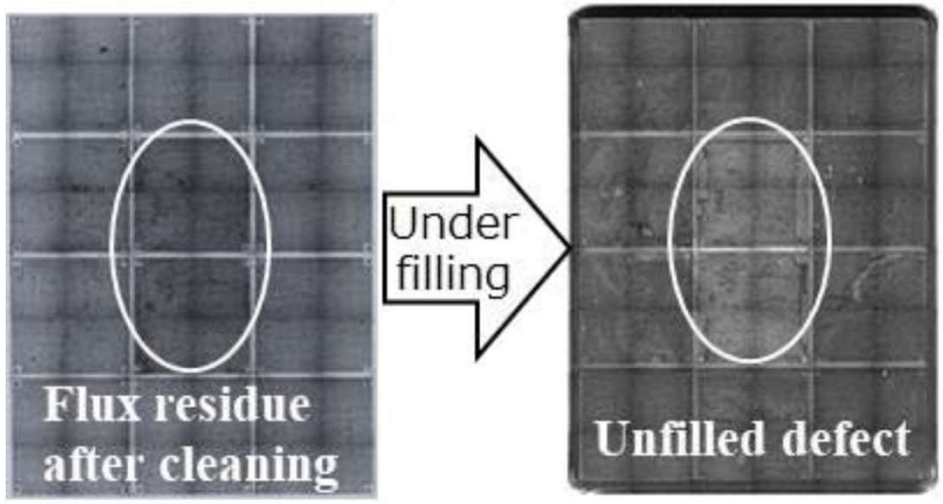




*S. Wen, Flip Chip Interconnect Course, 2023 ECTC*

# u-Pillar Underfill Defects

Issue:  Flux removal on micro-pillar joints is very difficult.
Residual flux results in underfill voids or underfill poor adhesion.

C-SAM Inspection after chip joining and after underfill with flux processing.

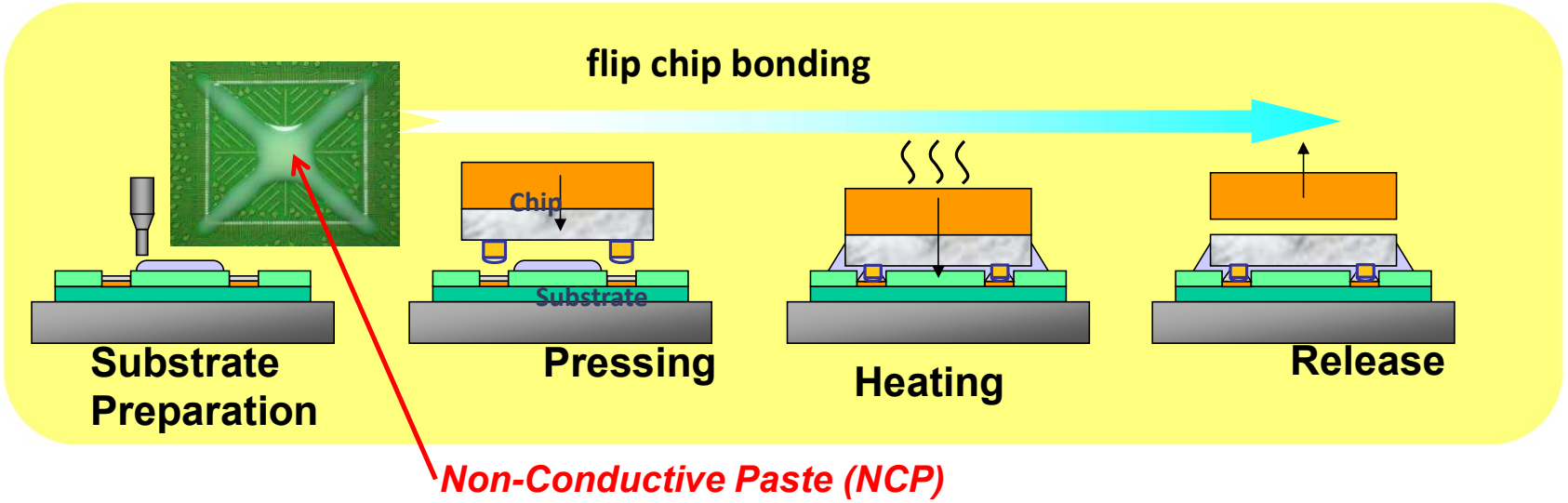



Solution 1:  Fluxless TCB via formic cleaning or wet cleaning.

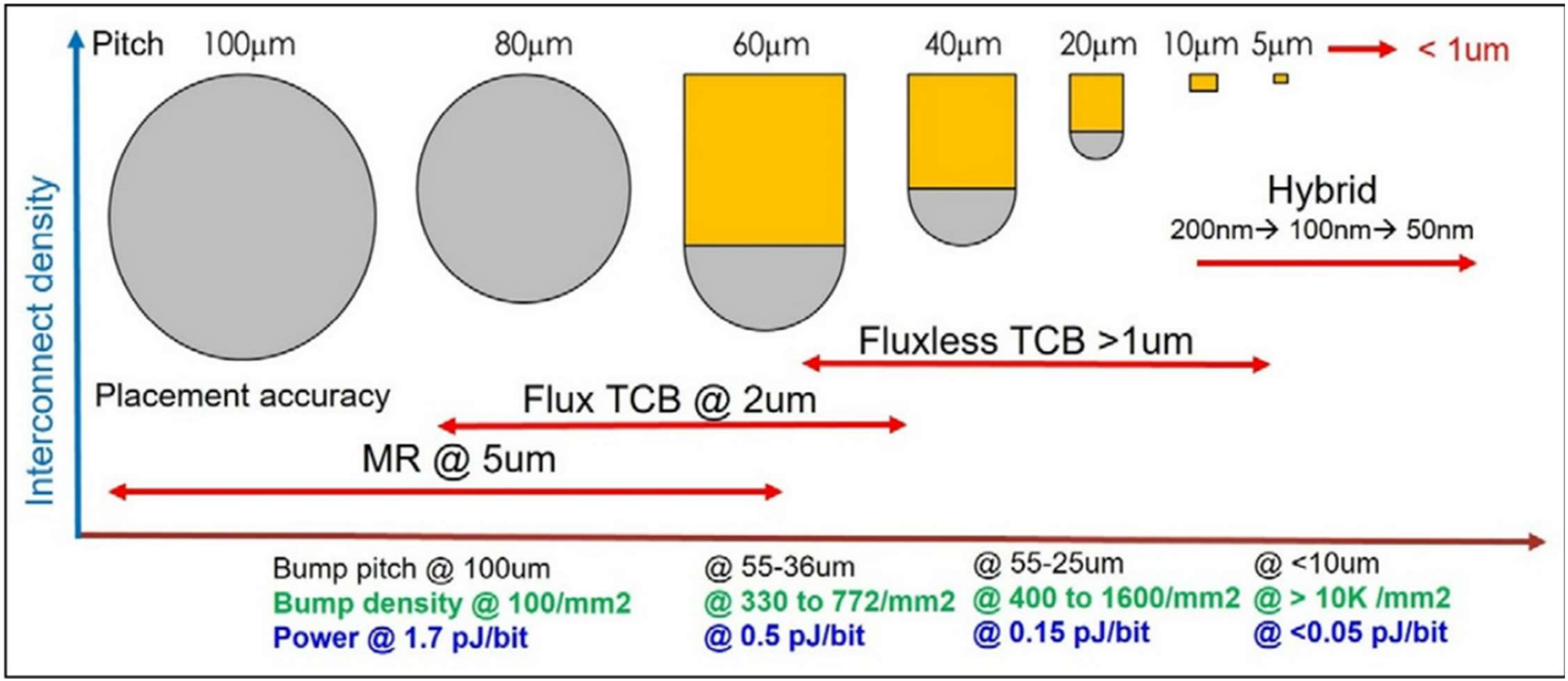
*Sadaaki Katoh, et. Al" Development of Fluxless Micro-Bonding and Narrow Gap Filling Process." 2023 ECTC*

# Thermal Compression Bonding w/NCP

Solution 2: TCB to with NCP - reducing cycle time and processing costs:



# Flux vs Fluxless , MR vs TCB Guideline



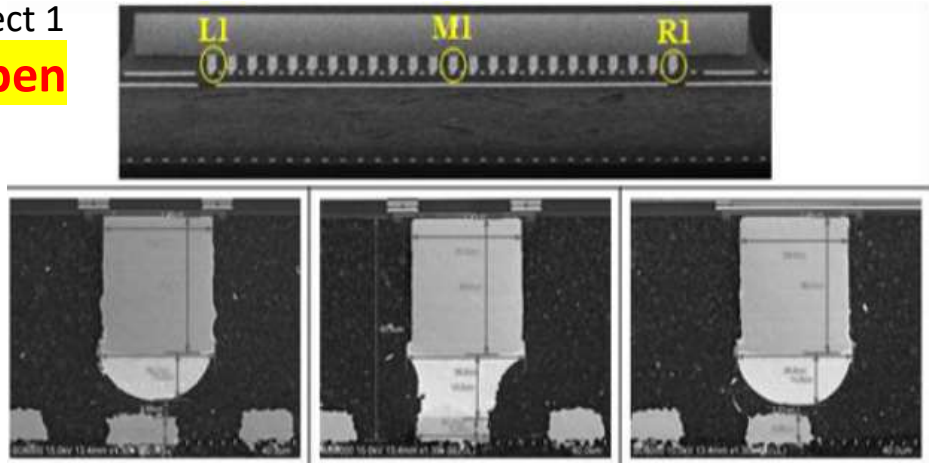

*Nelson Fan, ASMPT – Chip scale review July/August 2023*

# u-Pillar Joining Defects

## Effect of Substrate Warpage:

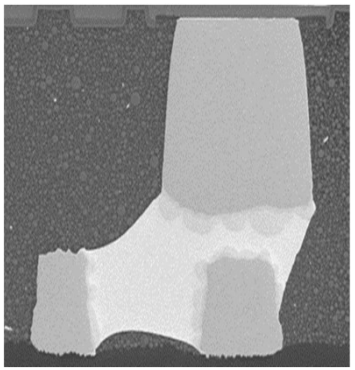
Defect 1

**Open**




Defect 2

**Short**



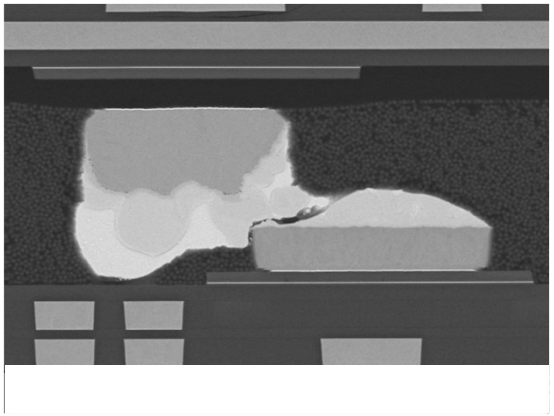
**Pitch** and Bump **Size**

# u-Pillar Joining Defects , continue

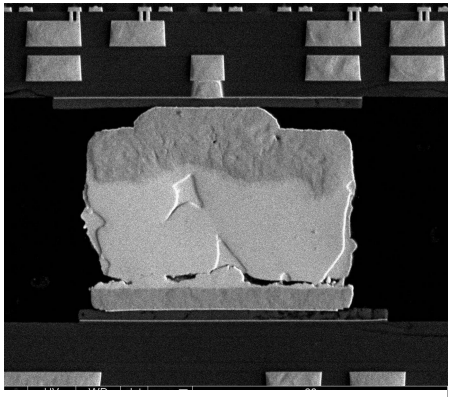
**Joining Defect:**

3. Significant mis-alignment between micro-joints and micro-pads on interposer.
4. Pad contaminant preventing full wetting.
5. Excessive TCB force.

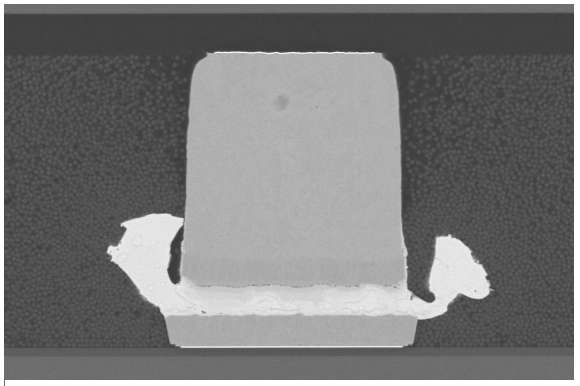
Defect 3



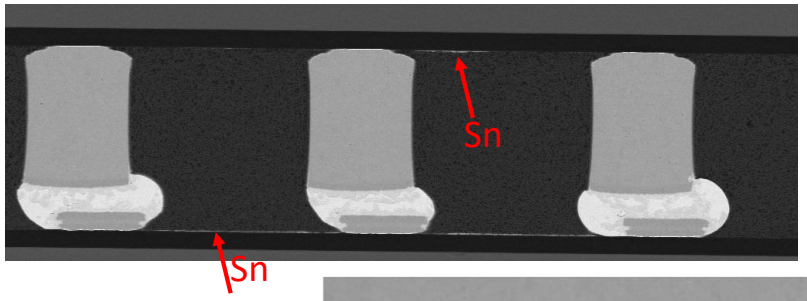
Defect 4



Defect 5



# u-Pillar Joining Defects, Continue



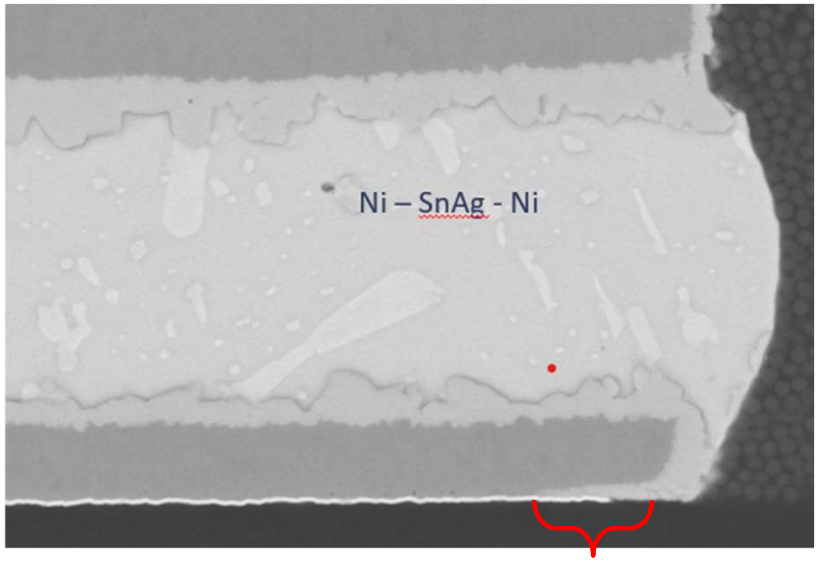

Defect 6:

Residual Sn at Joining

Defect 7:

Cu seed Reaction to solder results in Cu-Sn intermetallic.

Intermetallic adhesion to Ti or TiW is poor.




Cu seed Under cut (~4um)

# 20um Pitch: Cu / BMx / SnAg

**UBM Options:**
- **Cu/SnAg**
- **Cu/Ni/ SnAg**
- **Cu/BM2/SnAg**

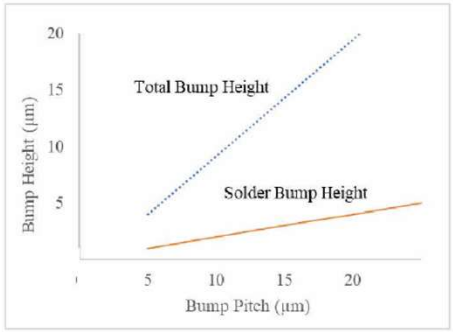



**Figure 1.** Estimated decrease in bump height due to bump pitch reduction.

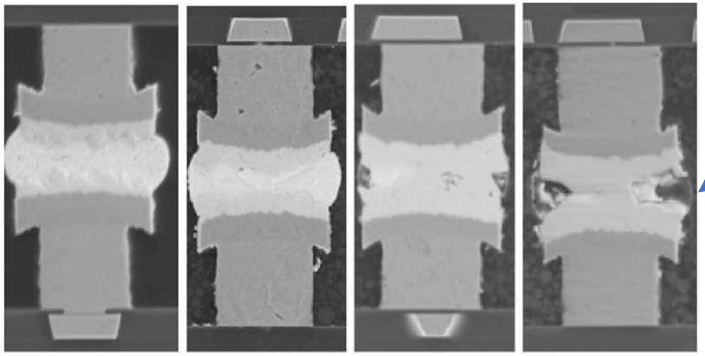



**Figure 13.** Isothermal aging of 20 μm pitch Cu/BM1/SnAg solder joints at 150°C for (a) 0 hour (b)168 hours (c)1008 hours (d)2016 hours.

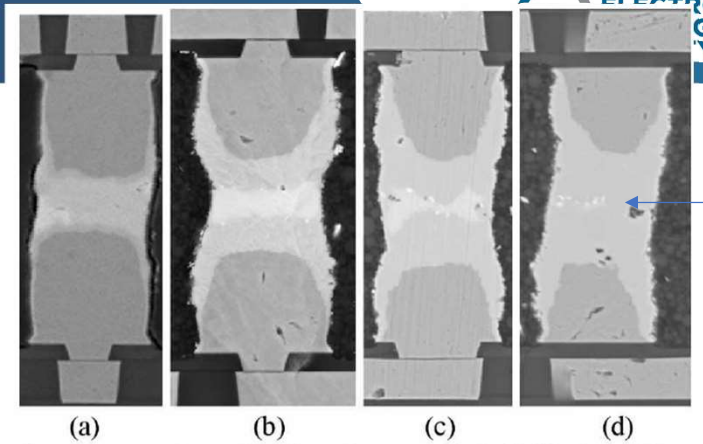



**Figure 12.** Isothermal aging of 20 μm pitch Cu/SnAg solder joints at 150°C for (a) 0 hour (b)168 hours (c)1008 hours (d)2016 hours.

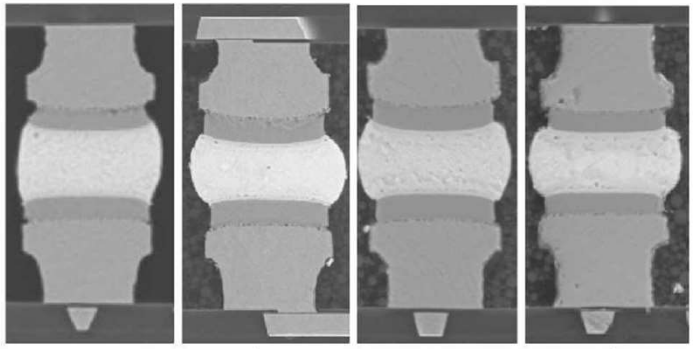
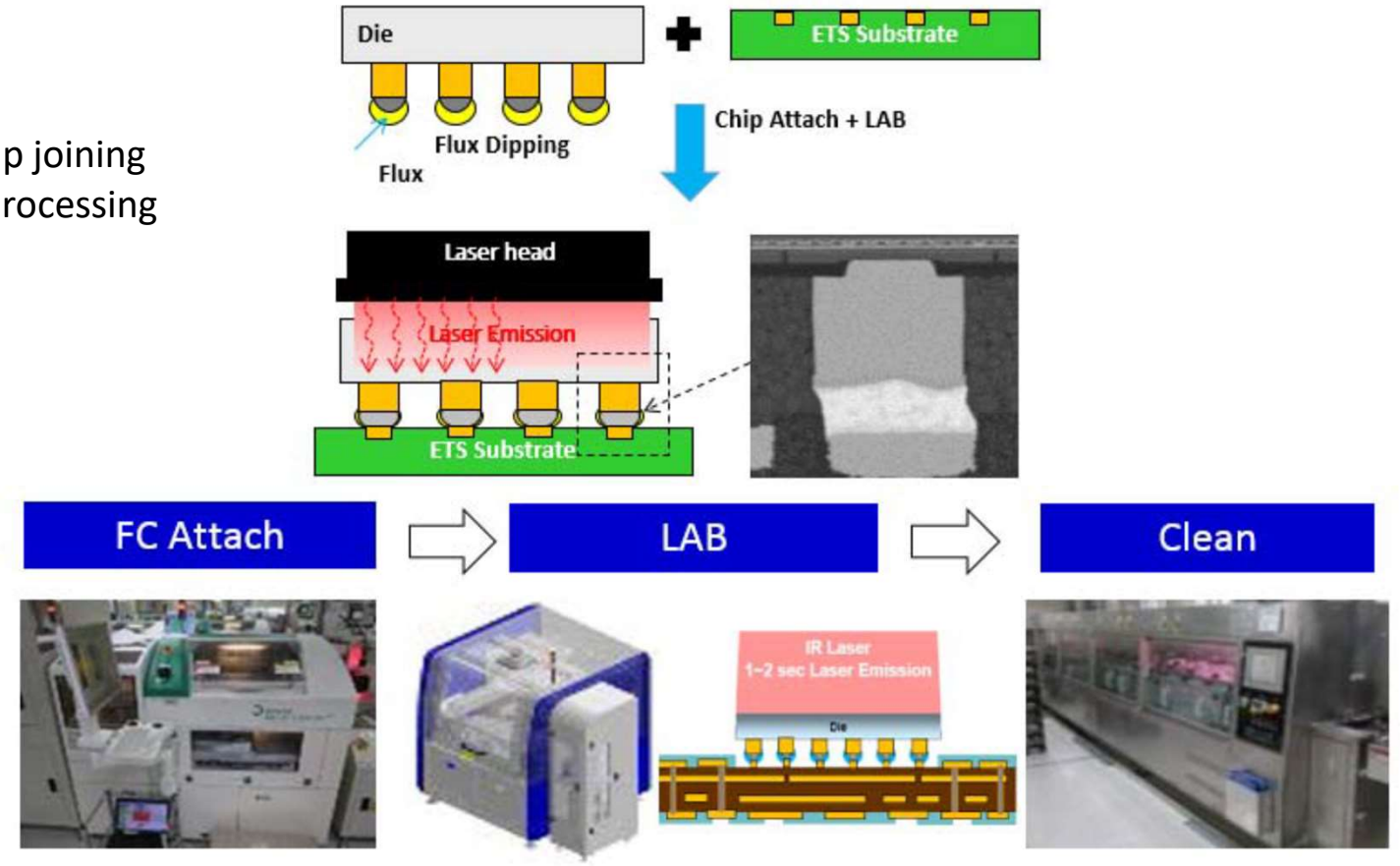



**Figure 14.** Isothermal aging of 20 μm pitch Cu/BM2/SnAg solder joints at 150°C for (a) 0 hour (b)168 hours (c)1008 hours (d)2016 hours.

*Zhaozhi Li', et at., "Scaling Solder Micro-Bump Interconnect Down to 10 pm Pitch for Advanced 3D IC Packages," 2021 ECTC*

# Laser Assisted Bonding (LAB)

LAB methodology can reduce chip joining cycle time from traditional TCB processing

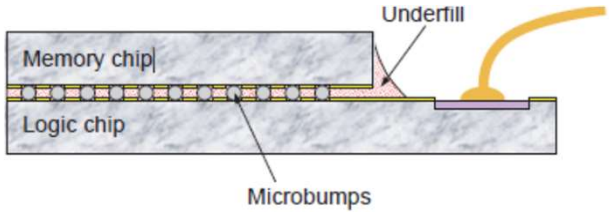


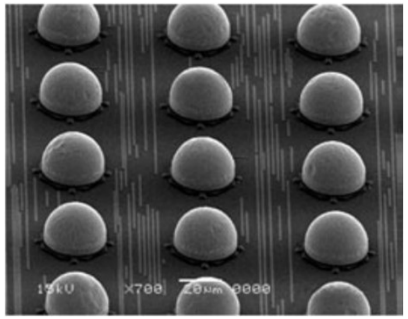

*Ian Hsu, et al., "7nm Chip-Package Interaction Study on a Fine Pitch Flip Chip Package w/LAP and MR Technology," 2019 ECTC*

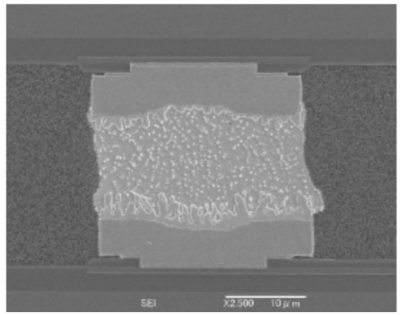
# u- Pillar TCB Assembly Options

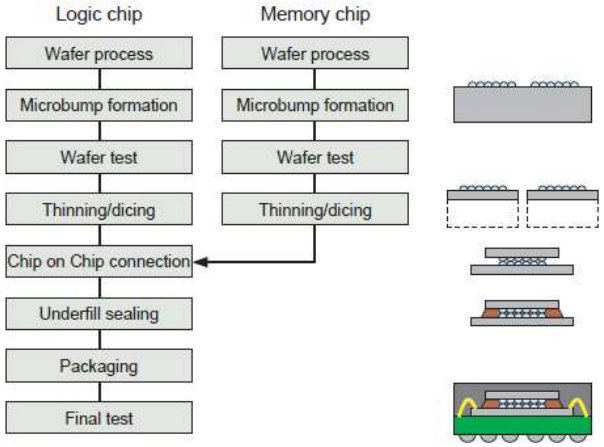
- TCB vs Mass Reflow depends on the alignment tolerances
  - Large dies with high substrate warpage require TCB for improved yields and white bump elimination.
  - LAP Process can also minimize CPI concerns and white bump issues.
- As the Cu-Pillar pitch decreases, the Cu height/solder height ratio increases to allow for increased gap resulting in better cleaning and good underfill.
  - Rule of thumb: Solder height < UBM diameter
- For u-Pillar with small underfill gaps, there are two main choices:
  - TCB Fluxless joining with solder pretreatment, such a formic acid or wet treatment, followed by fine particle underfill
  - NCP or NCF with TCB joining.

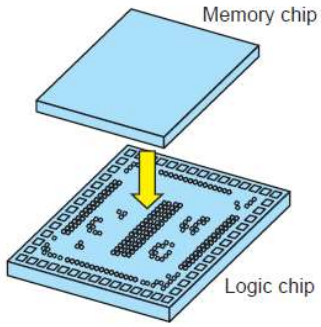
# First u-Pillar TCB Implementation: Sony D2D

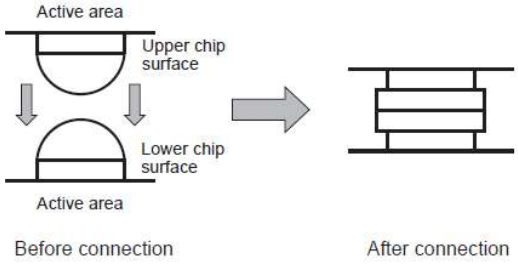







Multi-Chip LSI (MCL) used in the early assembly of the CPU of Sony PlayStations. SnAg solder bump for both the logic and memory are 30 μm C4s with 60 μm pitch. Thermal compression bonding is used, having a misalignment of less than 3 μm (average + 3σ).

*www.sony.net/Products/SC-HP/cx_news/vol50/pdf/featuring_1.pdf (2010)*

# Part 3: uPillar -Applications:
# Assembly / Structure Options

# HBM Integration and High-Performance Packaging

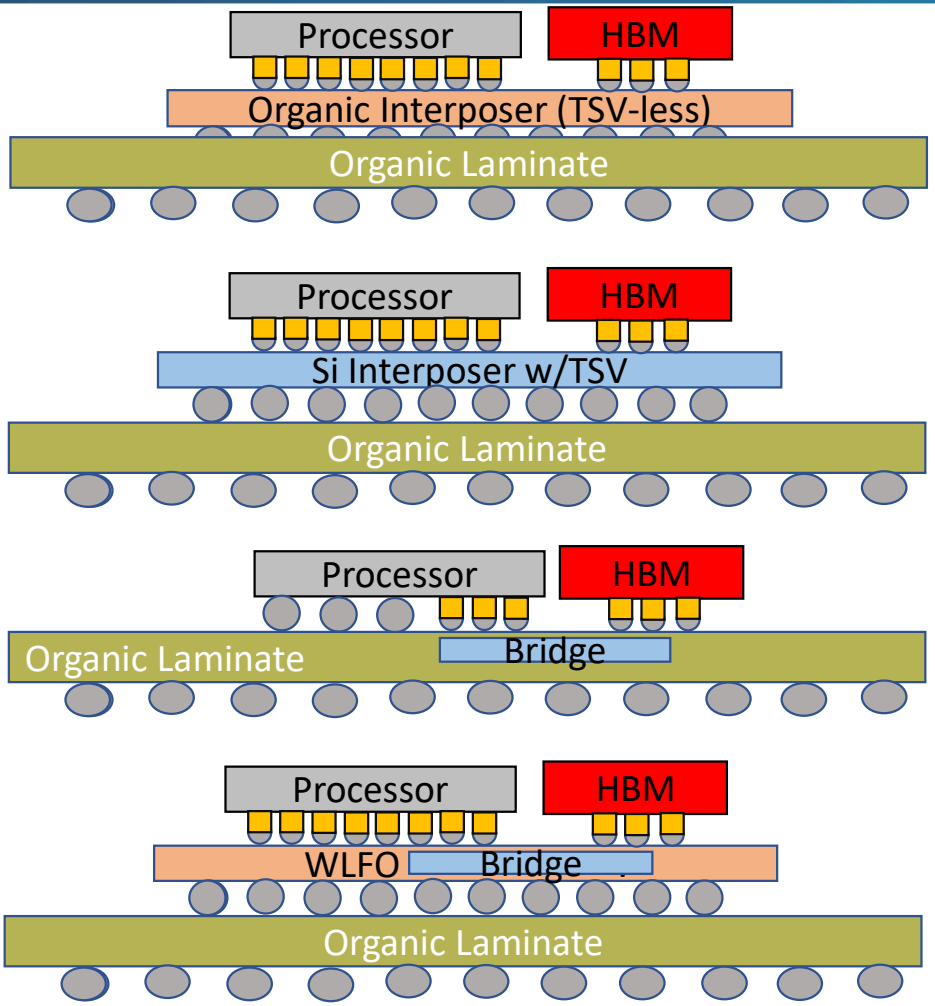
The introduction of HBMs with 55um Pitch / 30 um diameter Cu-Pillar required advanced packaging:

1) High performance laminate with organic RDL
   - Organic Interposer (RDL first FO-WLP) or iThop

2) Chip to Si interposer or to processor
   - 2.5D 3D, CoWoS, Memory
   - Requires Thru-Si-Vias (TSV)

3) Bridge technology
   - Intel EMIB, TSMC InFO-L

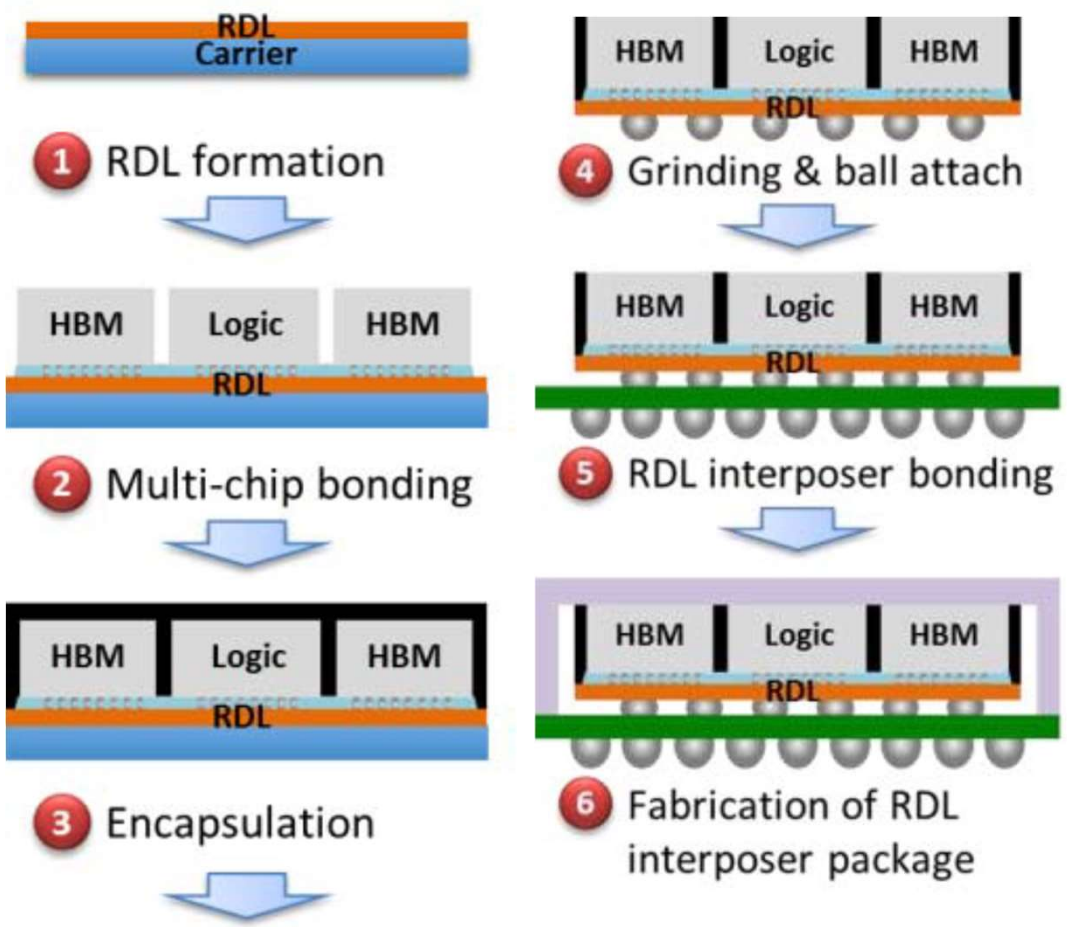
Note: Minimum laminate pitch limit is 90 um



# FO-WLP Process: RDL First

## Organic Interposer

- 1.5um L/S RDL are possible with a mechanical stable carrier
  - Si or Glass carriers
  - Low warpage
- Chips with u-Pillars are joined to the organic interposer, followed by underfill and encapsulation
- After the carrier is removed, C4 are attached to the interposer backside, then diced, tested and joined to the laminate substrate.

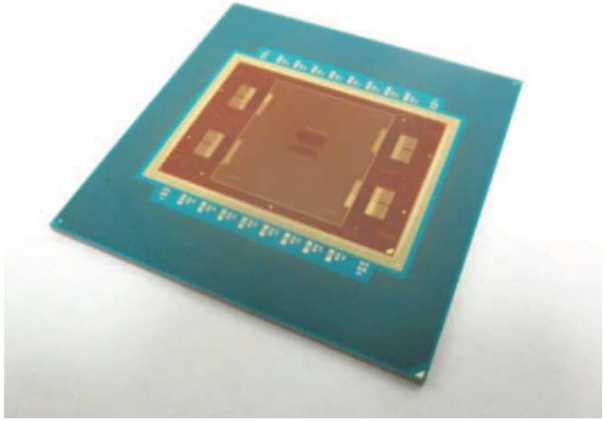


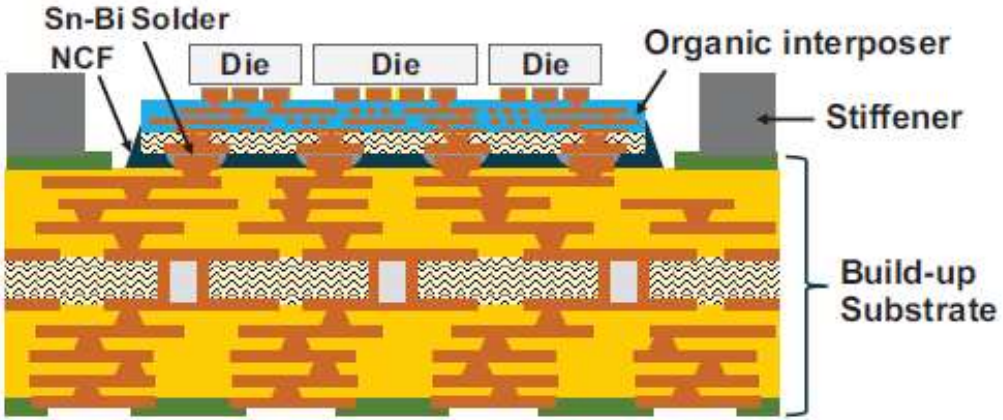

*K.L. Suk, et. Al.,"Low-Cost Si-less RDL Interposer Package for High Performance Computing Applications," 2017 ECTC*

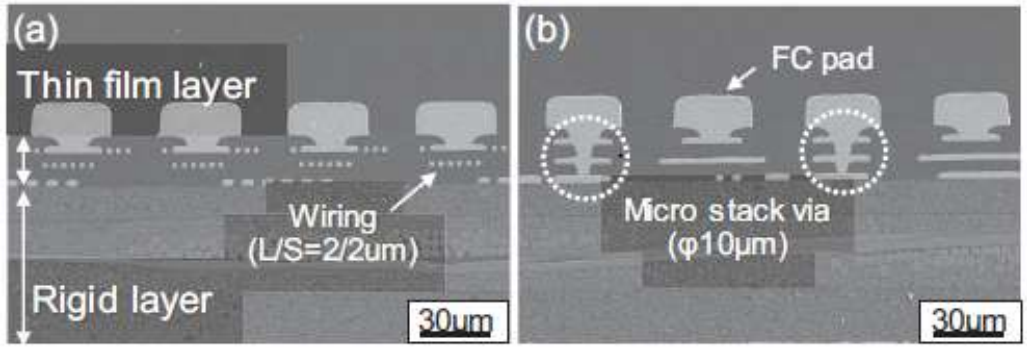
# 2.3D Hybrid Laminate

## Shinko's Integrated-Thin film High density Organic Package (i-THOP® )

To support 55um u-Pillar pitch HBM, a highly dense organic RDL patch was developed by Shinko.
The Cu-Polyimide RDL is fabricated on rigid carrier, then diced and joined to the laminate, prior to processor and HBM joining.

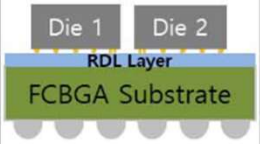
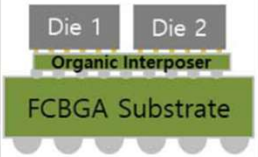
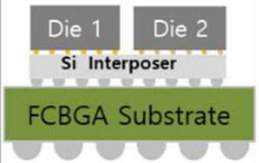
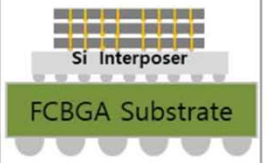


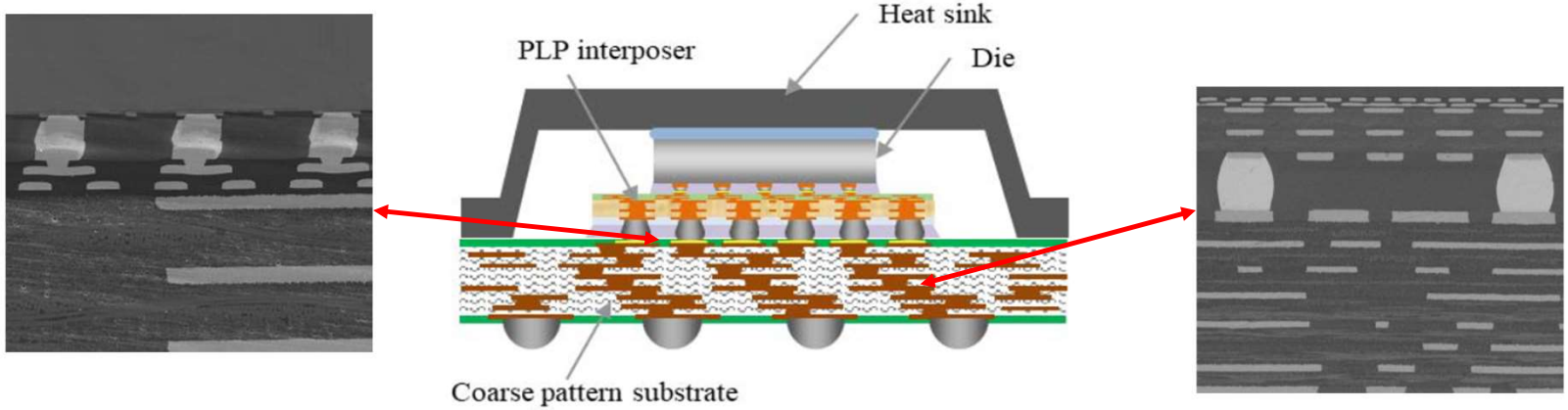



Shota Miki, 2019 ECTC

# x.xD Structure – Integration with Flip Chip

| Package Type | 2D | 2.1D | 2.3D | 2.5D | 3D |
|---|---|---|---|---|---|
| Schematic Image |  |  |  |  |  |
| L/S (μm) | 9/12 | ~2/2 | ~2/2 | <1/1 | <1/1 |
| I/O Density | Low | Middle | Middle | High | High |




*S. Wen, Flip Chip Interconnect Course, 2023 ECTC*

# HBM Interconnect Options w/Chip Last Approach

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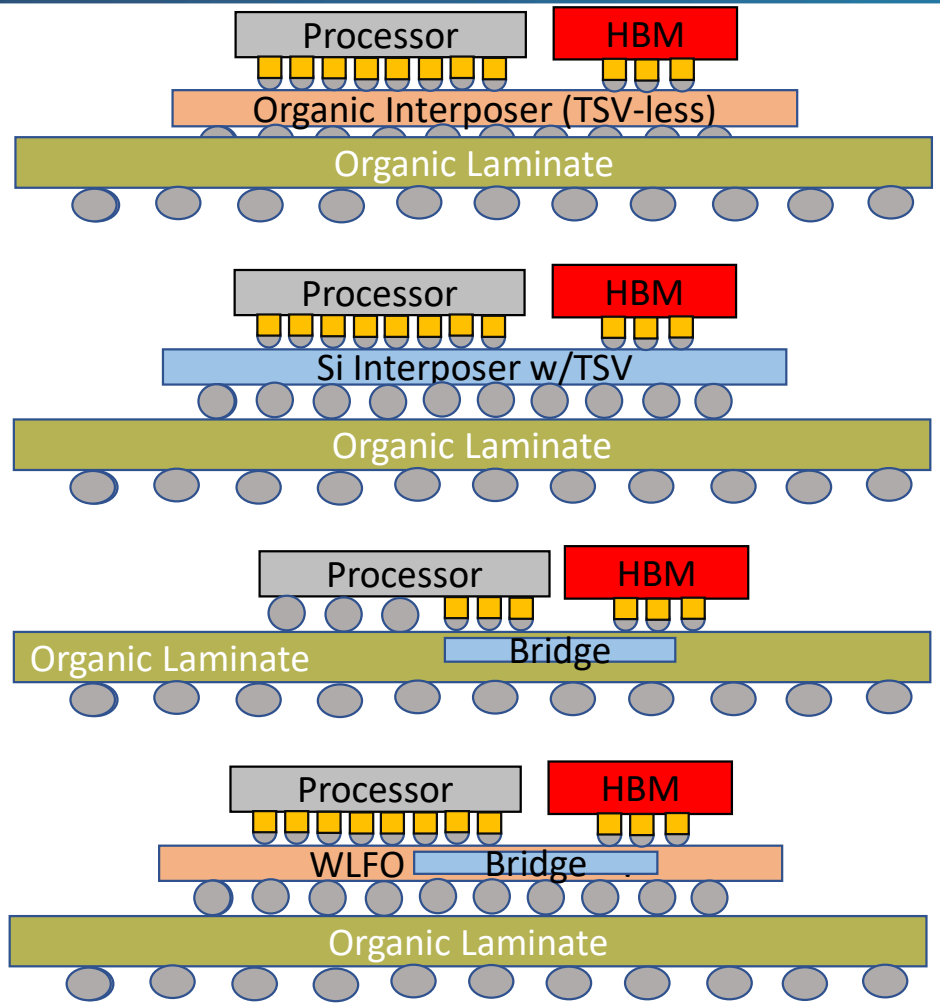
1) High performance laminate with organic RDL
   - iThop or Organic Interposer (RDL first FO-WLP)

2) Chip to Si interposer or to processor
   - 2.5D 3D, CoWoS, Memory

3) Bridge technology
   - Intel EMIB, TSMC InFO-L

Note: Minimum laminate pitch limit is 90 um

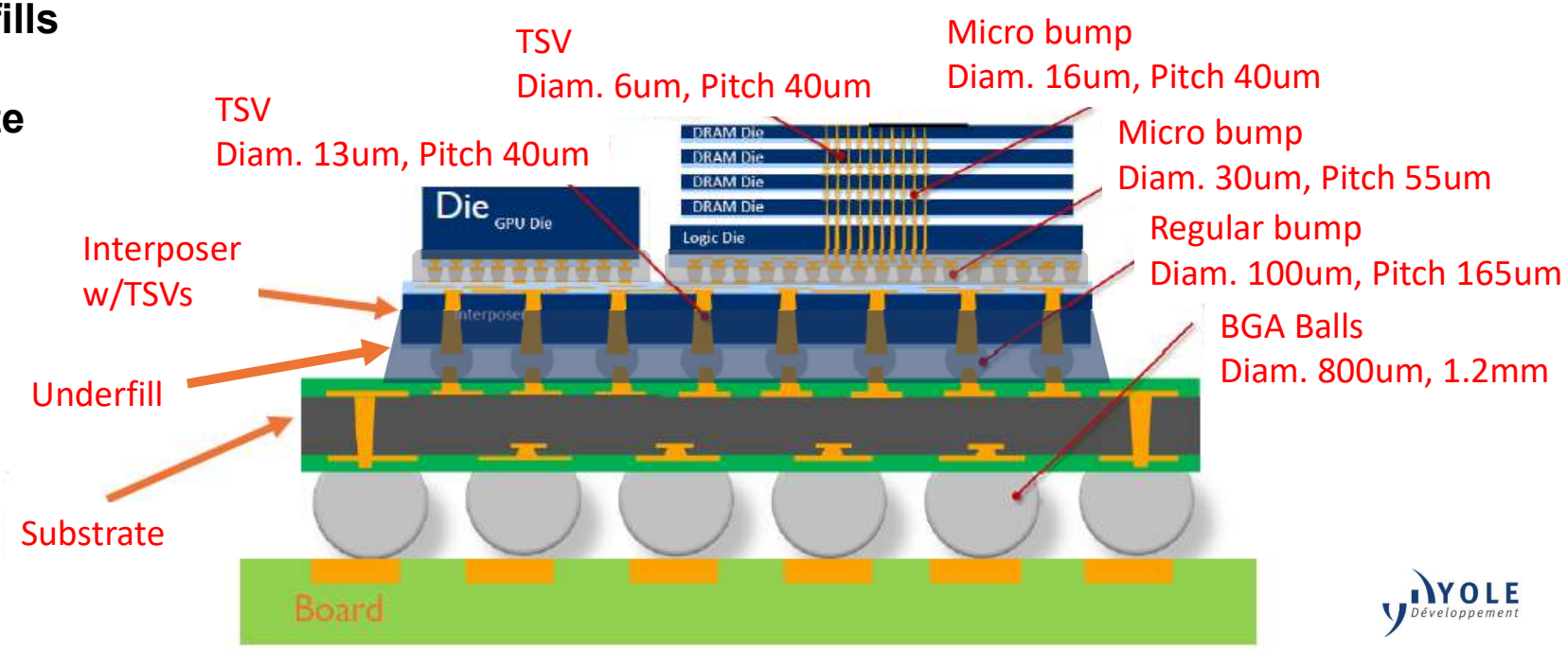


# Flip Chip Application at a Glance: 2.5D

**Flip Chip Interconnection: 3 elements**

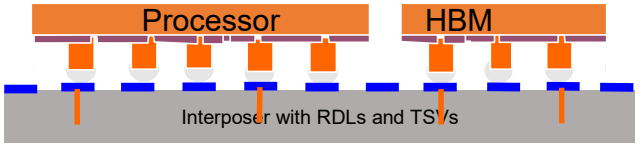
- **4 solder connections**
- **2 Underfills**
- **Substrate**

Si Interposer with Thru-Si-Vias (TSV)

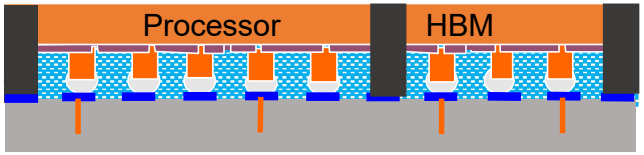


# Si Interposer Assembly

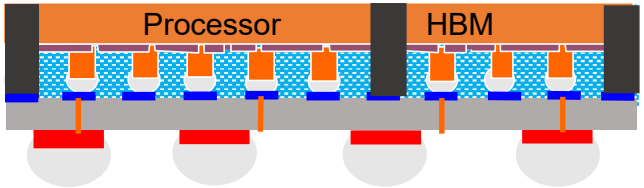

Si Interposer with TSVs and Capture pads



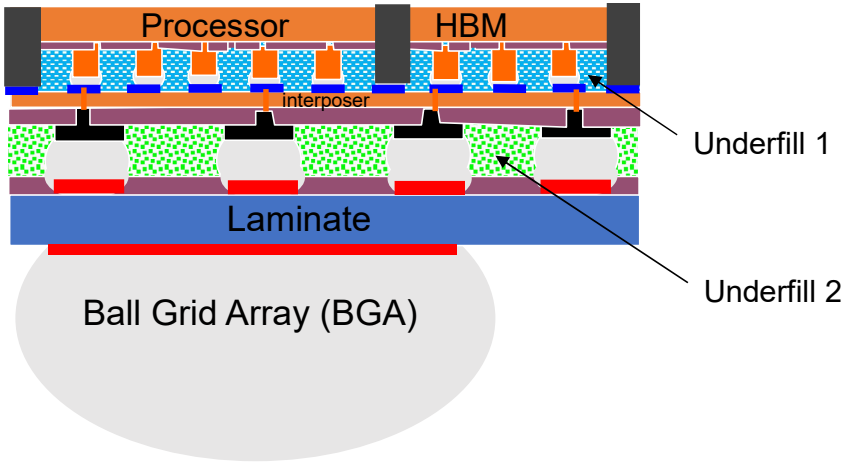

D2W joining of Top dies




Underfill + Overmold and Mold/Chips Thinning



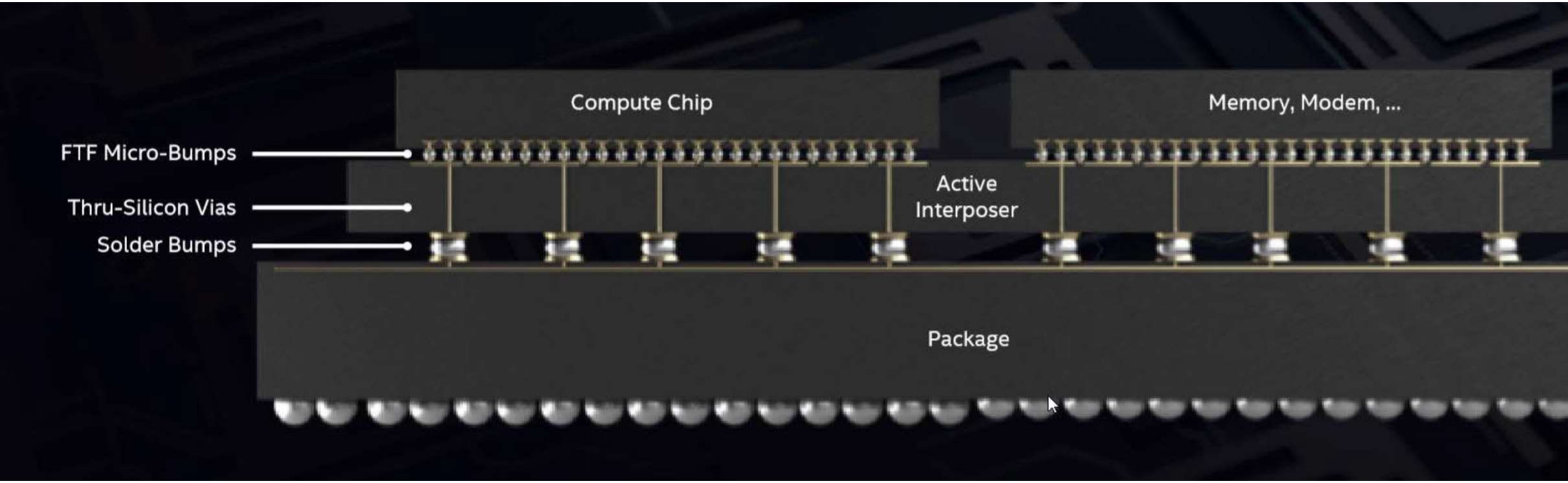

TSV Reveal + C4 fabrication +Test + Dice


Join module to Laminate + Underfill + BGA + Test

# 3D Die Staking

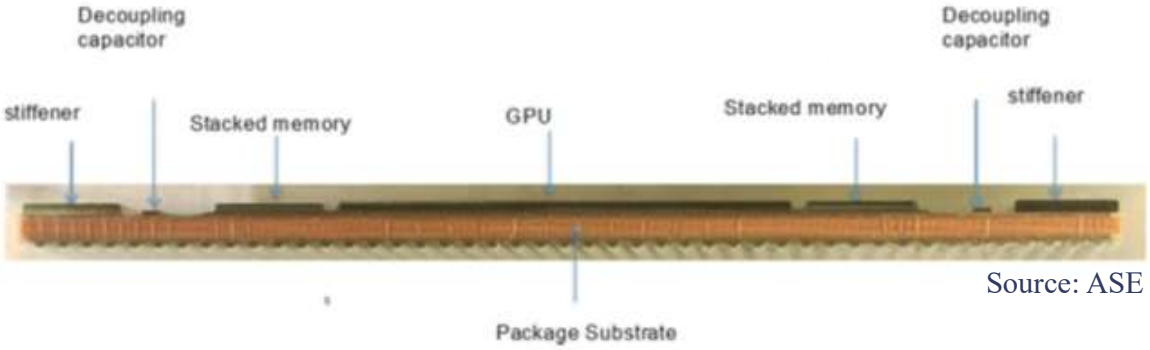
3D Die stacking consist of replacing a passive Si interposer with an active chip with TSV . While the technology to fabricate is the same as 2.5D, additional layers of an active chip significantly increases the wafer bow and handling complexity.



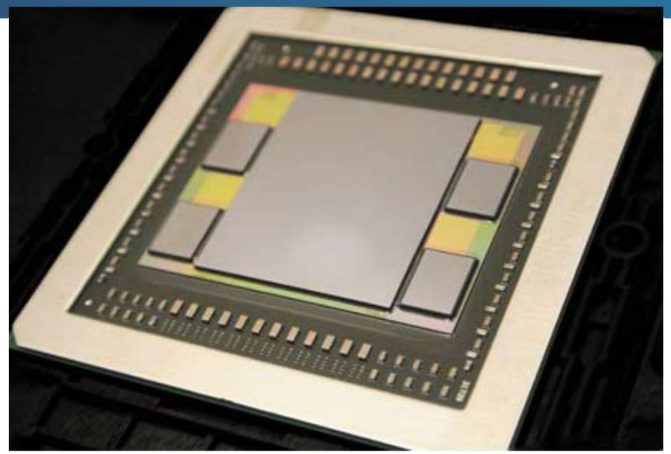

**FOVEROS 3D chip stacking by Intel**

https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2021-edition.html

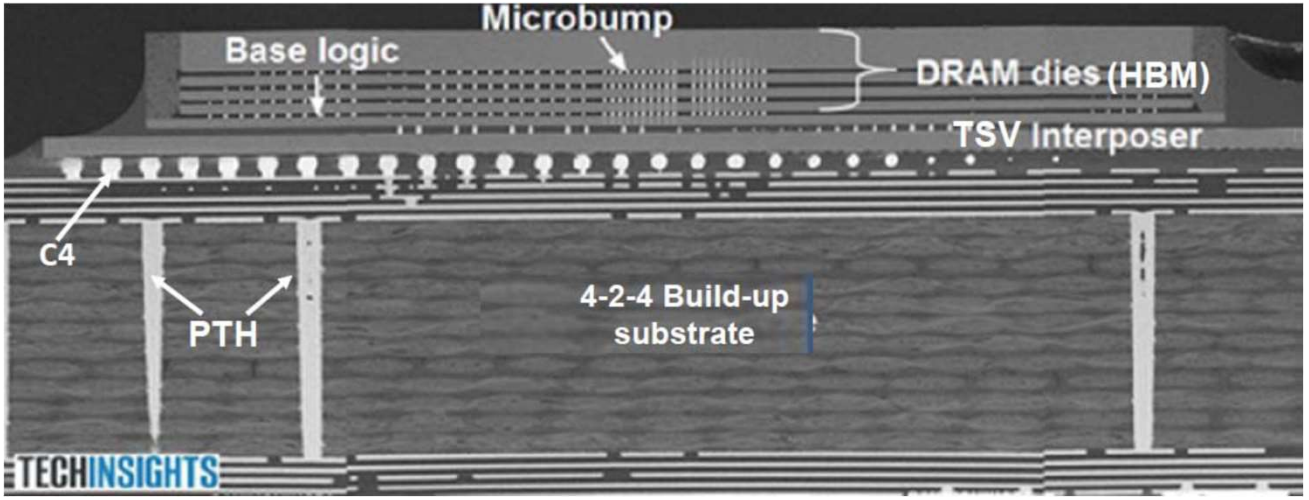
# 2.5D Si Interposer: AMD Fiji




Source: ASE

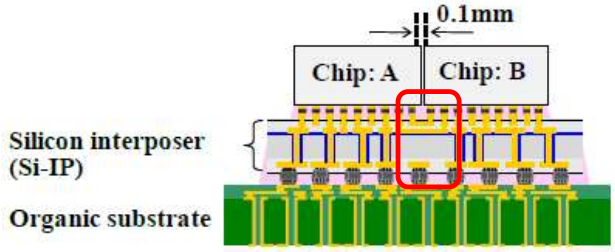


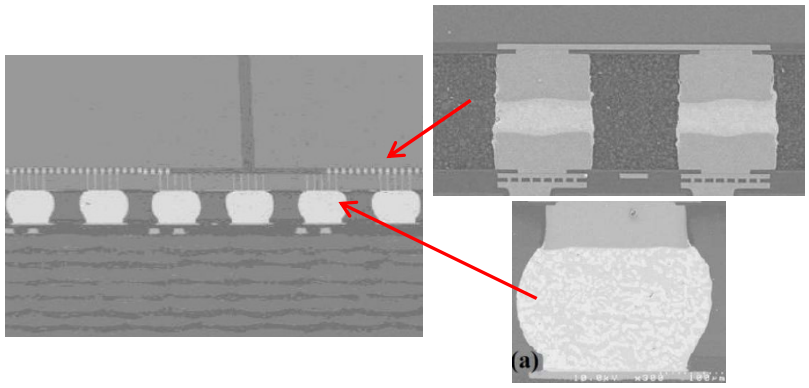
AMD Fuji:
- 23mm x 27mm Chip
- 28mm x 35mm Si Interposer with 1 um L/S RDL
- 54x54 mm organic laminate with Caps and stiffener on top and BGA on bottom

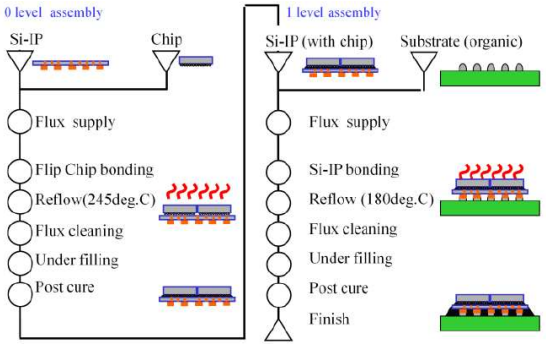



*S. Wen, Flip Chip Interconnect Course, 2023 ECTC*

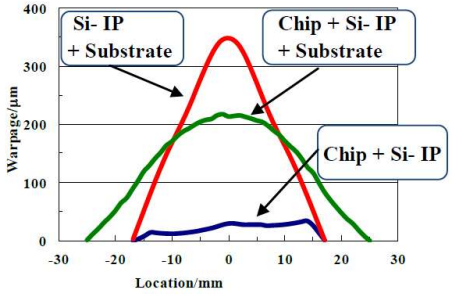
# D2D with 2.5D Interposer Integration

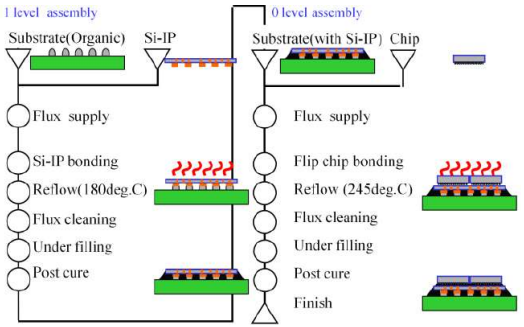



Chip First ✓




Chip Last

Best approach is chip first but using Die-to-Wafer Process

*Murayama, K., et al, "Warpage Control of Silicon Interposer for 2.5D Package Application," 2013 ECTC*

# HBM Interconnect Options w/Chip Last Approach

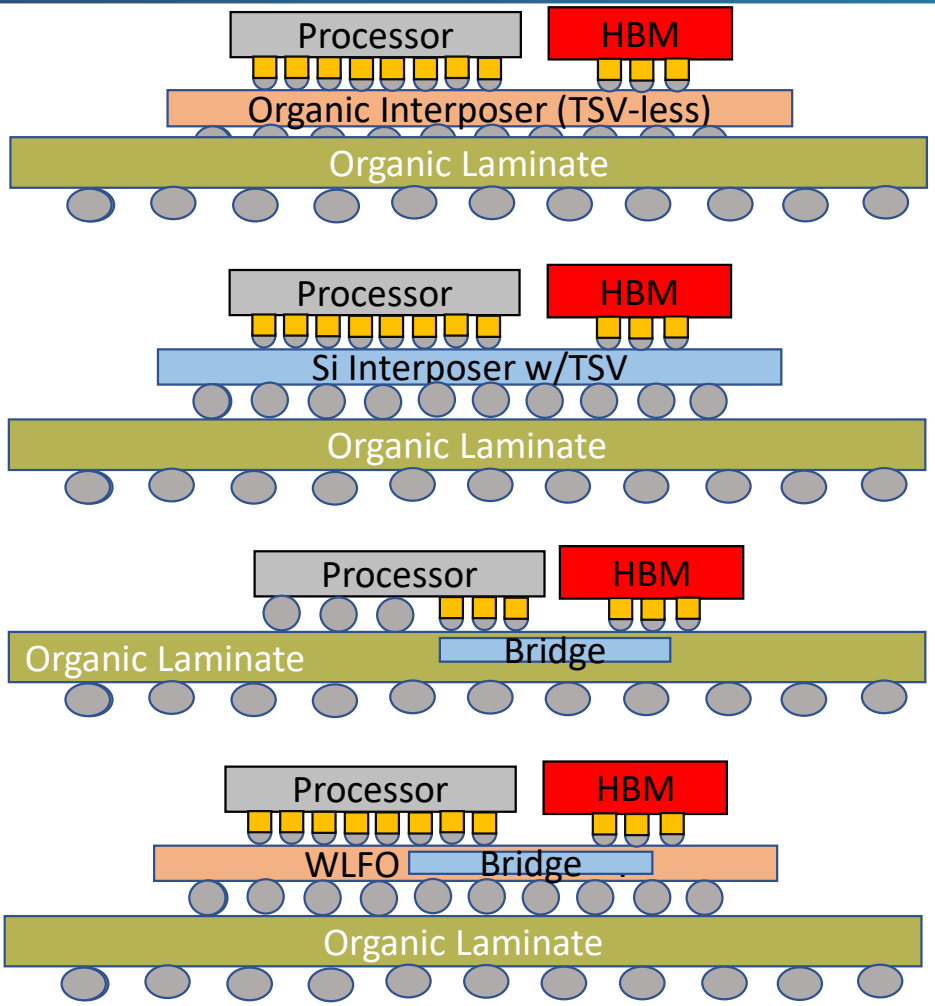
The introduction of HBMs with 55um Pitch / 30 um diameter Cu-Pillar required advanced packaging:

1) High performance laminate with organic RDL
   - iThop or Organic Interposer (RDL first FO-WLP)

2) Chip to Si interposer or to processor
   - 2.5D 3D, CoWoS, Memory

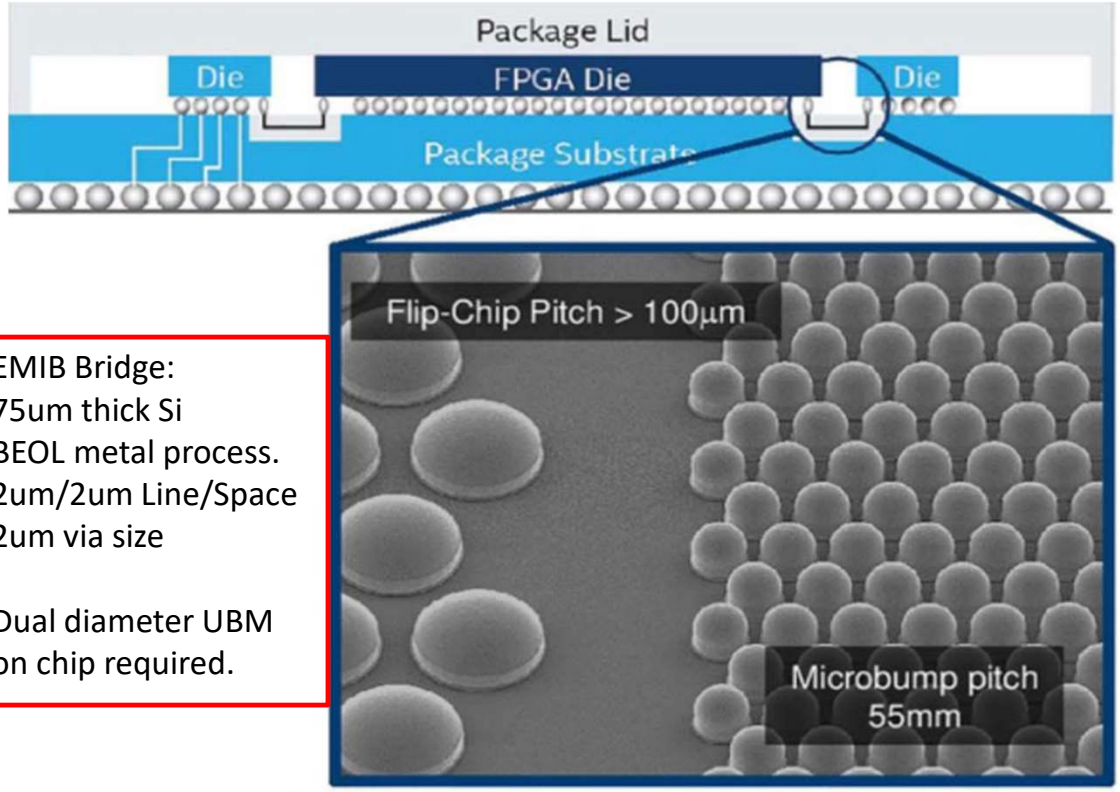
3) Bridge technology
   - Intel EMIB, TSMC InFO-L

Note: Minimum laminate pitch limit is 90 um



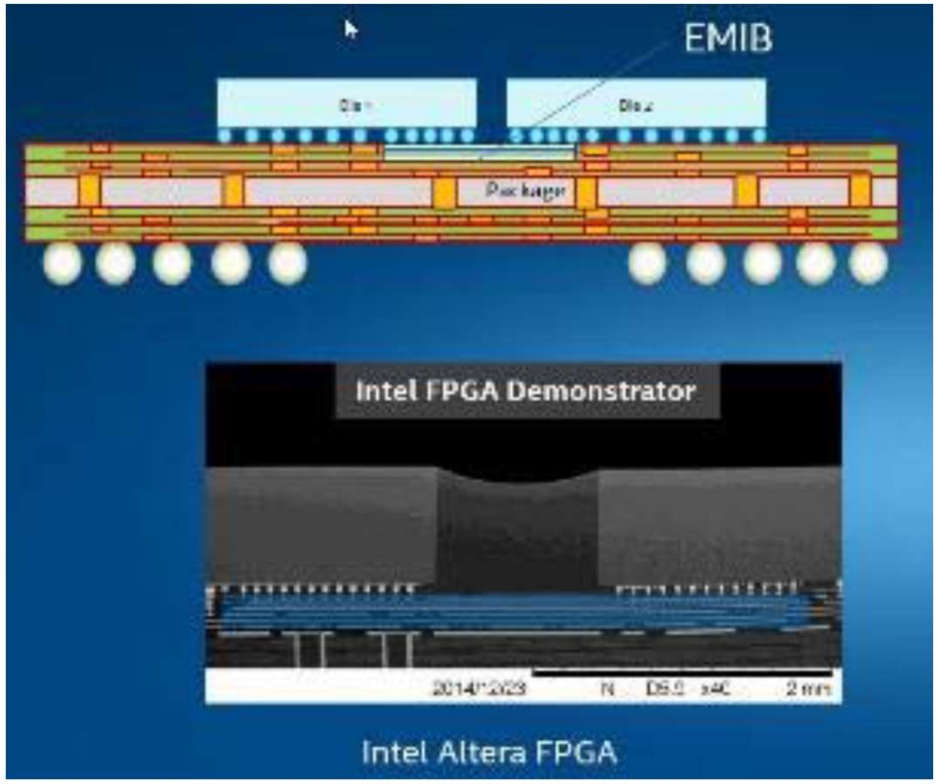
# Si Bridge Technology

## Intel's Embedded Multi-die Interconnected Bridge (EMIB)




EMIB Bridge:
75um thick Si
BEOL metal process.
2um/2um Line/Space
2um via size

Dual diameter UBM
on chip required.




A Si chip is placed in the laminate to interconnect the HBM to the processor chip.

https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2021-edition.html

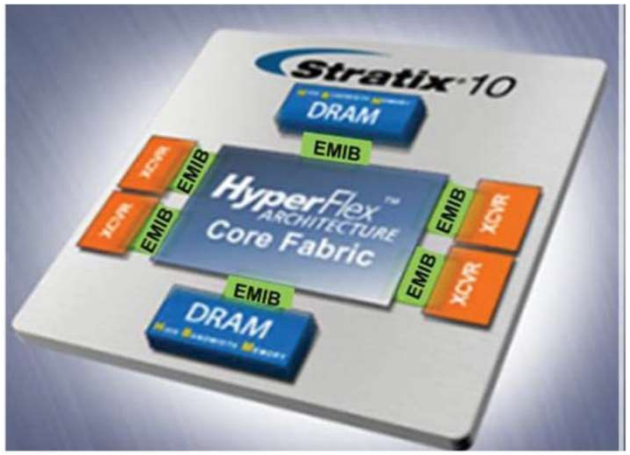
# EMBI Interconnect Technology

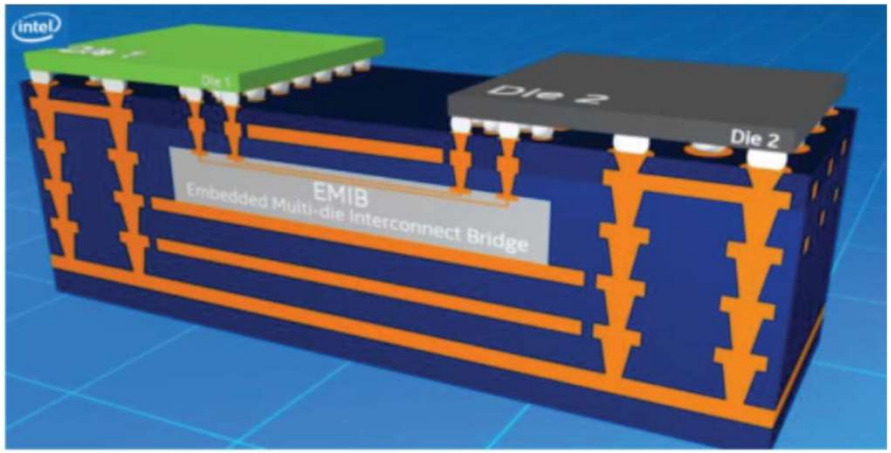
## EMBI Advantages:

- Replaces lower yields 6 laminate layers with a high yield pre-inspected Si chip bridge.
- Extends the Laminate technology
  - Laminate fine pitch I/O.

## Disadvantages:

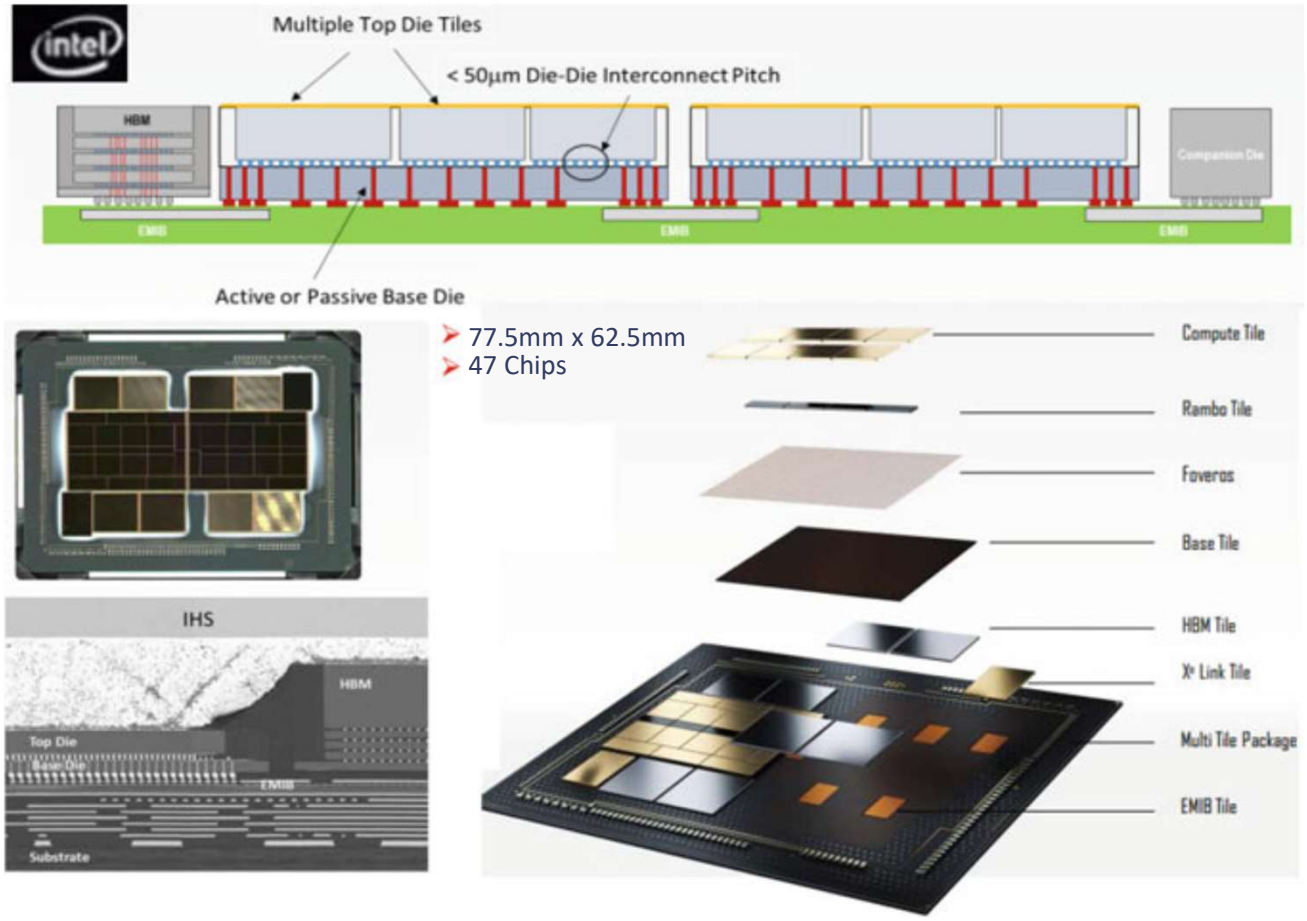
- Requires mixed pitch in the processor chip.
- Limits large pitch underfill mechanical performance – less Silica fill.
- Requires 2 additional layers to capture embedded chip I/O.




https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2021-edition.html
https://youtu.be/mRQFJFmYMak

# Intel Ponte Vecchio GPU

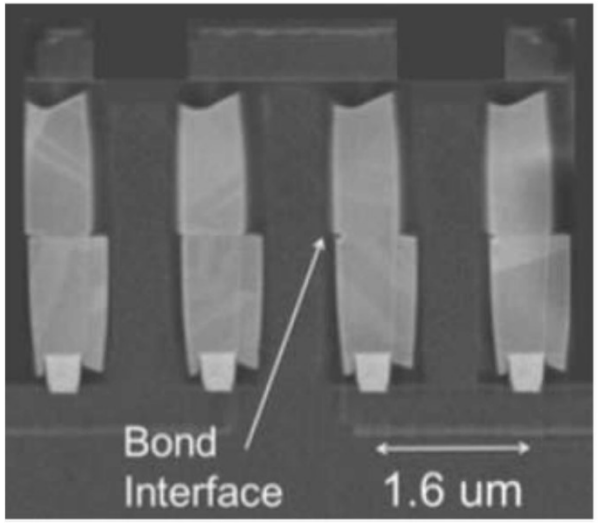



https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2021-edition.html

# Hybrid Bonding Process: A Non-Solder Joint


Hybrid bonding is a Si to Si interconnect. Initially started at Wafer level with Sony camera but new die to wafer applications are currently surfacing.

Main issues are contamination, Cu recess, surface treatment, TCB accuracy and voids. The process works best at <10 um pitch and joined diameter of ≤ 5um since it relies on tight control the recessed Cu gap.

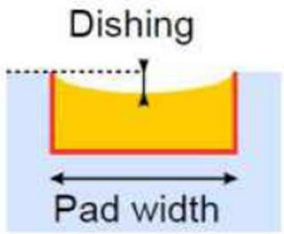


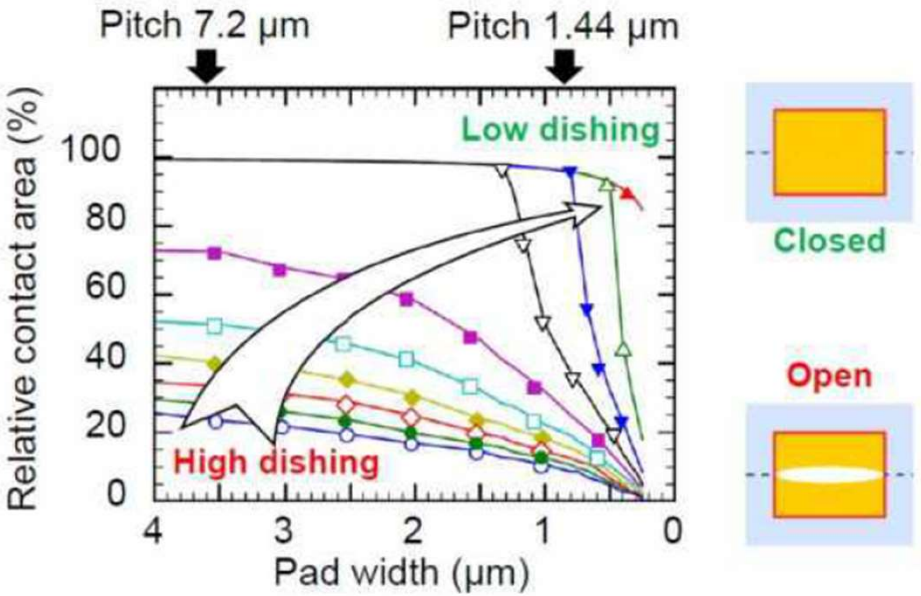

https://4sense.medium.com/hybrid-bonding-technologies-info-f547fd0dc7c5,

L. Wang, et al., "Direct Bond Interconnect (DBI®) for fine-pitch bonding in 3D and 2.5D integrated circuits," 2017 Pan Pacific Microelectronics Symposium

# Cu Dishing

Simulation of Cu/Cu interface closure at 400 °C



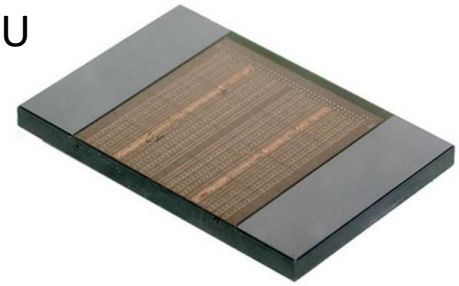

Smaller pads require significantly less dishing during the CMP process

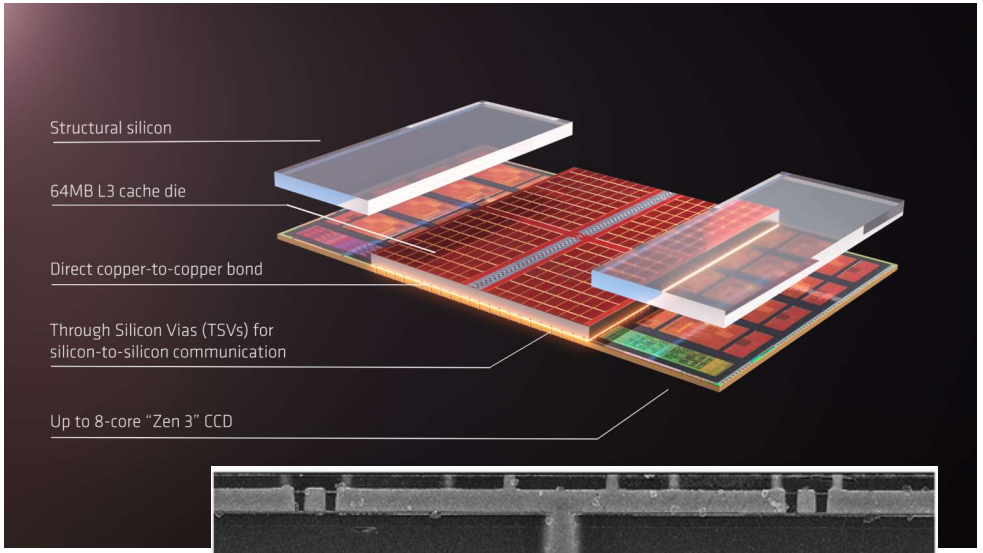
➔ Mixed pad diameter or pitch not recommended.

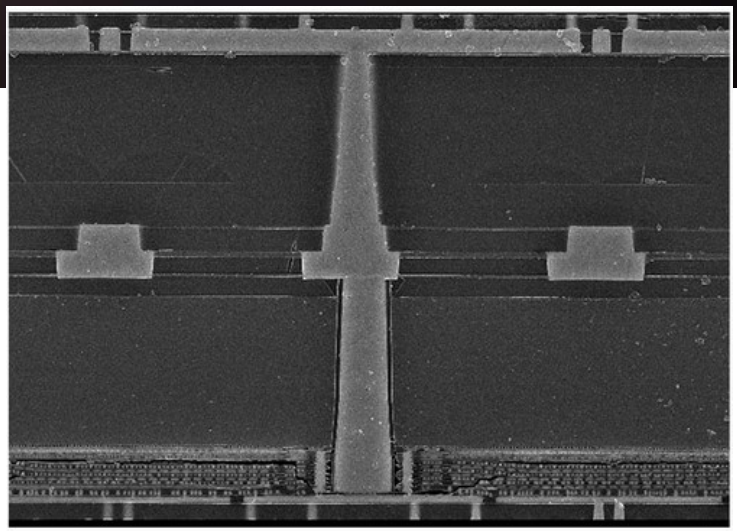
i-Nemi webinar by 2021 C.S. Tan ; Source: ST Micro and 3DIncites

# Hybrid Bonding Implementation: AMD / TSMC

Hybrid bonding connects the cache memory dies to the CPU compute die. The process involves direct copper-to-copper bonding. 3D V-Cache technology is a packaging technology using through silicon via (TSV) interconnections for for higher data transfer rates between chips.





It achieved higher interconnection density, increased bandwidth, and ultra-robust interface between the two dies. Hybrid bonding offers 15 times higher interconnect density and higher energy efficiency accompanied by superior thermal conductance compared to micro bump 3D solutions.

*2022 Yole brochure on AMD Ryzen 7 gaming CPU*

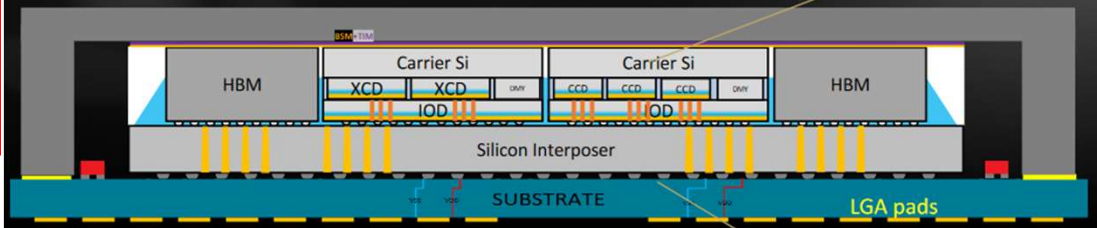
# AMD F2F Hybrid Bonding

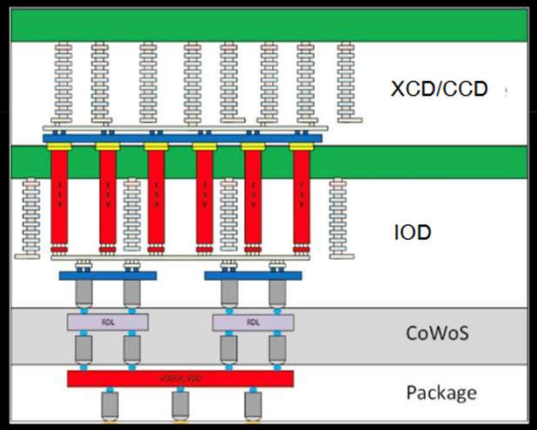
TOV
(or Through Oxide Via)
is a unique application which enables hybrid bonding to std chips.

## AMD INSTINCT™ MI300 FAMILY

### 3.5D Advanced Packaging Elements

Unique Thermal architecture
→ ~750W TDP

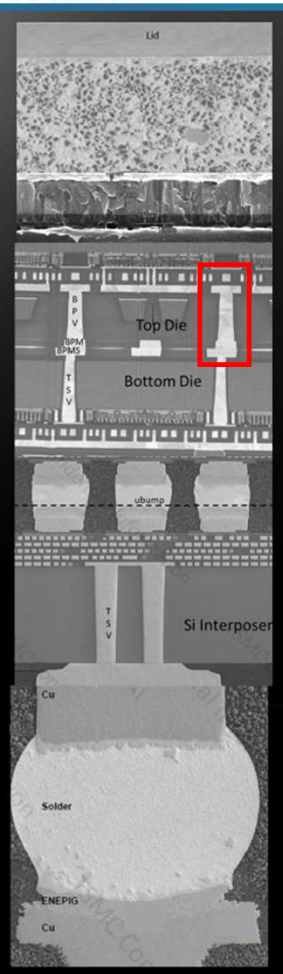



Advanced 3D Hybrid Bonding→ Compute density and perf/W

Advanced 2.5D Arch→ Ultra high BW IOD-IOD and HBM3 integration

Large module Attach on Advanced 2D Substrate




*AMD Instinct™ MI300X Accelerator: Packaging and Architecture Co-Optimization – 2024 VLSI*

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AMD
together we advance_

# Thank You

## John Lau

**Advanced Substrates for Chiplets and Heterogeneous Integration**

John H Lau, with more than 40 years of R&D and manufacturing experience in semiconductor packaging has published more than 535 peer-reviewed papers (375 are the principal investigator), 51 issued and pending US patents (35 are the principal inventor), and 23 textbooks (all are the first author). John is an elected IEEE fellow, IMAPS Fellow, and ASME Fellow and has been actively participating in industry/academy/society meetings/conferences to contribute, learn, and share.

## Fumihiro Inoue

**Key Technologies and Mechanism Analysis for Next-Generation Hybrid/Fusion Bonding**

Fumihiro Inoue is an Associate Professor at Yokohama National University, specializing in 3D integration and chiplet. Before joining the university, he contributed extensively to advancing unit processes for 3D integration during his role as researcher at imec, which lasted until 2021. In recognition of his significant contributions to the field, he received the prestigious IEEE EPS Outstanding Young Engineer Award in 2022. Since April 2024, Dr. Inoue has also served as the Vice-Director of the Semiconductor and Quantum Integrated Electronics Research Center at Yokohama National University, where he continues to lead cutting-edge research initiatives