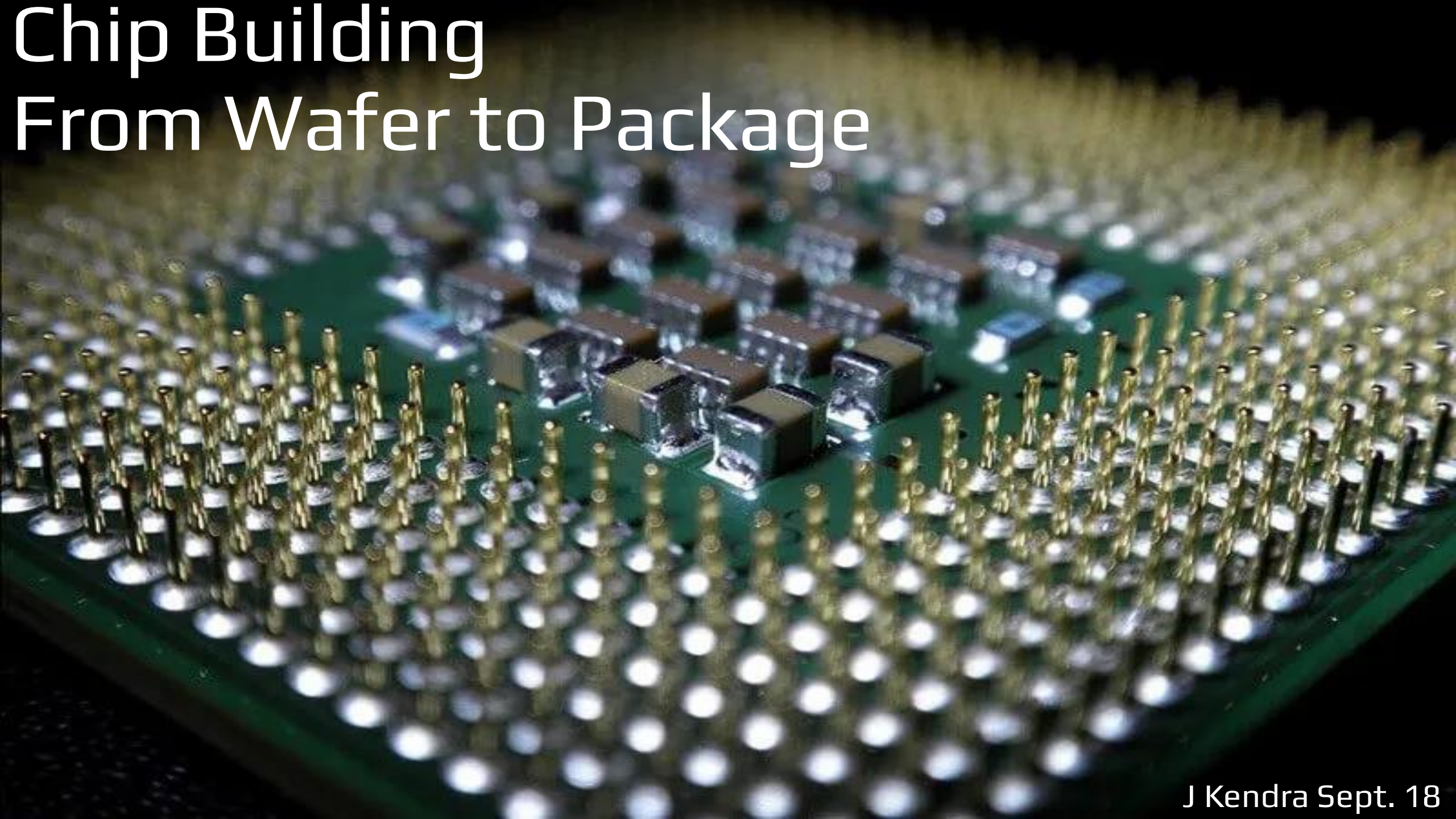
Chip Building
From Wafer to Package



J Kendra Sept. 18

What is a transistor?

- https://youtu.be/Bfvyj88Hs_o?si=pmCoD15TxR33IPaB&t=68

GBM Attendance

What is a transistor?

https://youtu.be/Bfvyj88Hs_o?si=pmCoD15TxR33IPaB&t=68

How many processing steps does it take to make...

-A transistor?

-A full die (E.g. CPU)

The Transistor: How does this compute anything?

Basic Flow:

- Transistors -> Logic Gates
- Logic Gates -> Discrete Math
- Discrete Math -> Computing

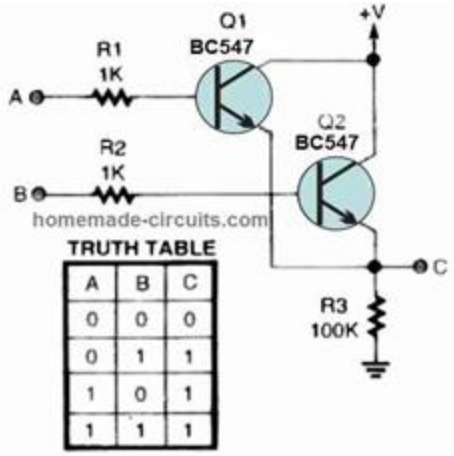


Fig. 5. By integrating the separate buffer circuits in a configuration like this, a straightforward OR gate can be created.

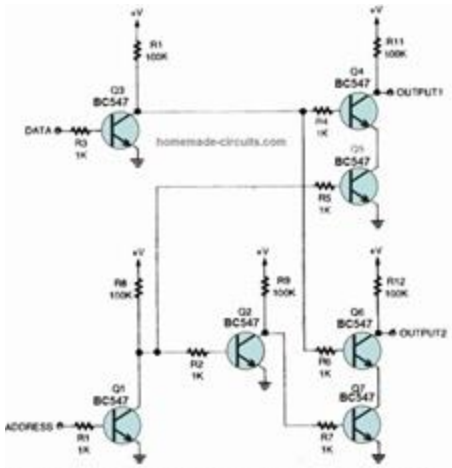
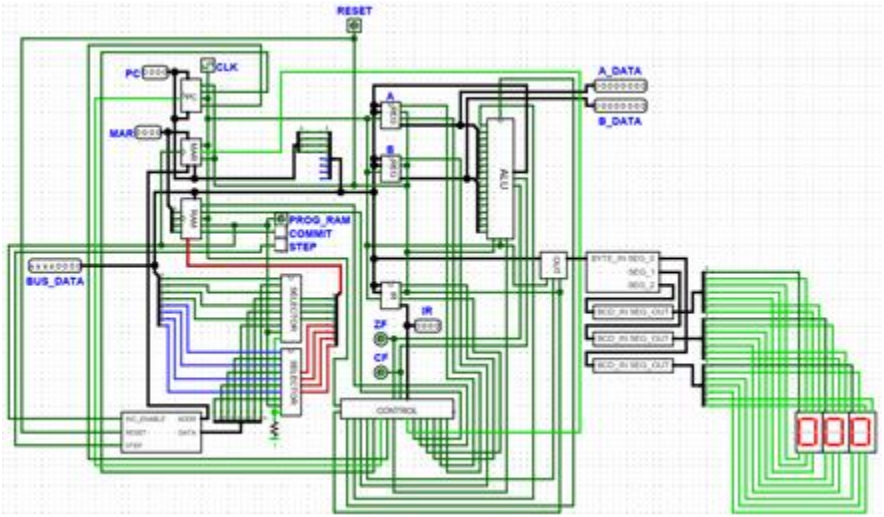


Figure 7 illustrates how the fundamental digital-logic circuits AND, NAND, OR, NOR, and inverter may be joined to create more intricate circuits that are able to carry out more complex operations. In this case, a triad of inverters and two NAND gates work together to create a 1-of-2 demultiplexer circuit.



MOSFET Fabrication Tools/Processes

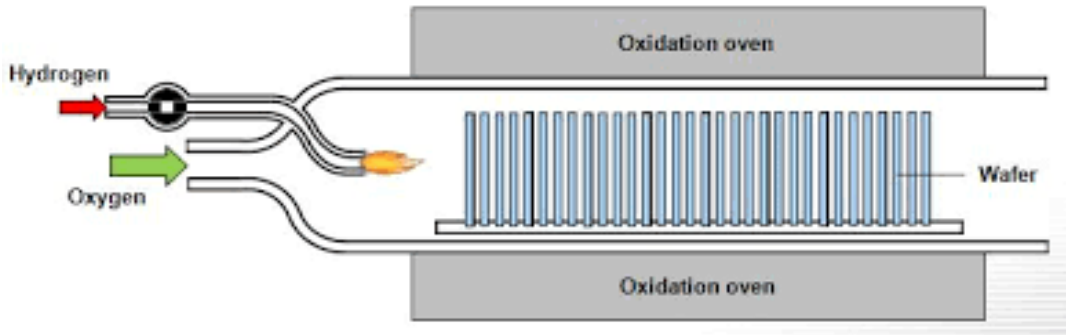
1. Oxide Growth
2. Lithography
3. Etching
4. Implantation/Doping
5. Deposition

Oxide Growth

Purpose: Create the gate insulator

Process:

- Oxide growth is the process of growing a thin layer of silicon dioxide (SiO_2) on the surface of a silicon wafer.
- This layer is typically created by exposing the silicon to oxygen or steam at high temperatures in a furnace.
- Silicon dioxide acts as an insulator between the gate and the semiconductor, preventing current leakage and controlling the electrical behavior of the transistor.



Types of Oxide Growth:

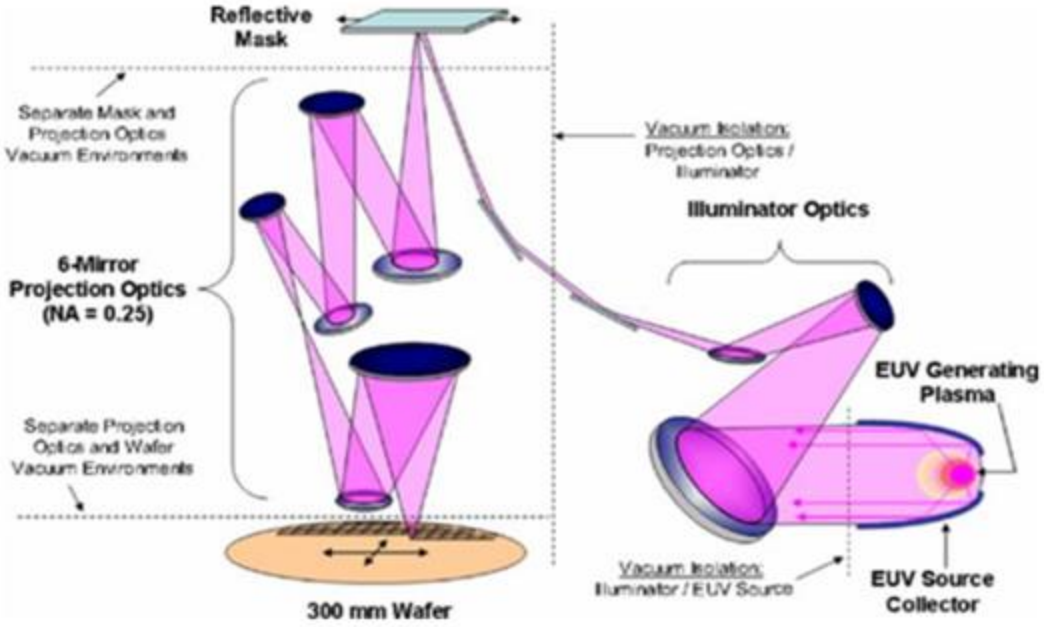
- **Thermal Oxidation**: Direct oxidation in a furnace by reacting silicon with dry or wet oxygen.
- **Chemical Vapor Deposition (CVD)**: A method where oxide is deposited onto the wafer surface using a chemical reaction.

Lithography

Purpose: Define patterns on the wafer for circuit elements.

Process:

- Lithography is a method used to transfer patterns from a mask to a wafer.
- It involves applying a **photoresist** layer on the wafer, which is sensitive to light.
- The wafer is then exposed to ultraviolet (UV) light through a **photomask**, which defines the pattern of the circuit.



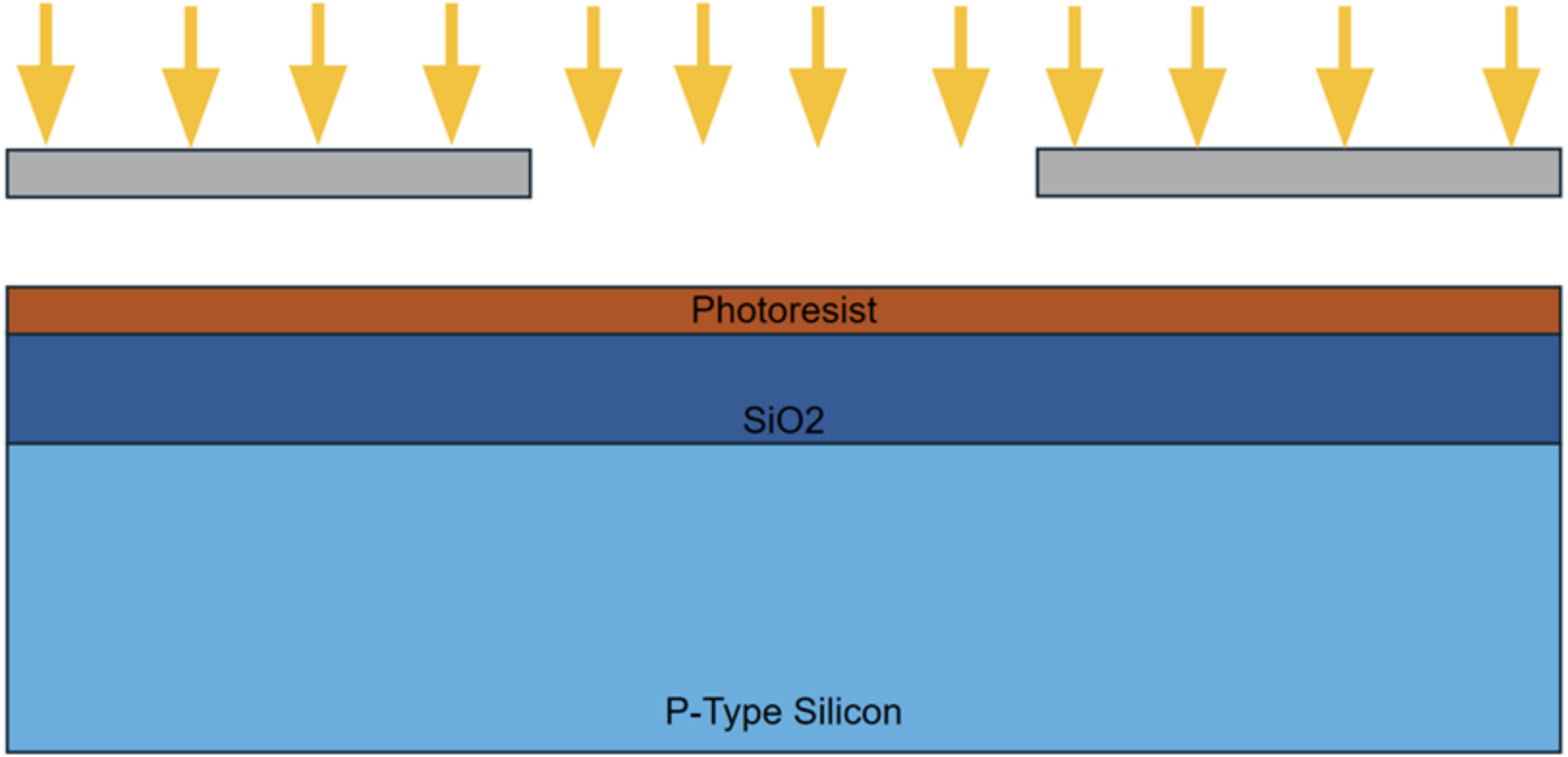
Types of Lithography:

- **Photolithography**: Uses UV light to transfer the mask pattern.
- **E-Beam Lithography**: Uses a focused beam of electrons to write custom patterns, often used in research or prototype production.
- **Extreme Ultraviolet (EUV) Lithography**: A cutting-edge technology for producing smaller features in advanced semiconductor manufacturing.

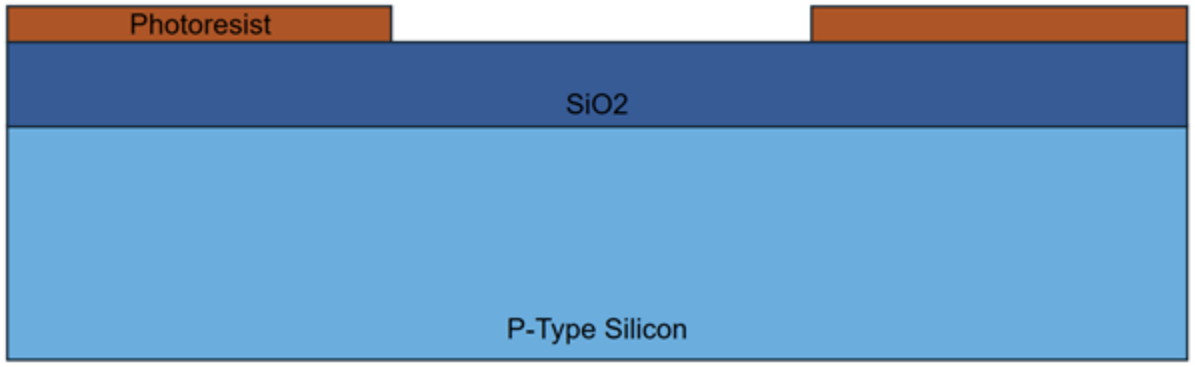
Lithography - Photoresists

Photoresist: A chemical that becomes stronger or weaker when exposed to light.

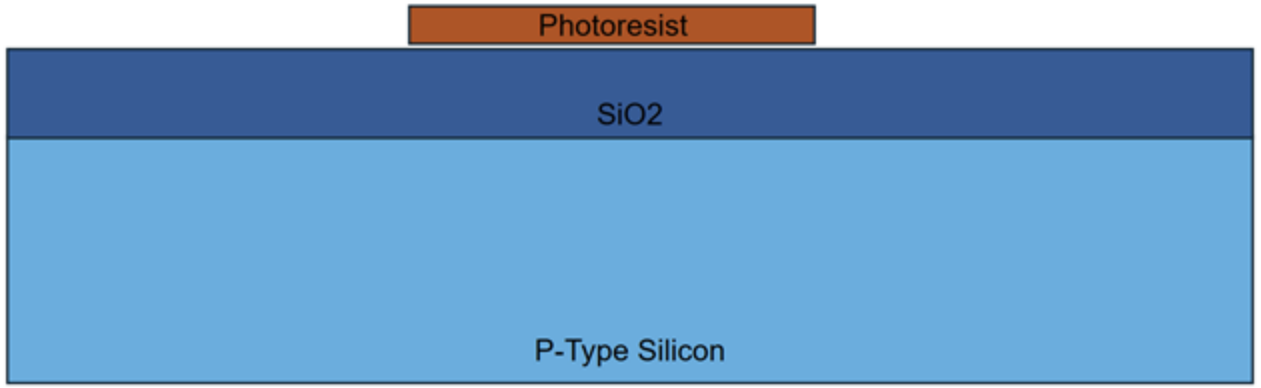
Positive	Negative
Long Polymer Chains	Small Molecules
Light Breaks Molecular Bonds	Light Forms Molecular Bonds
Becomes **Weaker** When Exposed	Becomes **Stronger** When Exposed



Positive

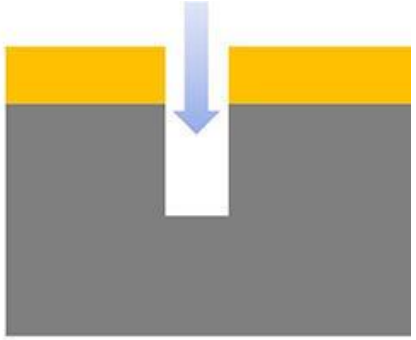


Negative



Etching

Isotropic Etching



Anisotropic Etching

Purpose: Remove material to define specific structures on the wafer.

Process:

- Etching is used to remove layers of material from the wafer to create the desired patterns defined by lithography.
- It can be used to selectively remove exposed areas of the wafer or thin films after the photoresist has been patterned.
- The etching process needs to be precise to ensure that only specific areas are removed while maintaining the integrity of other regions.

Types of Etching:

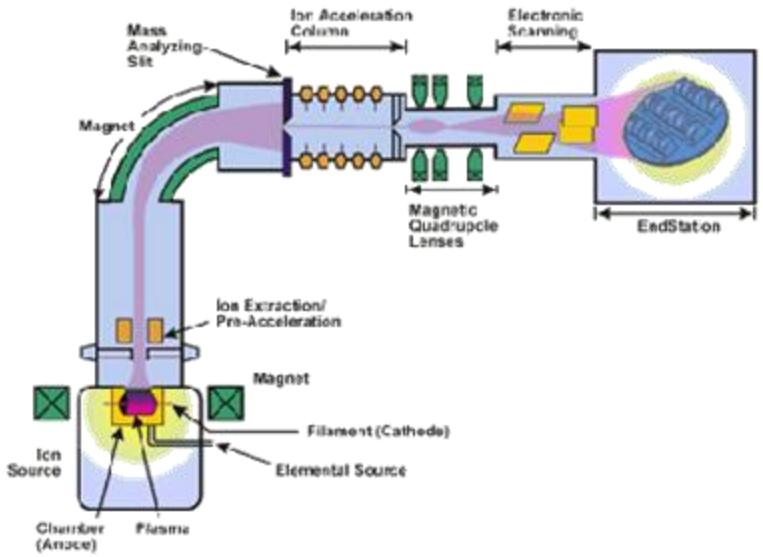
- **Wet Etching**:
  - Uses liquid chemicals (acids or bases) to dissolve materials.
  - Offers good selectivity but may lack precision for small-scale features.
- **Dry Etching**:
  - Uses gases or plasmas (ionized gases) to etch materials.
  - More precise and widely used in advanced semiconductor manufacturing.
  - Examples include **Reactive Ion Etching (RIE)**, which combines chemical and physical processes for better control.

Implantation/Doping

Purpose: Modify the electrical properties of the semiconductor by introducing impurities (dopants).

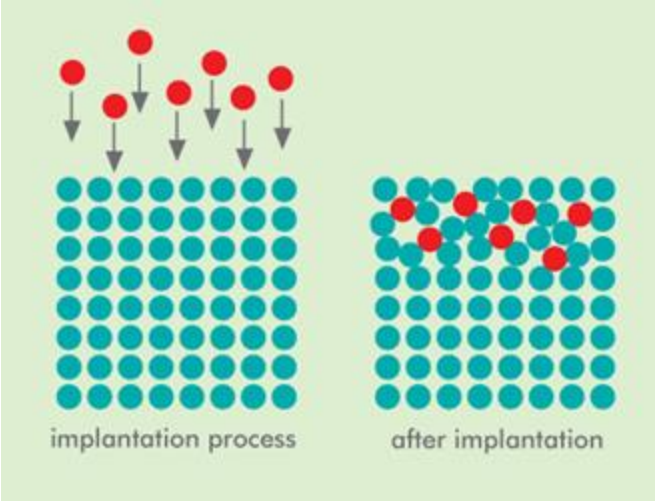
Process:

- Doping introduces atoms of elements such as boron (for p-type) or phosphorus (for n-type) into the silicon wafer to alter its conductivity.
- This is done by **ion implantation**, where ions are accelerated and embedded into the silicon surface at high velocities.
- After implantation, the wafer is usually heated (annealed) to repair the crystal structure and activate the dopants, allowing them to take their places in the lattice.



Types of Dopants:

- **N-type Doping**: Adds electrons to the material by introducing elements like phosphorus or arsenic, which have more electrons than silicon.
- **P-type Doping**: Creates holes (positive charge carriers) by adding elements like boron, which have fewer electrons than silicon.

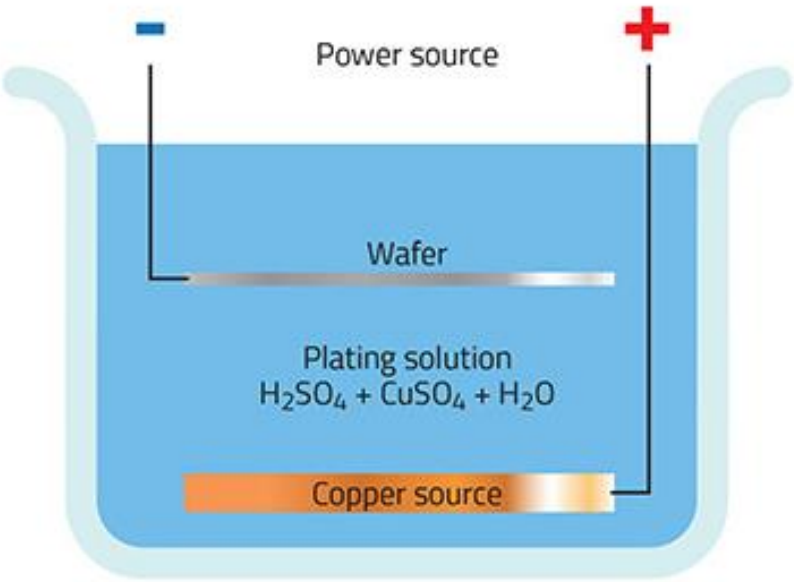


Material Deposition

Purpose: Place down new material to enable creation of complex structures

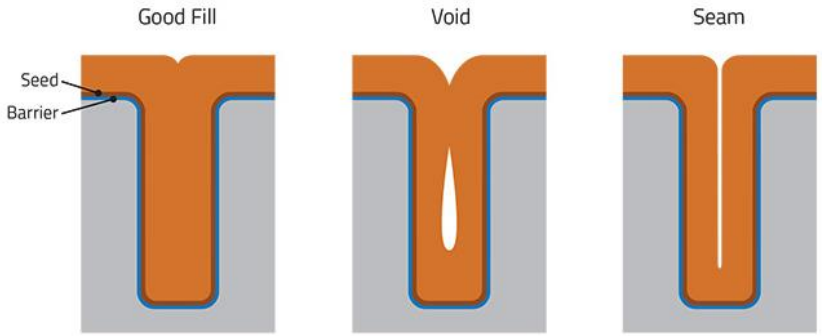
Process:

- Metal deposition involves placing a thin layer of metal onto the surface of the wafer to create conductive connections.
- Metals like aluminum, copper, or tungsten are commonly used because of the high conductivity.
- After deposition, the metal is patterned using lithography and etching to form t desired circuit interconnects.



Types of Metal Deposition:

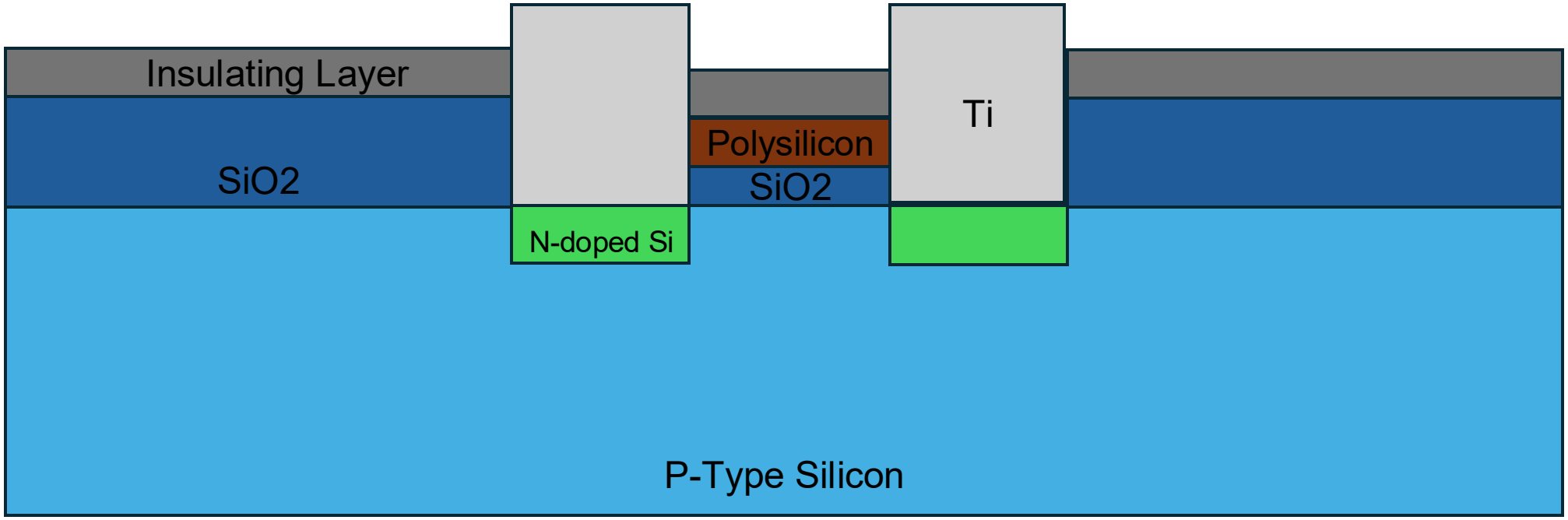
- **Physical Vapor Deposition (PVD)**:
  - Metals are vaporized in a vacuum and deposited as a thin film on the wafer.
  - Common methods include **Sputtering** and **Evaporation**.
- **Chemical Vapor Deposition (CVD)**:
  - A chemical reaction is used to deposit metal onto the wafer, often resulting in more uniform layers.
- **Electroplating**:
  - A layer of metal, commonly copper, is deposited on the wafer through an electrochemical process.



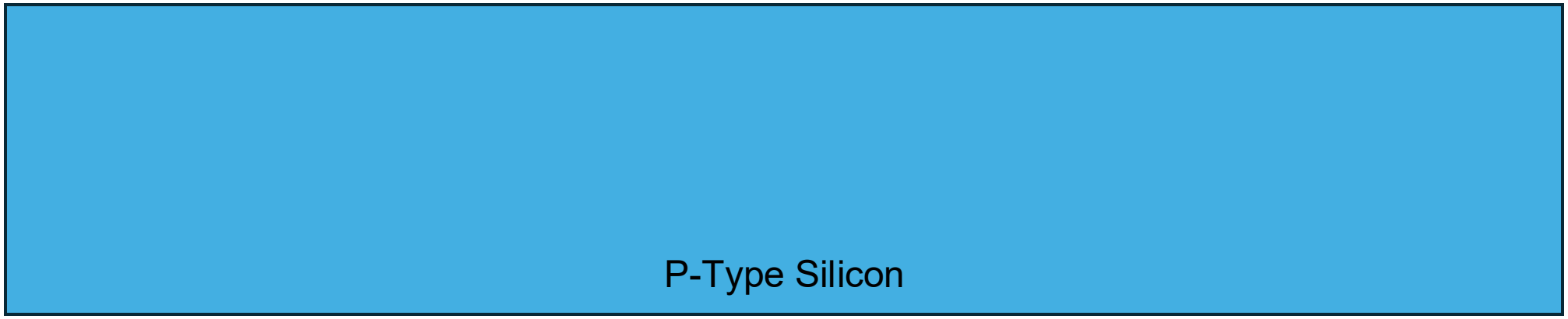
Make sense?

Let’s make a transistor

Final Goal

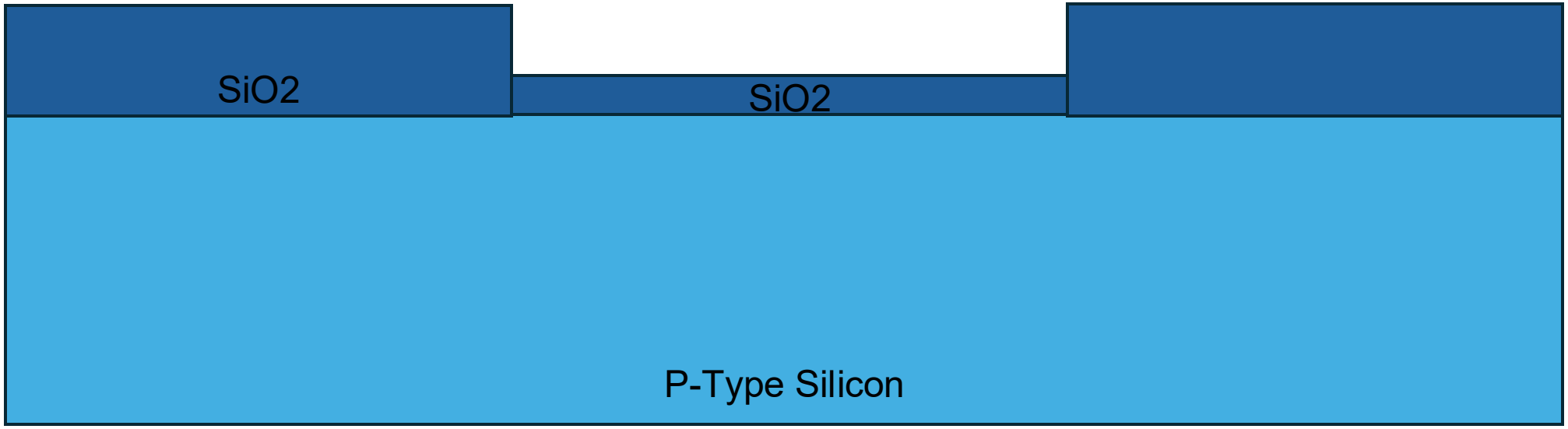

Insulating Layer
SiO2
Polysilicon
SiO2
Ti
N-doped Si
P-Type Silicon

0) Silicon Wafer arrives in fab

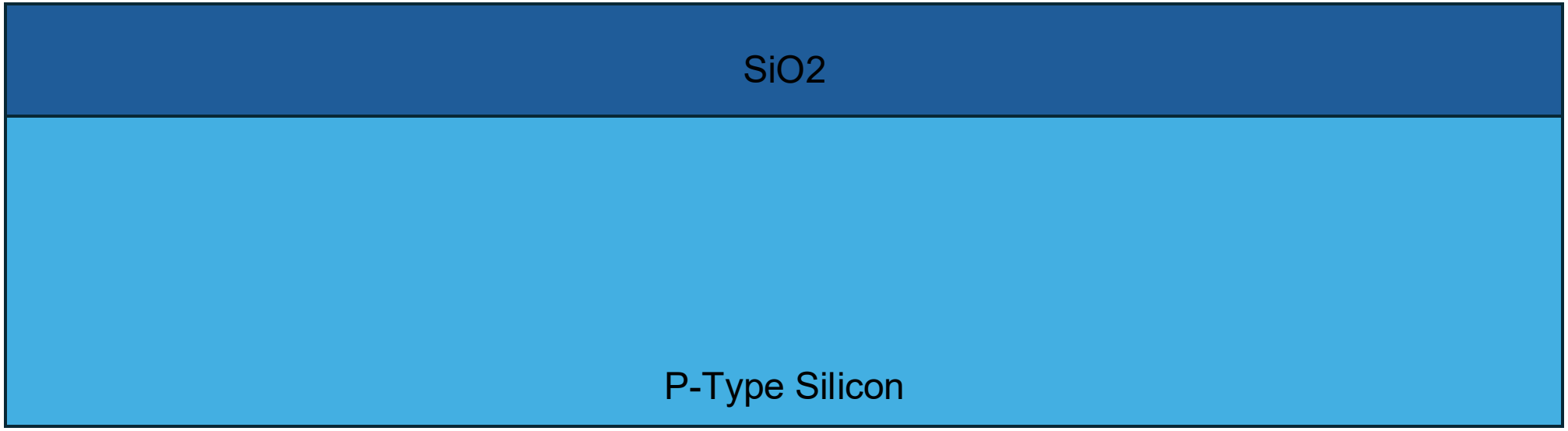


Field Oxide Formation

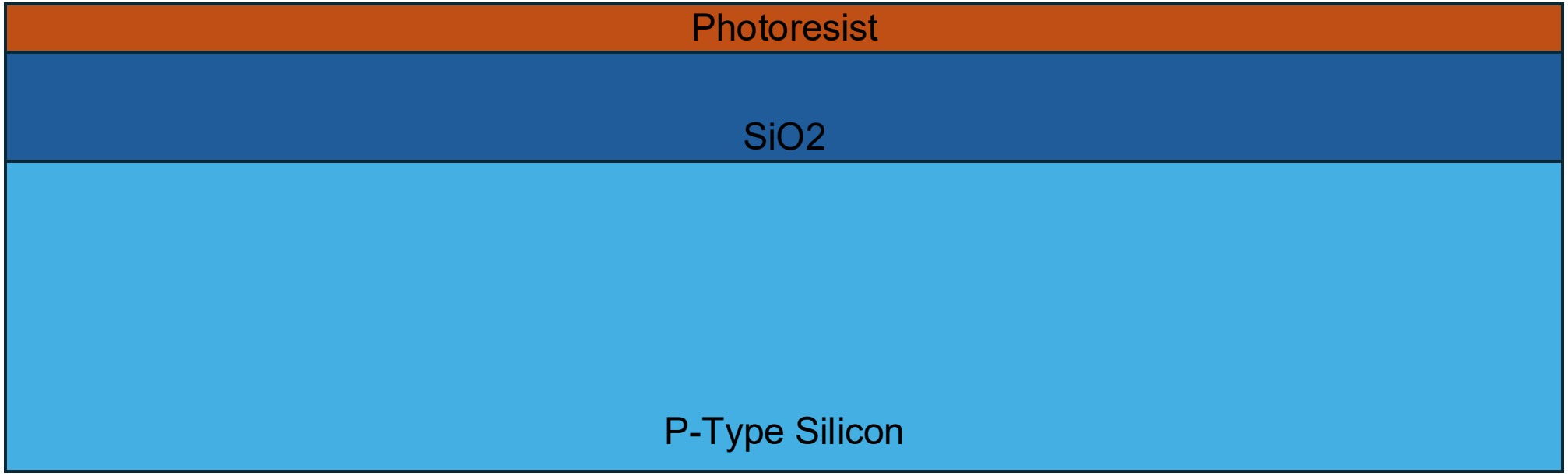
Goal:



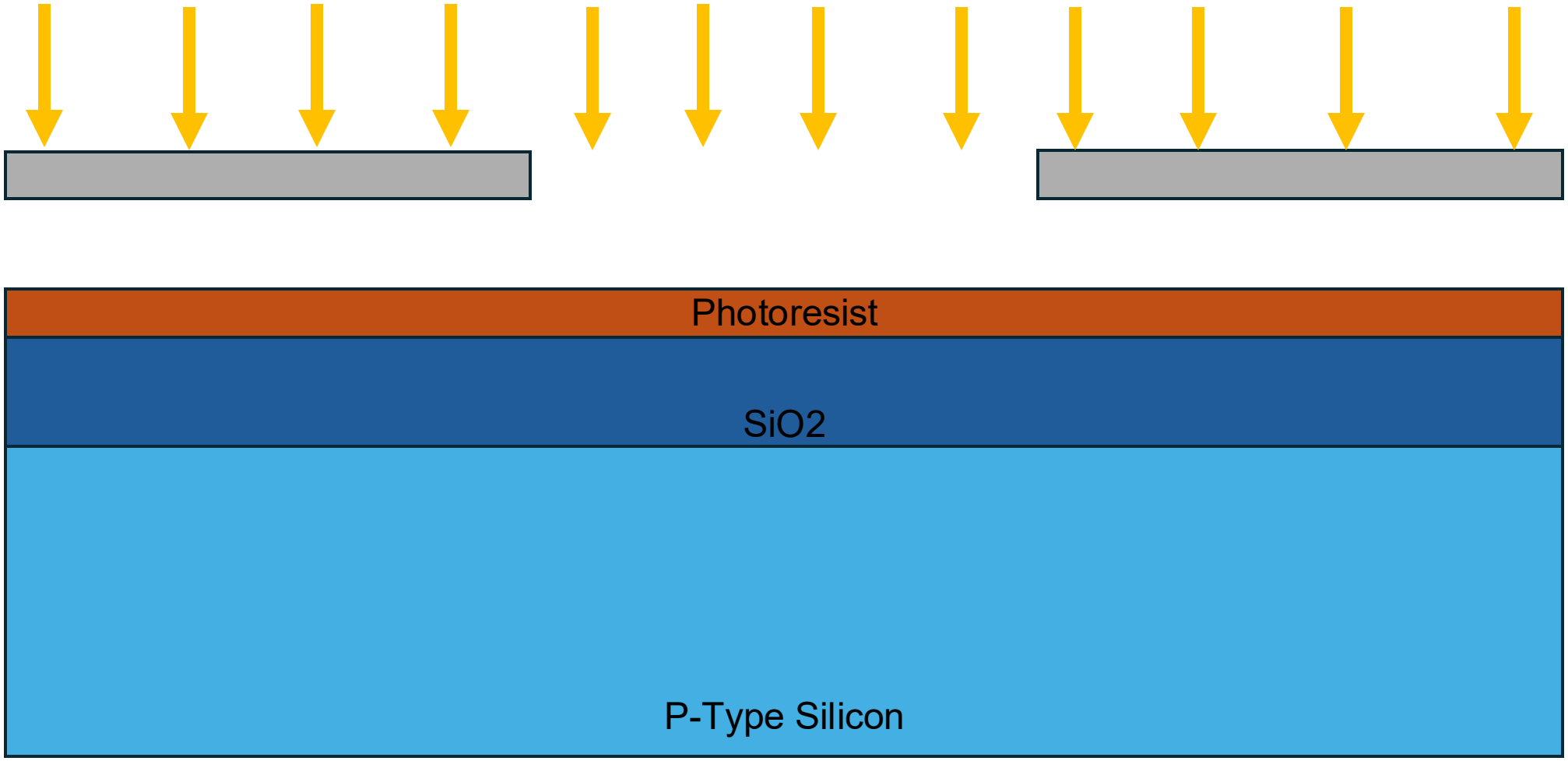
1) Thermal Oxide Growth



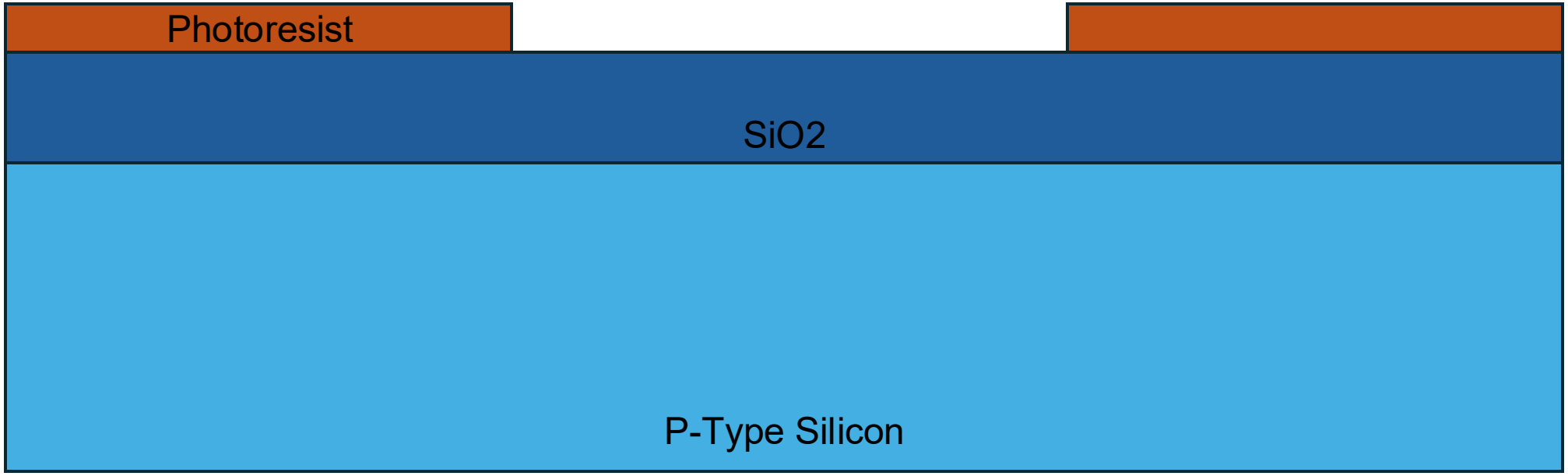
2) Spin-coat Photoresist



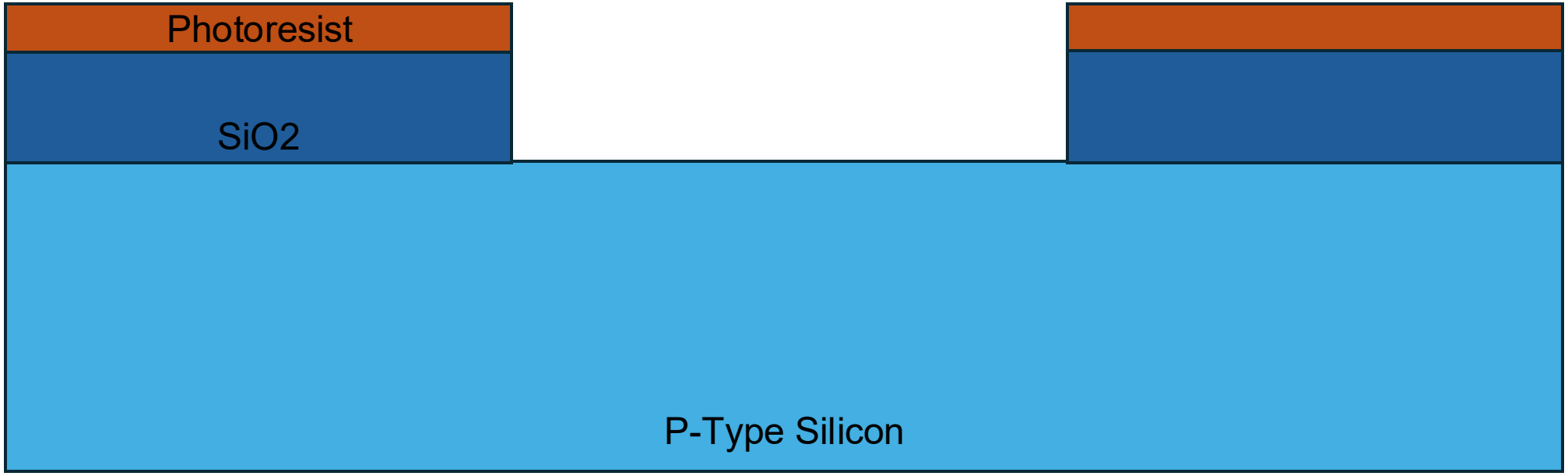
3) Photoresist exposed to light through mask, developed



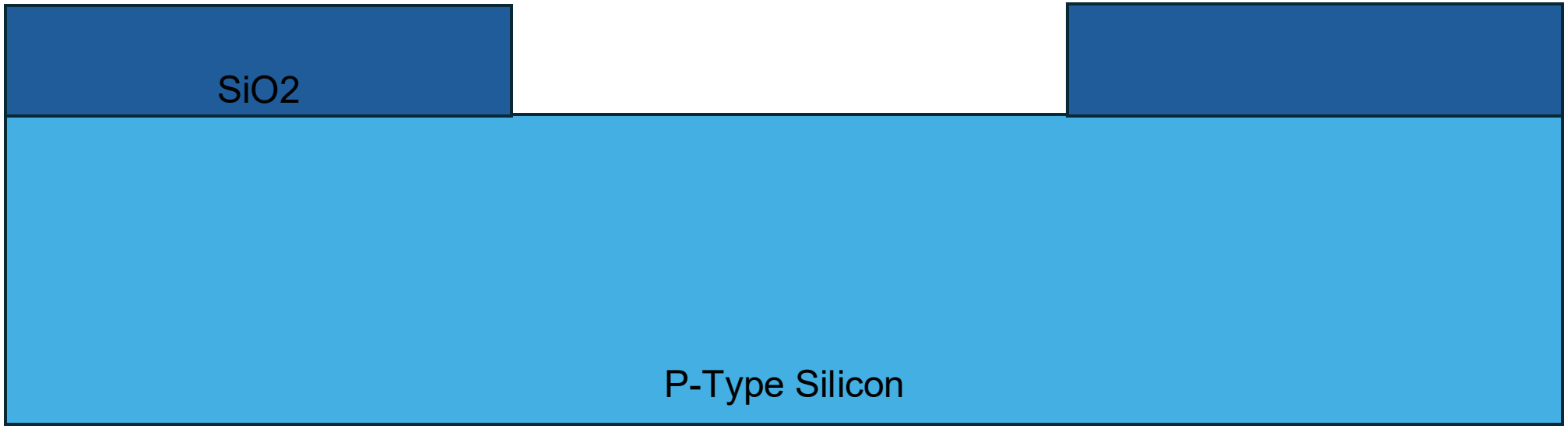
4) Uncured photoresist washed away



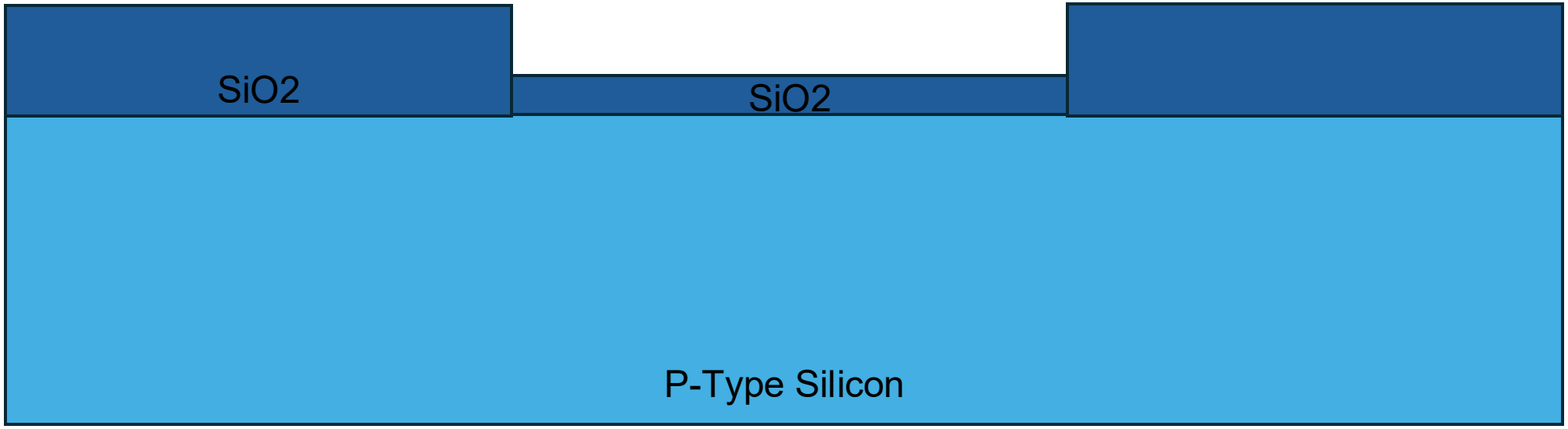
5) SiO2 is etched to substrate below



6) Photoresist is removed via acid solution

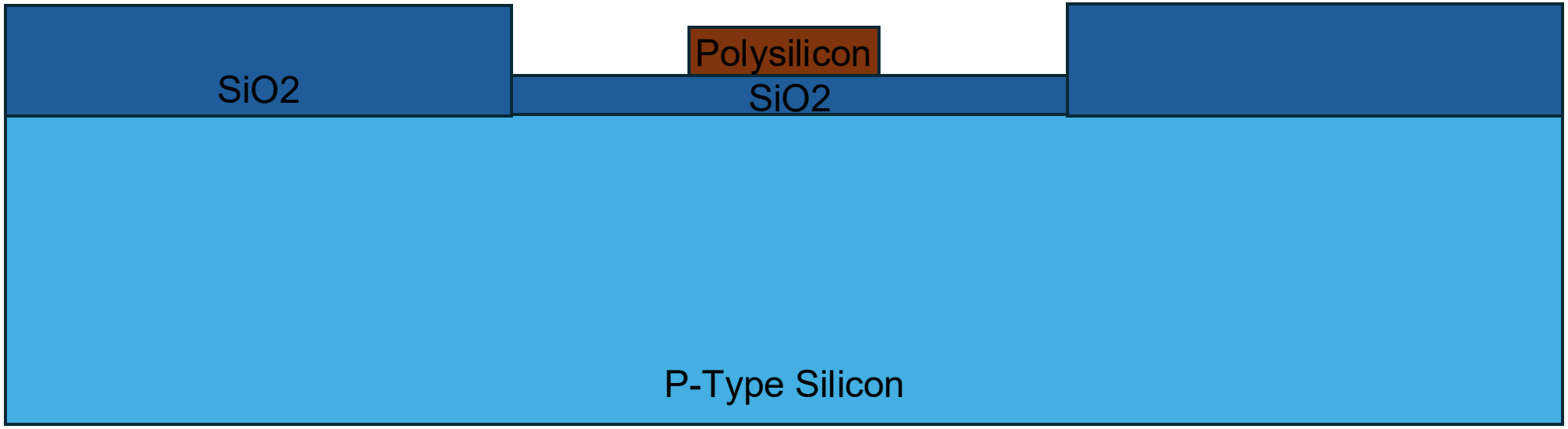


7) Thin layer of SiO2 is deposited (Thermal Oxide Growth)

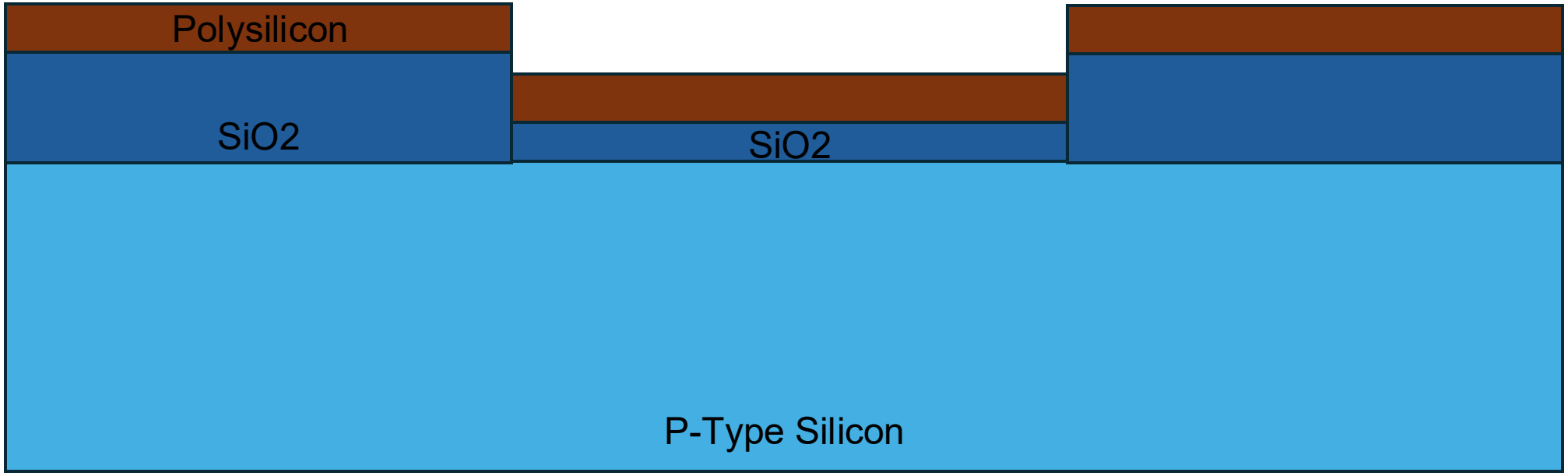


Gate Creation

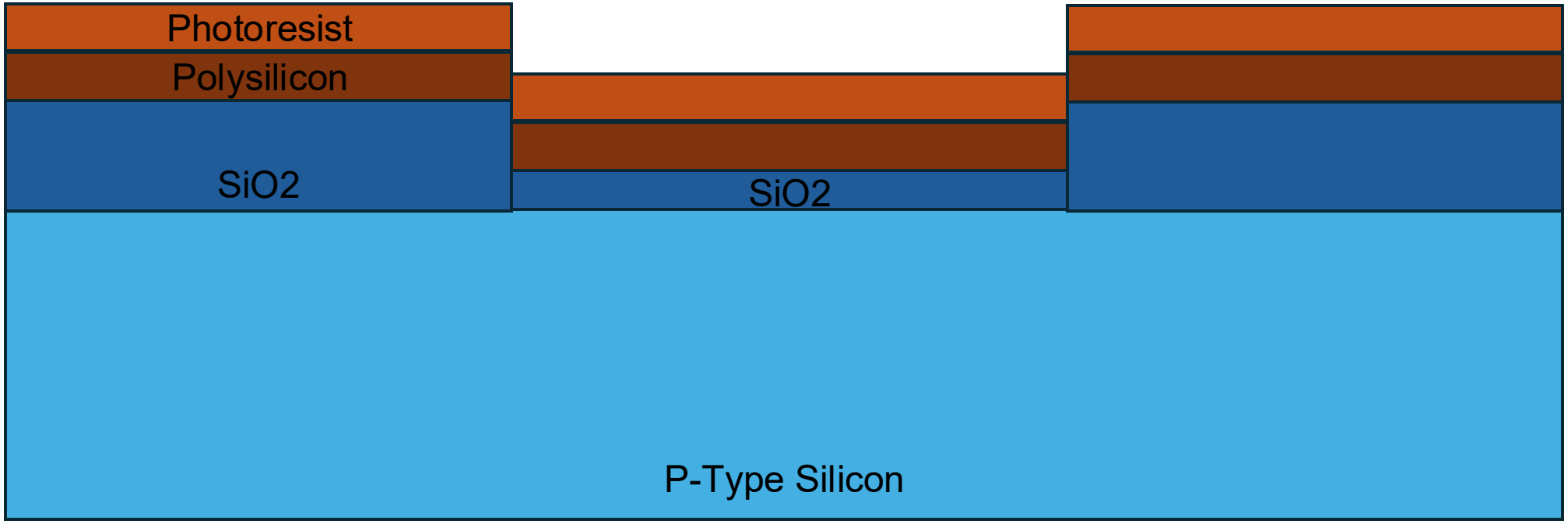
Goal:



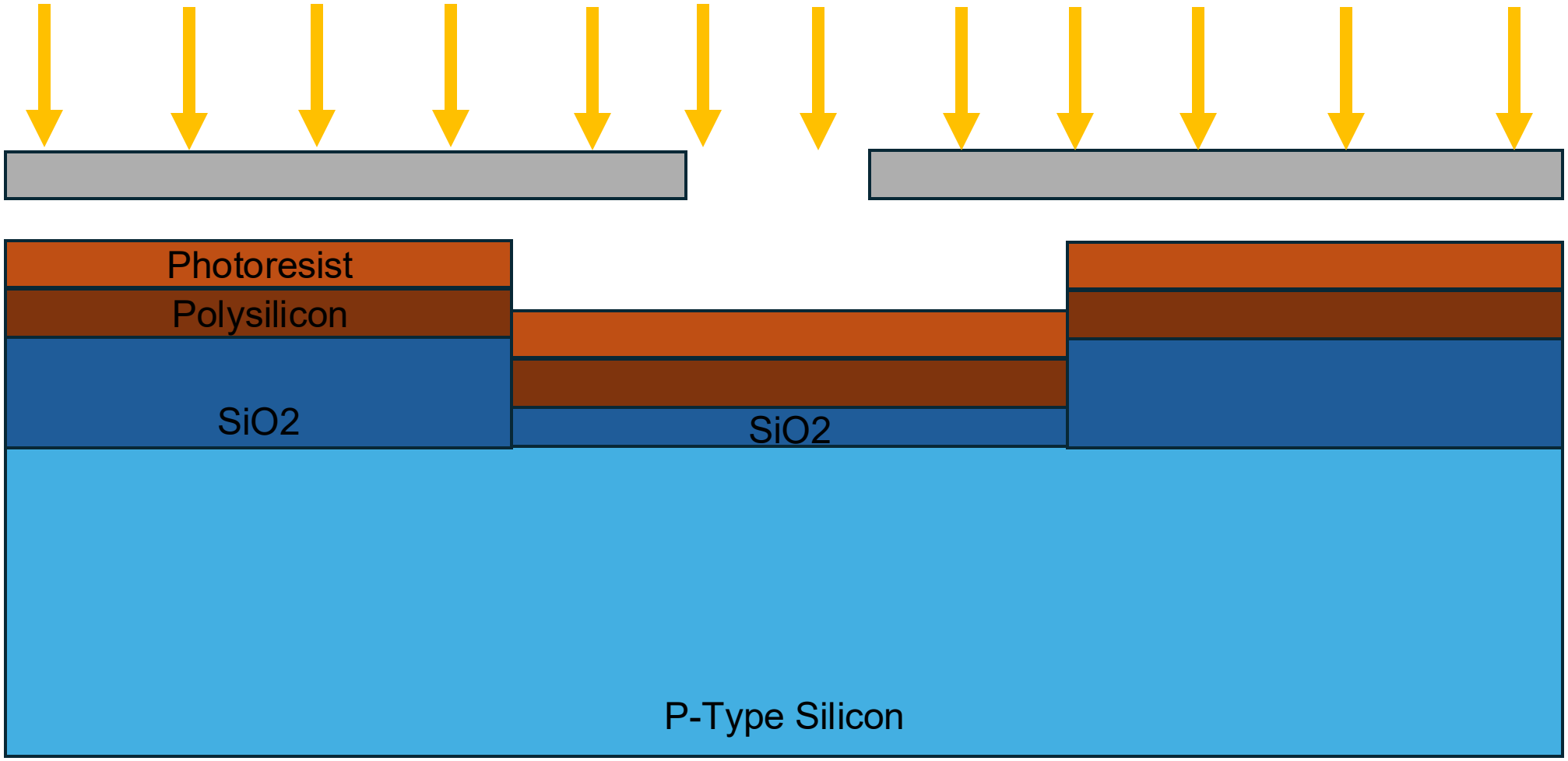
8) Polysilicon is grown on wafer (LPCVD)



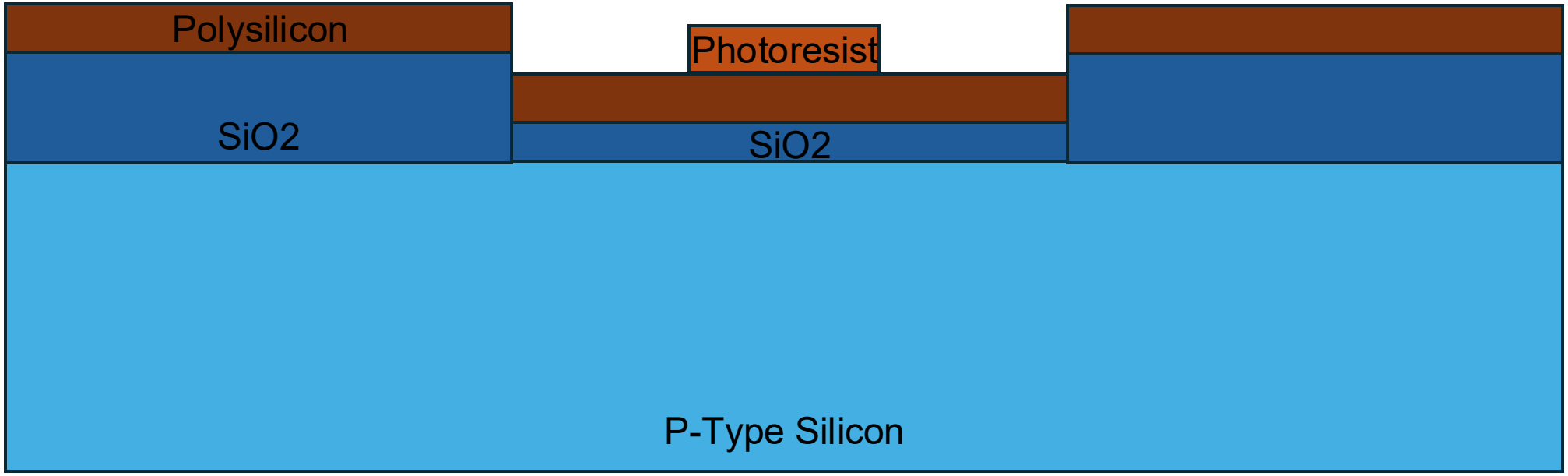
9) Photoresist is spun on surface



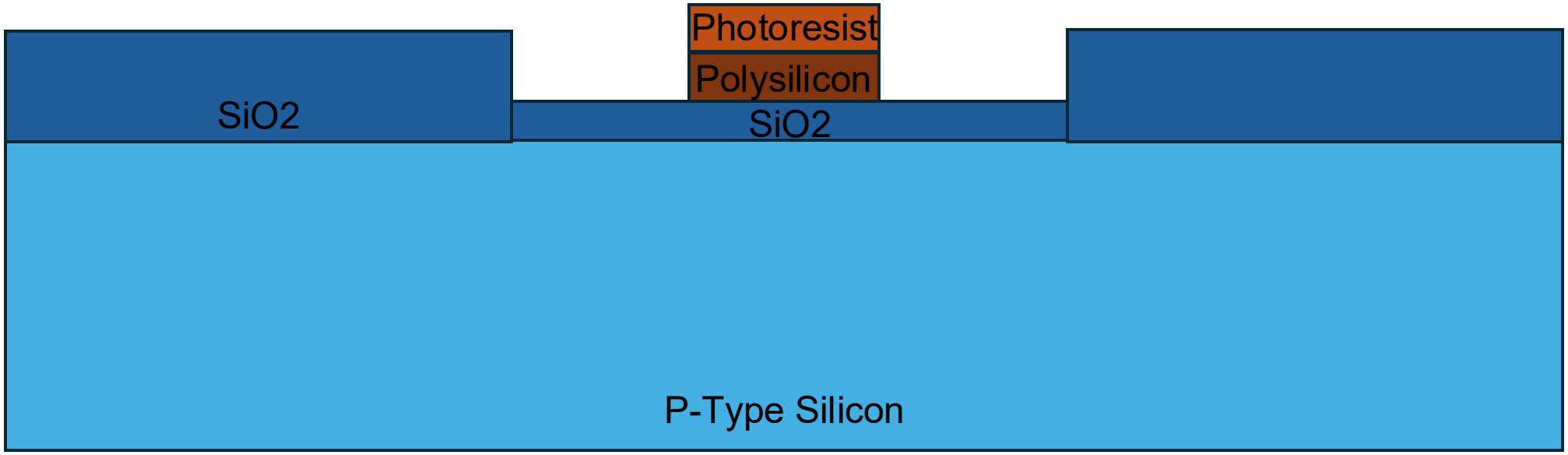
10) Exposed to light, developed



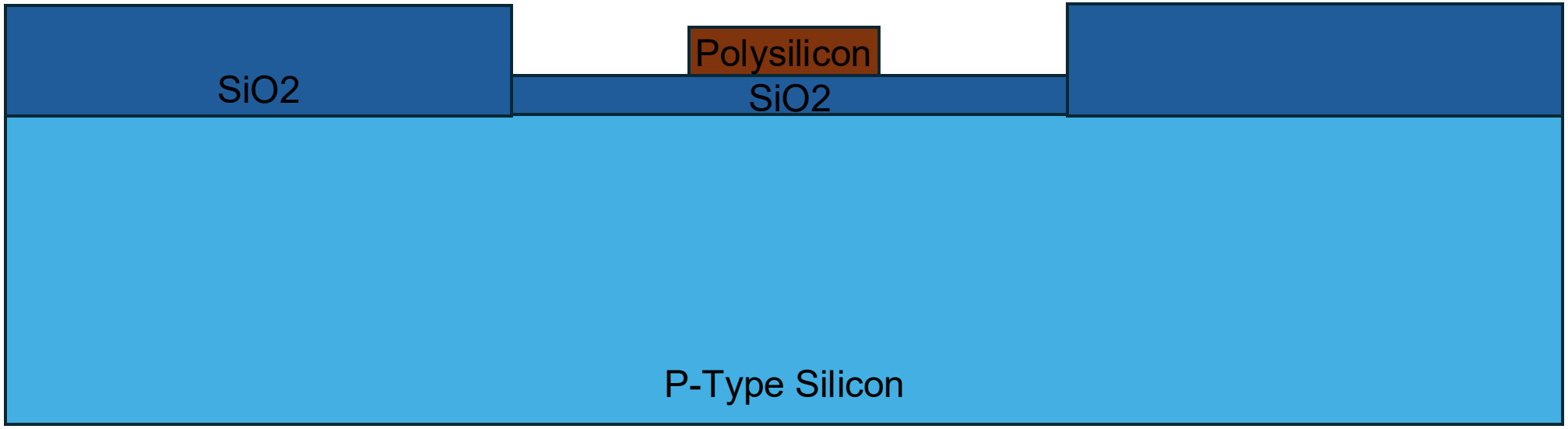
11) Photoresist is developed, uncured resist washed off



12) Polysilicon is etched, leaving SiO2 below

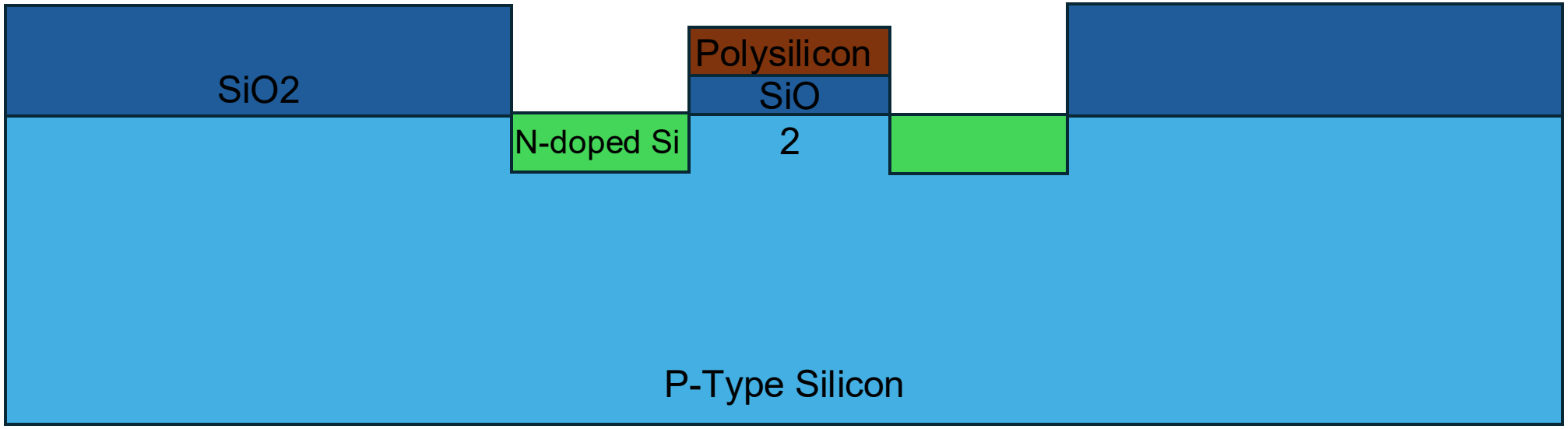


13) Acid wash removes Photoresist

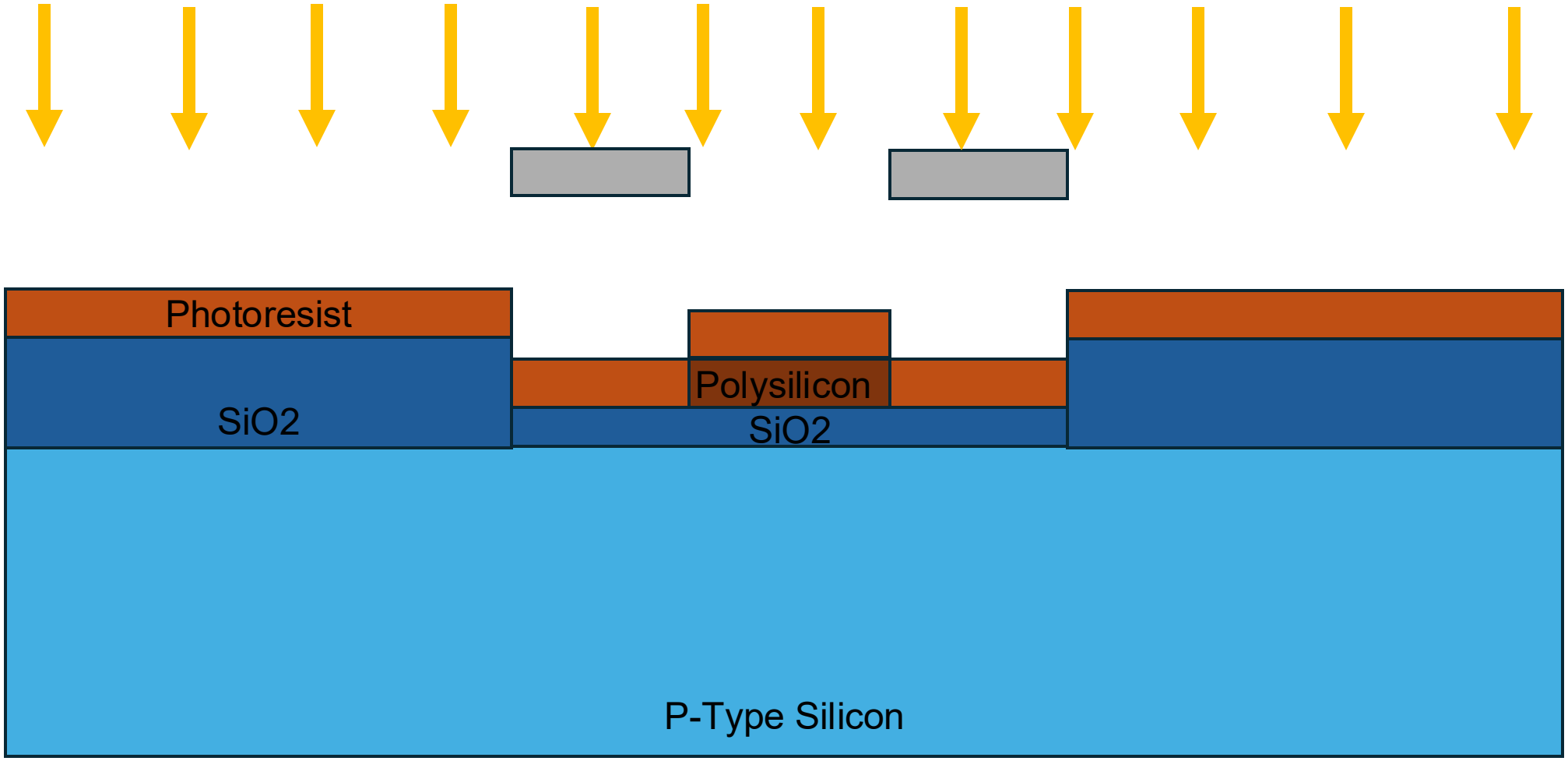


Source/Drain Doping

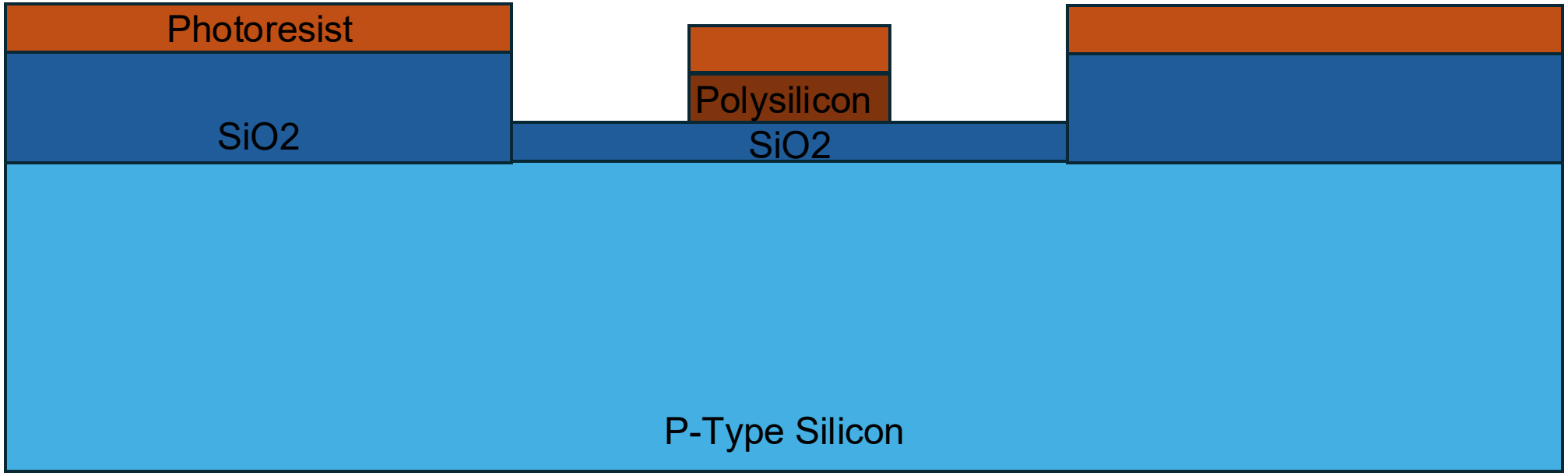
Goal:



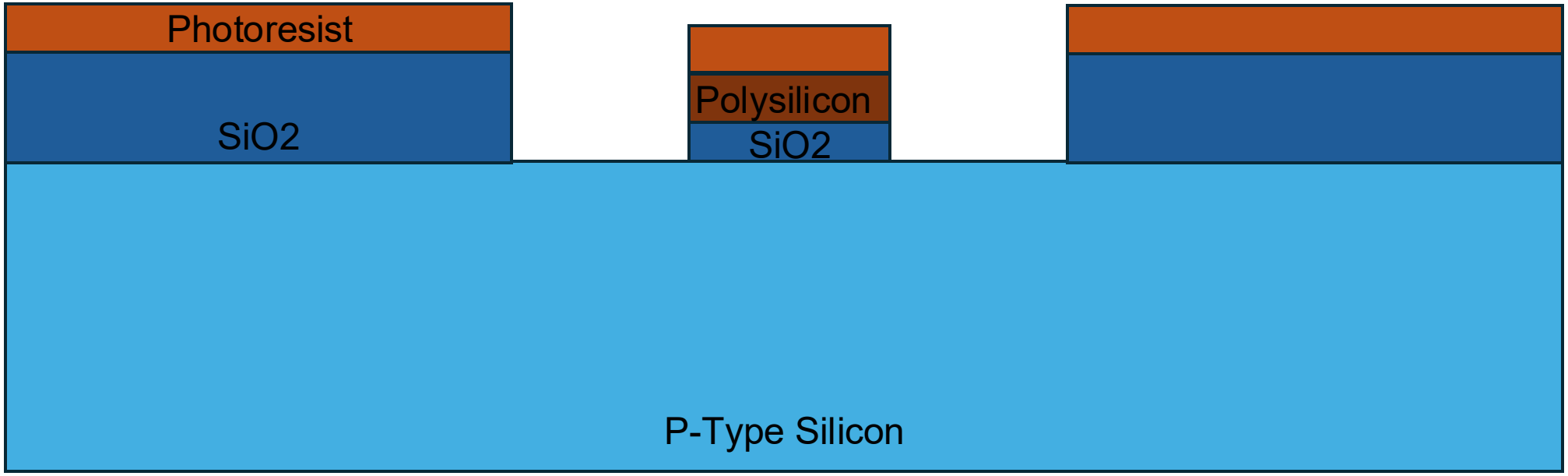
14) More photoresist spun on



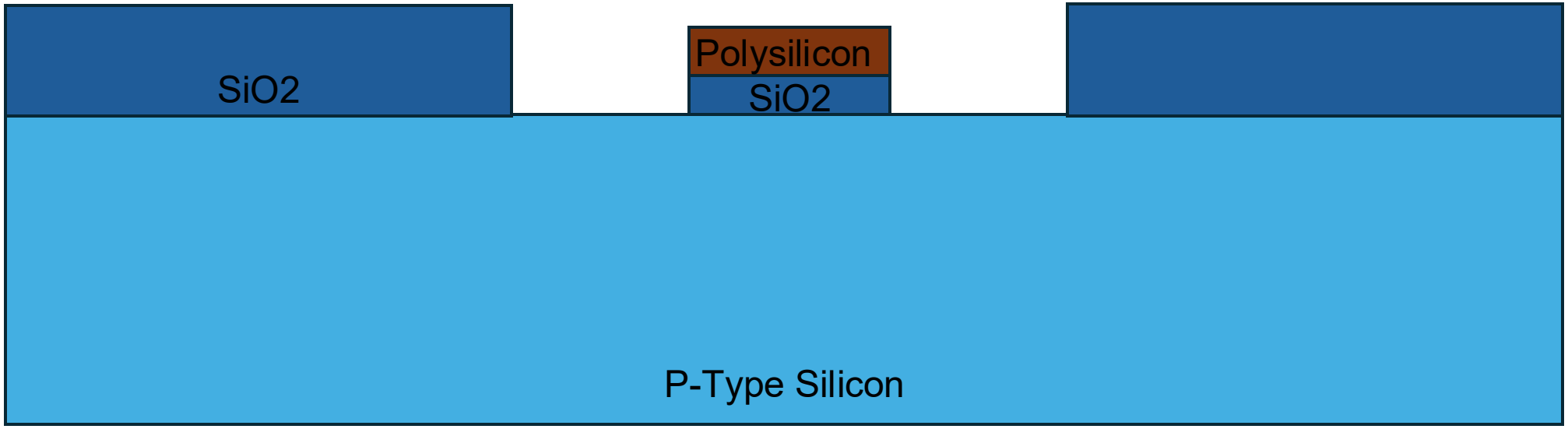
15) Photoresist developed, cleaned



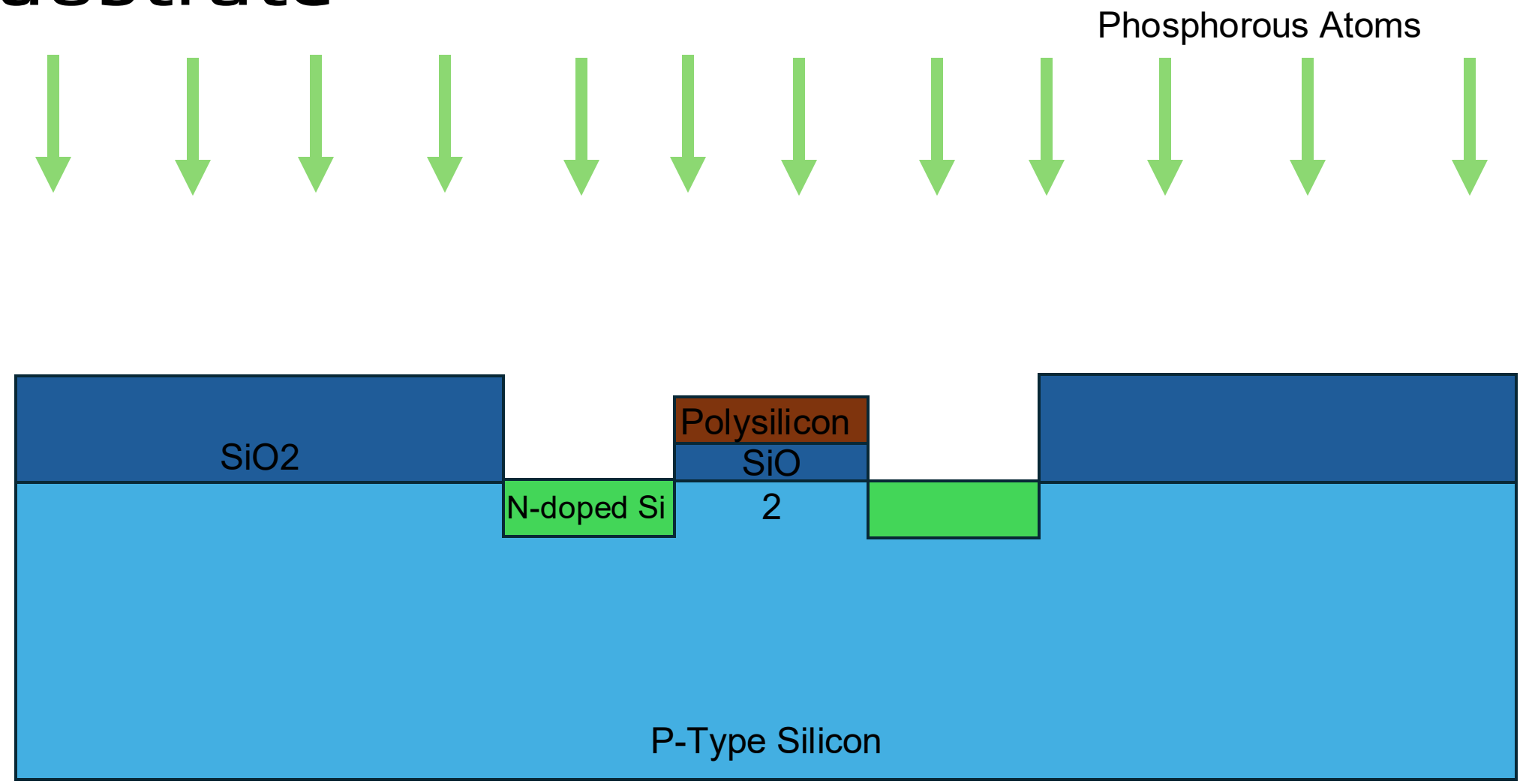
16) SiO2 layer is etched, revealing bare silicon below



17) Photoresist is acid washed

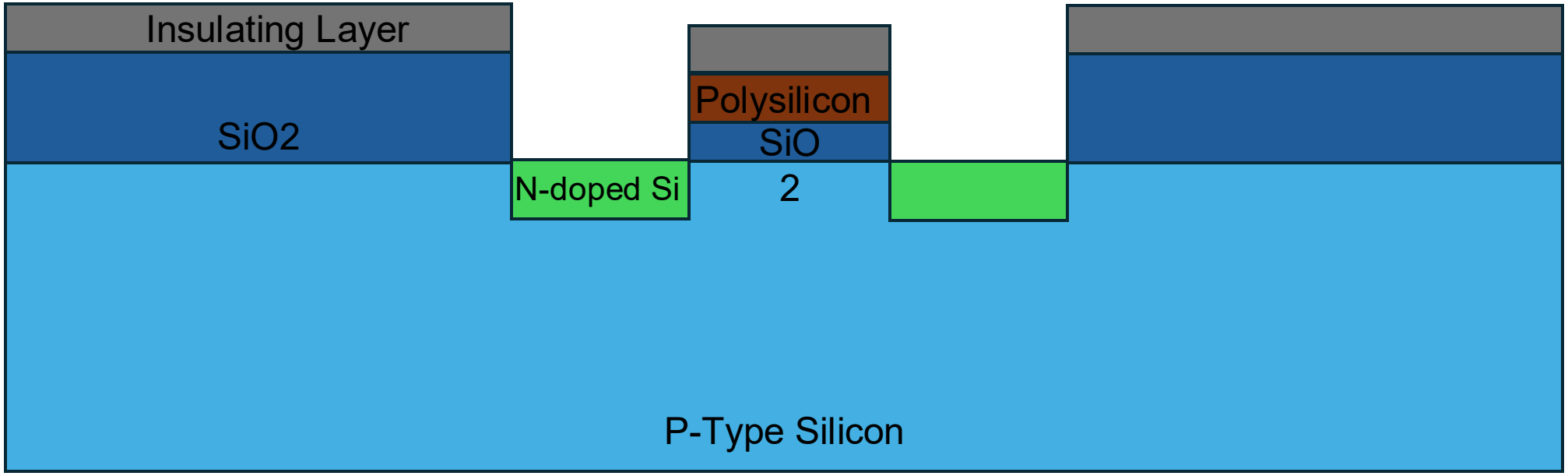


18) Phosphorous is used to dope substrate

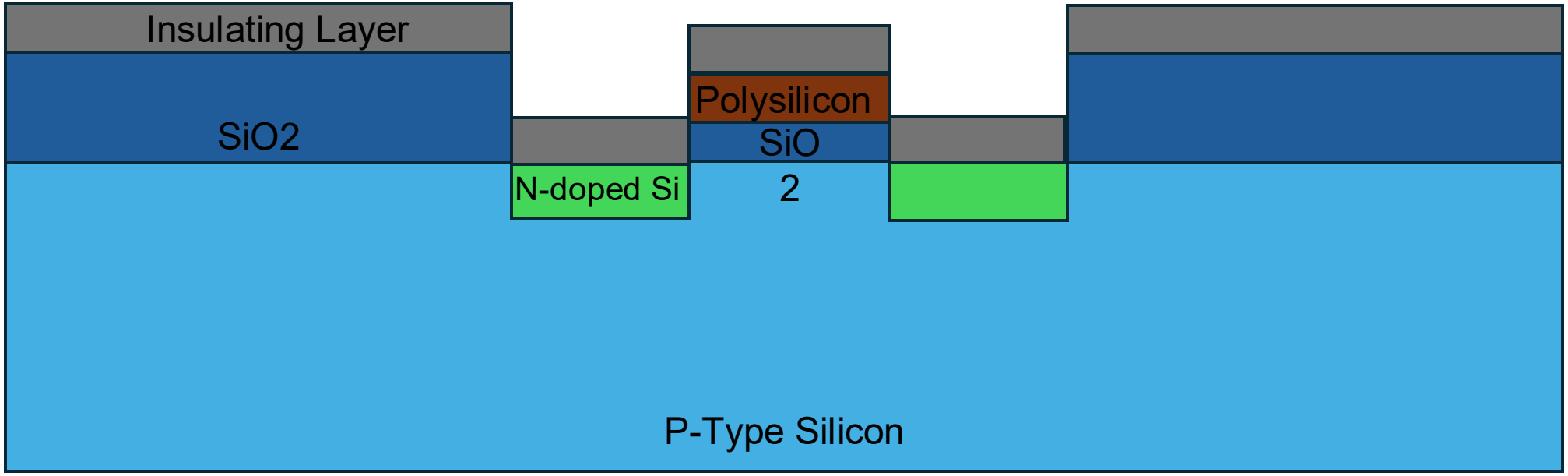


Metal Insulation Layer Creation

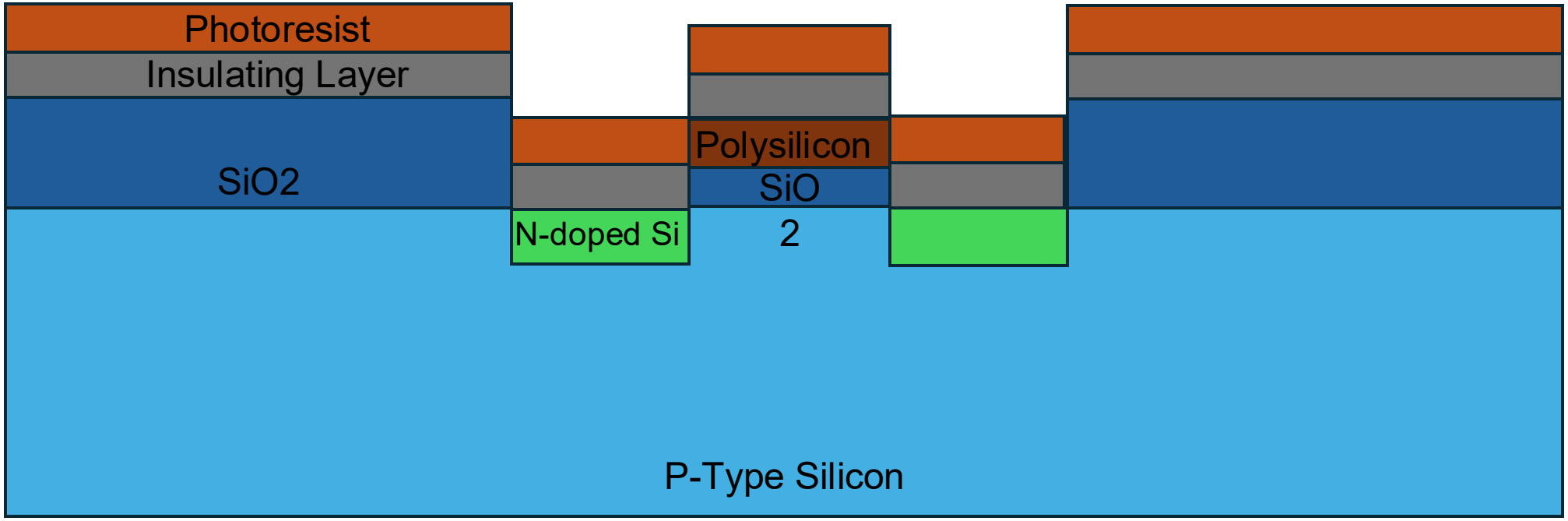
Goal:


Insulating Layer
SiO2
Polysilicon
SiO
2
N-doped Si
P-Type Silicon

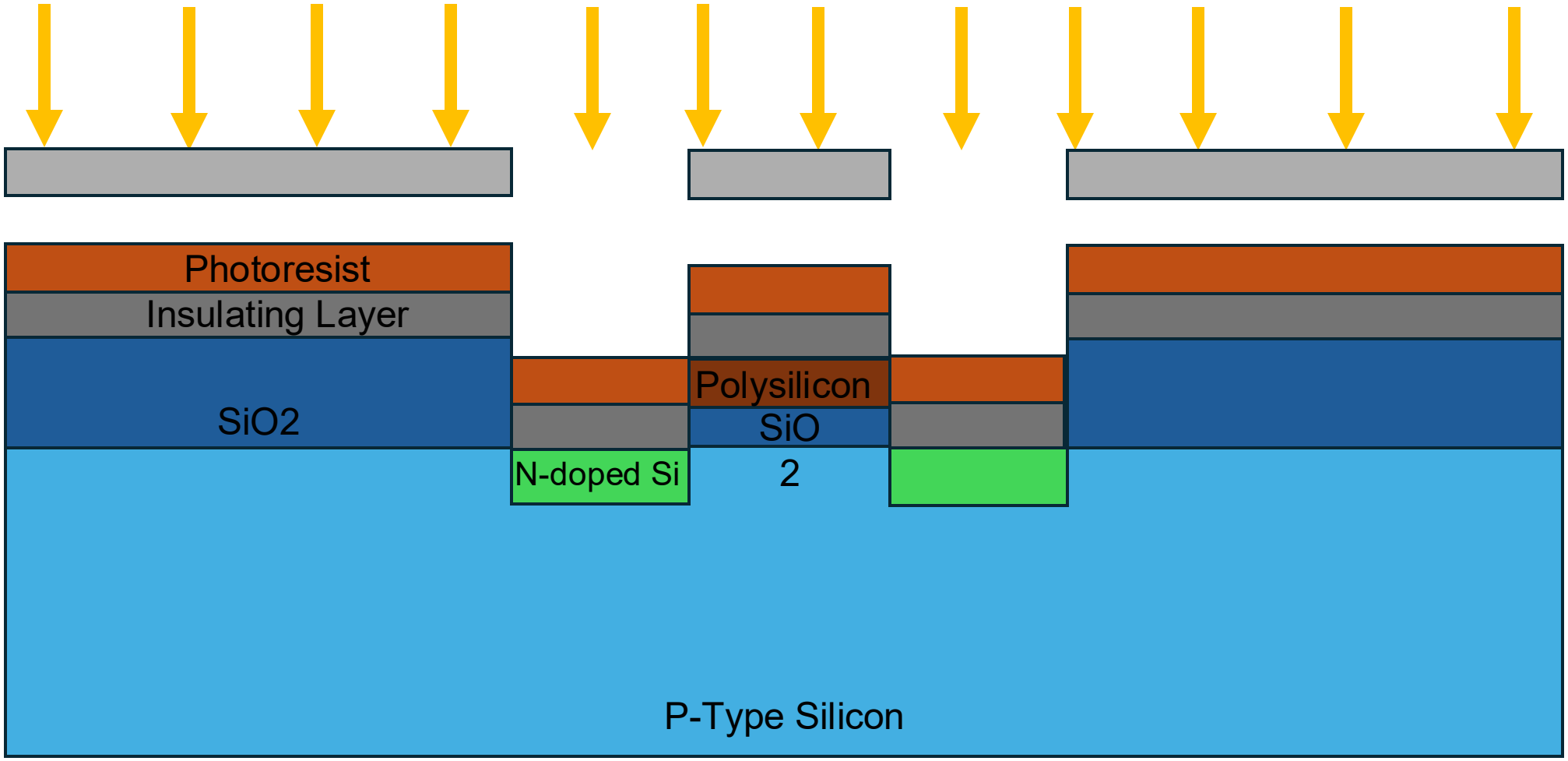
19) Insulating Oxide is deposited on surface



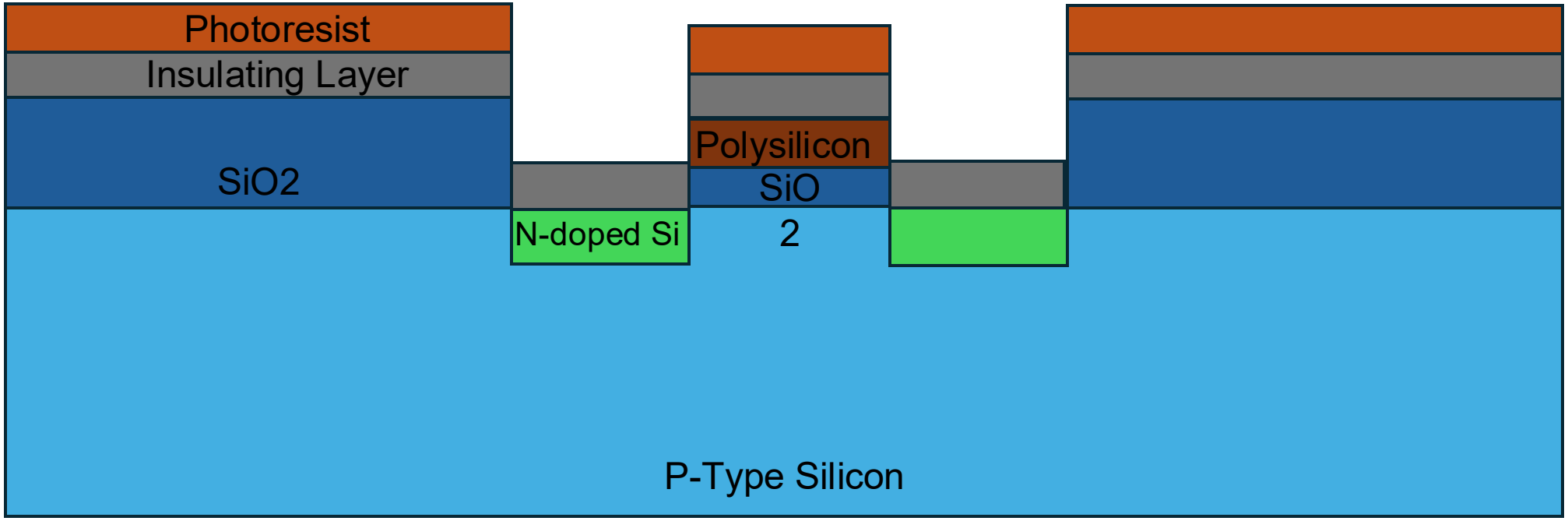
20) Photoresist spun on again



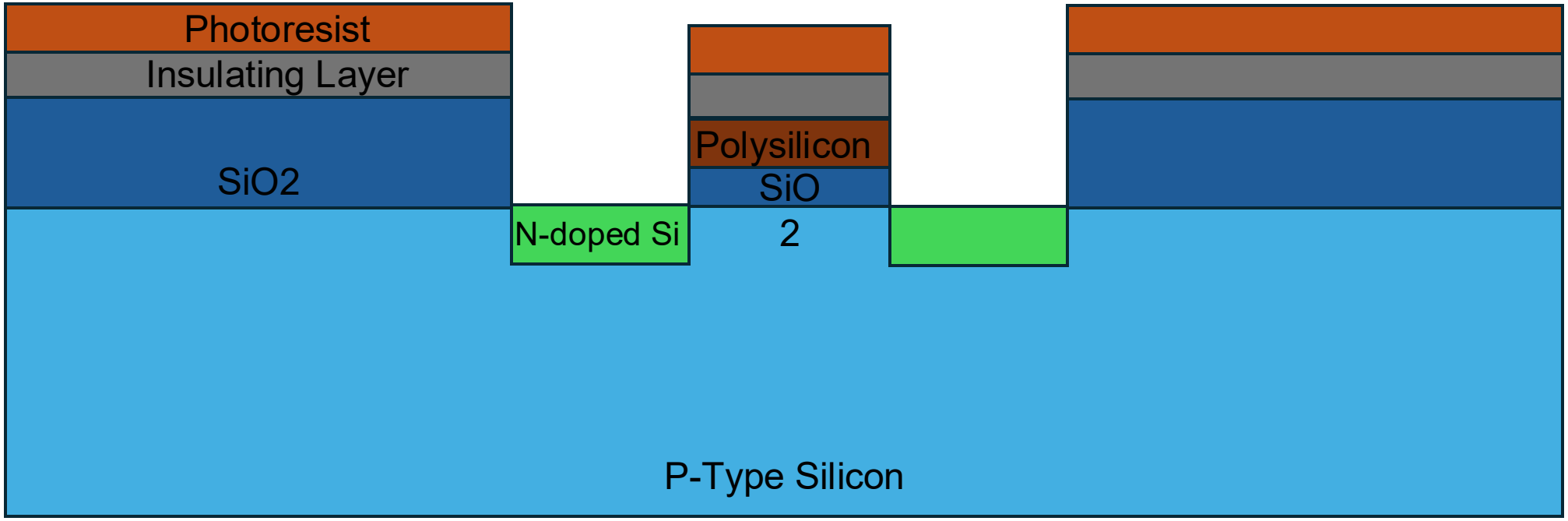
21) Exposed Again



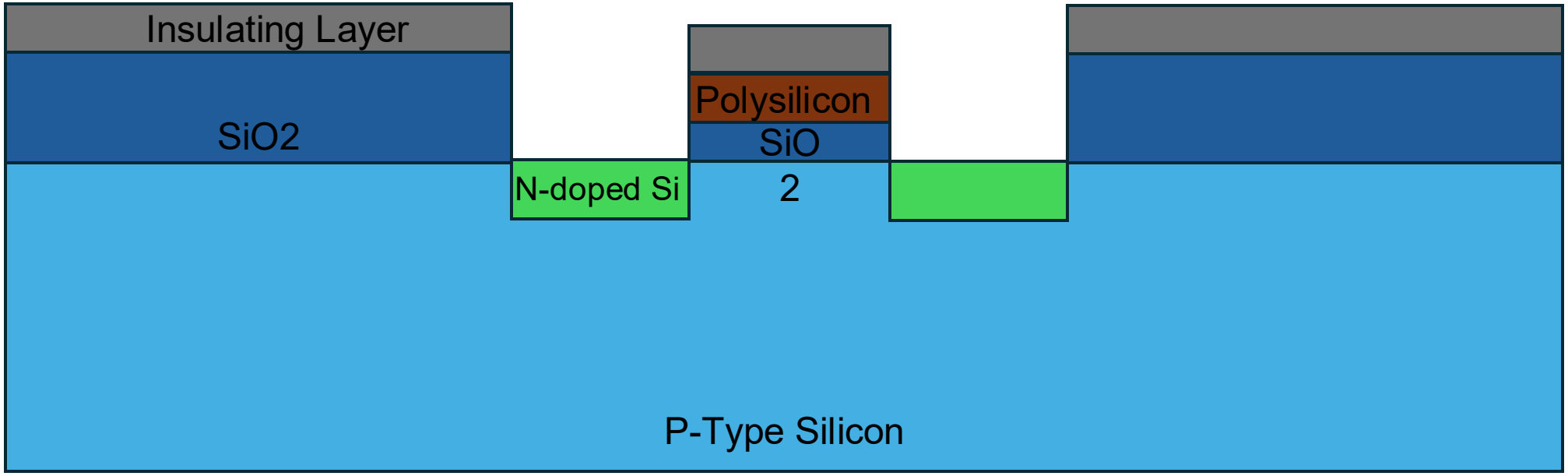
22) Developed, washed



23) Etched

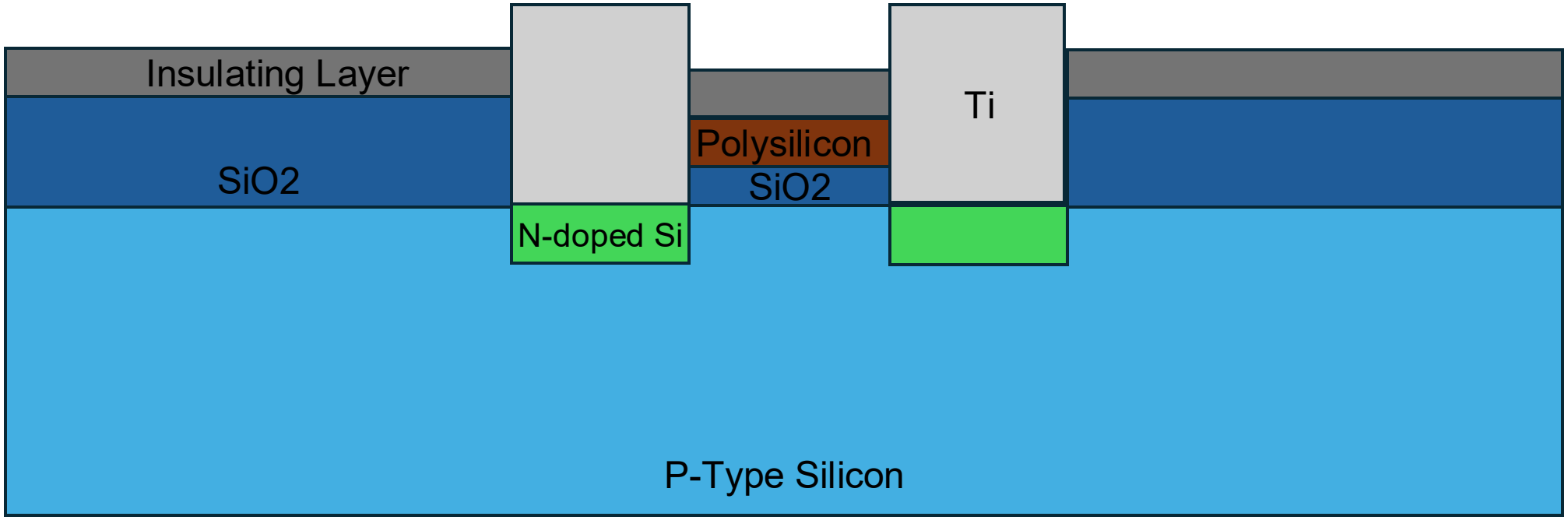

Photoresist
Insulating Layer
SiO2
N-doped Si
Polysilicon
SiO
2
P-Type Silicon

24) Photoresist Acidwashed

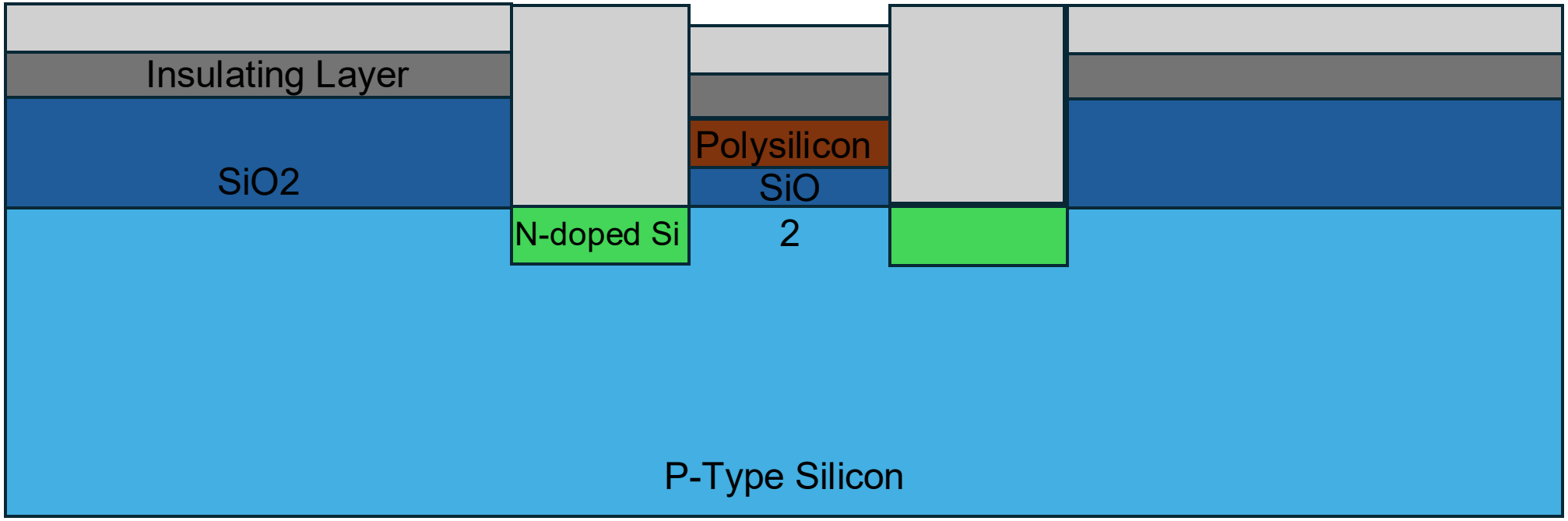


Metallization

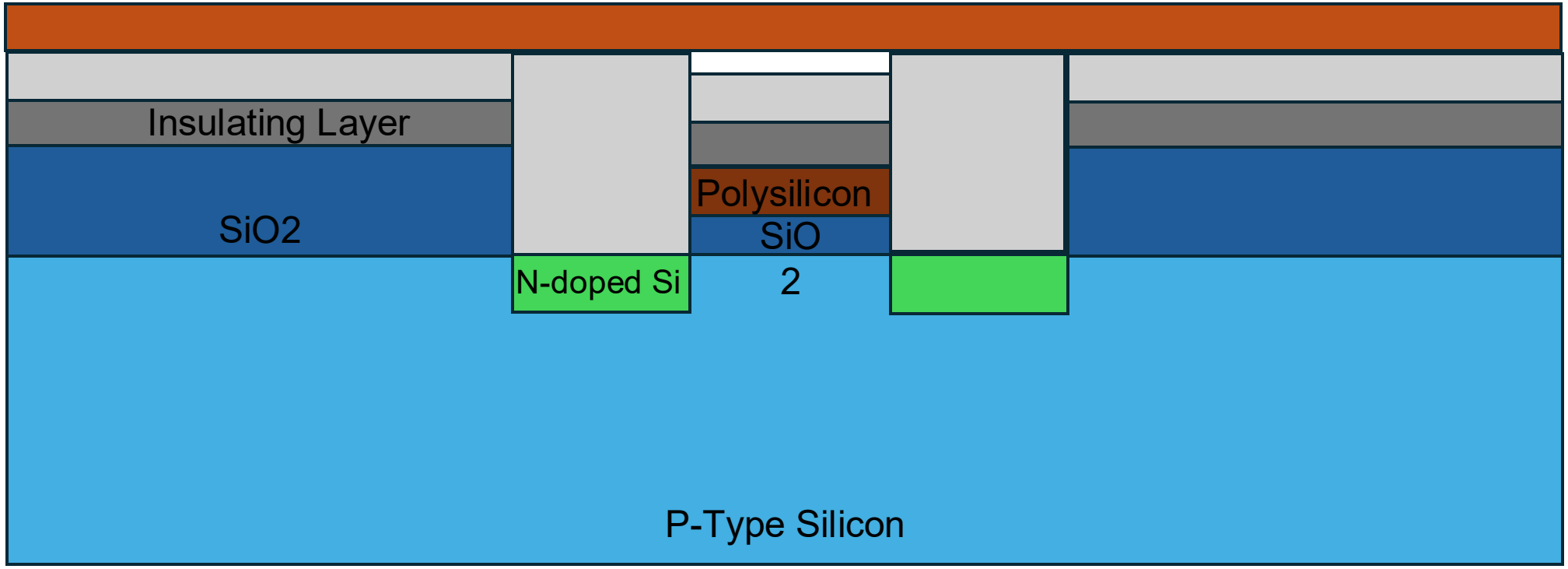
Goal:


Insulating Layer
SiO2
N-doped Si
Polysilicon
SiO2
Ti
P-Type Silicon

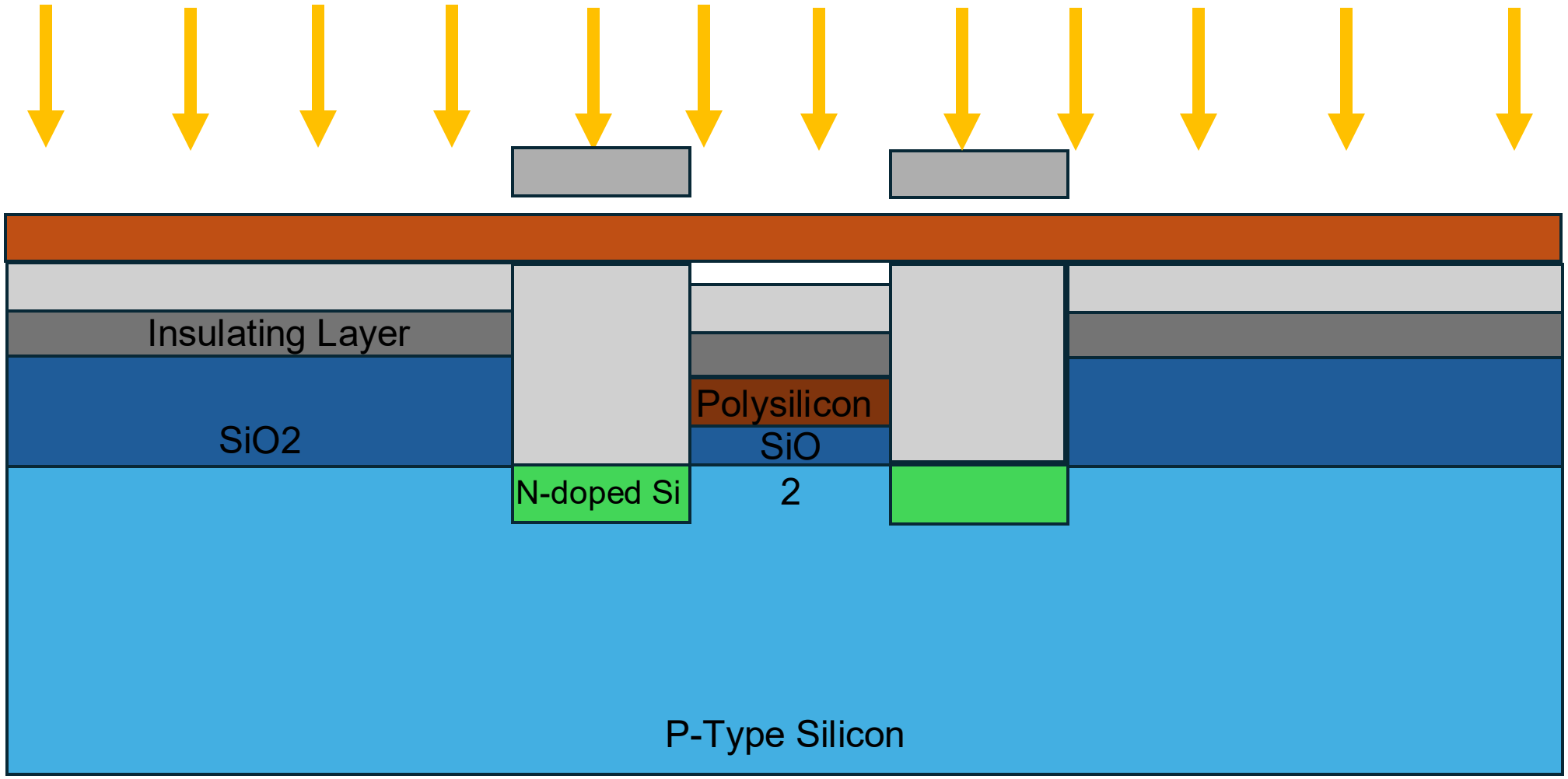
25) Metal (Ti) Deposited on surface



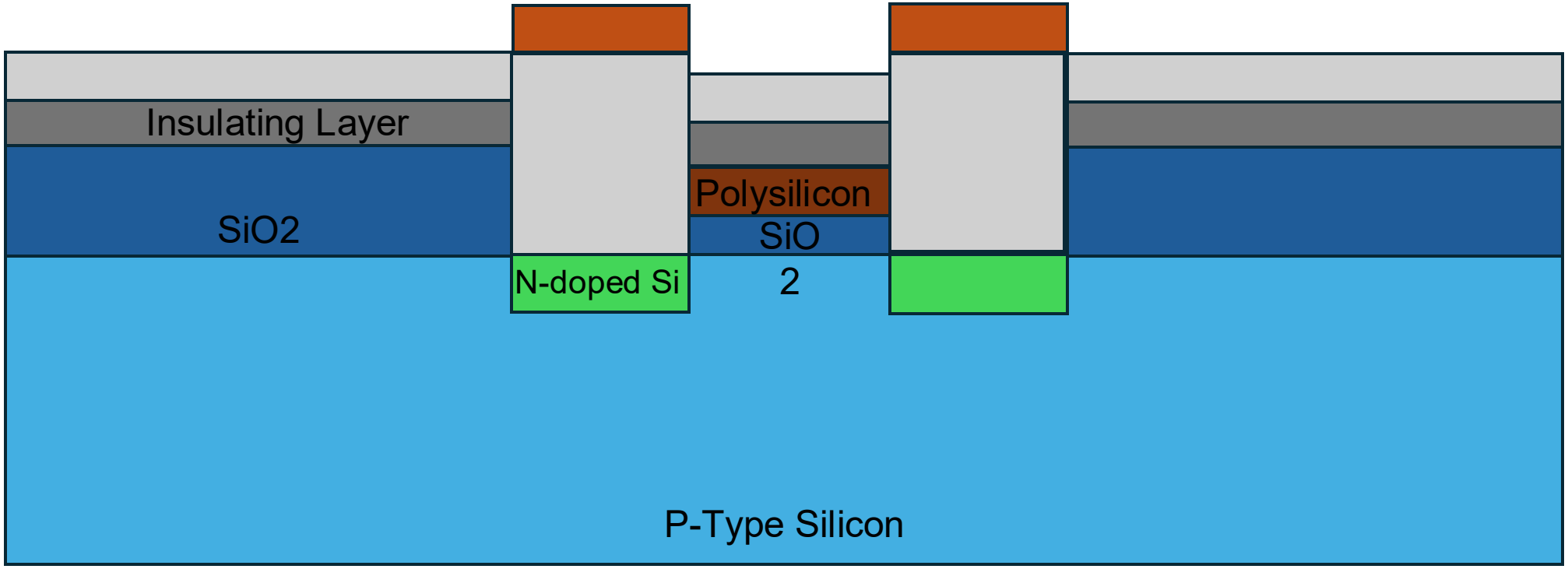
26) Resist spun on



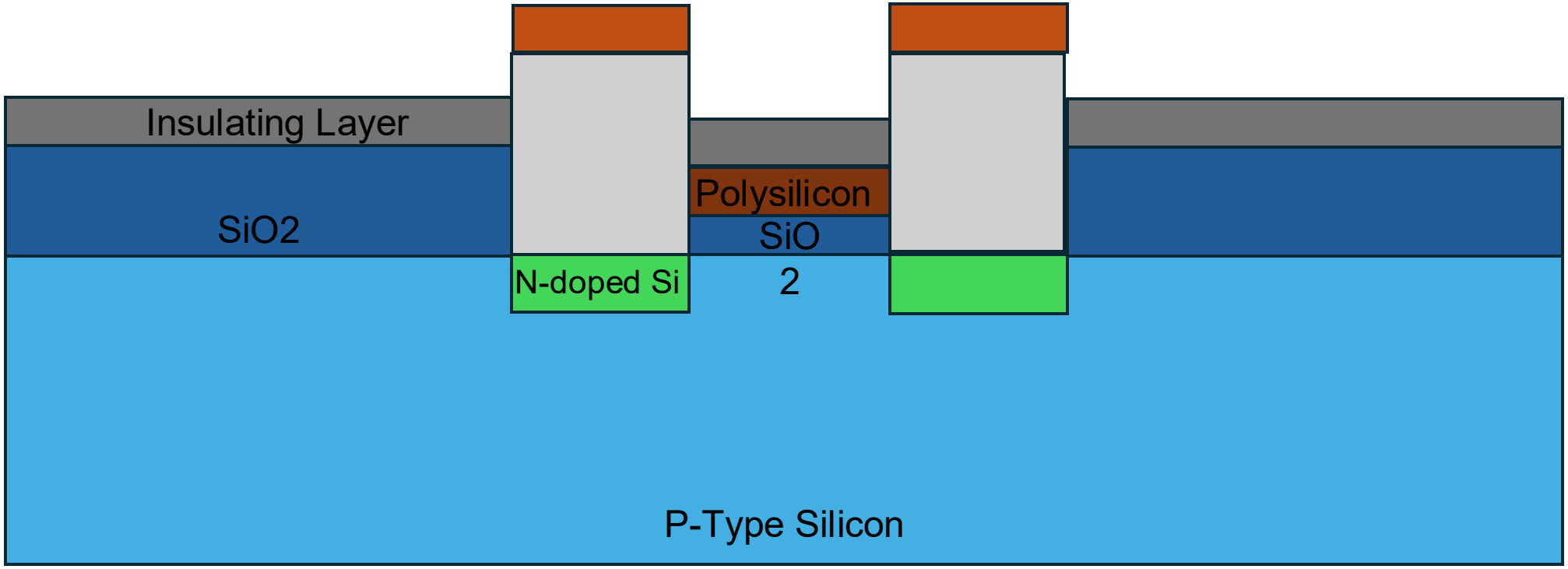
27) Resist exposed



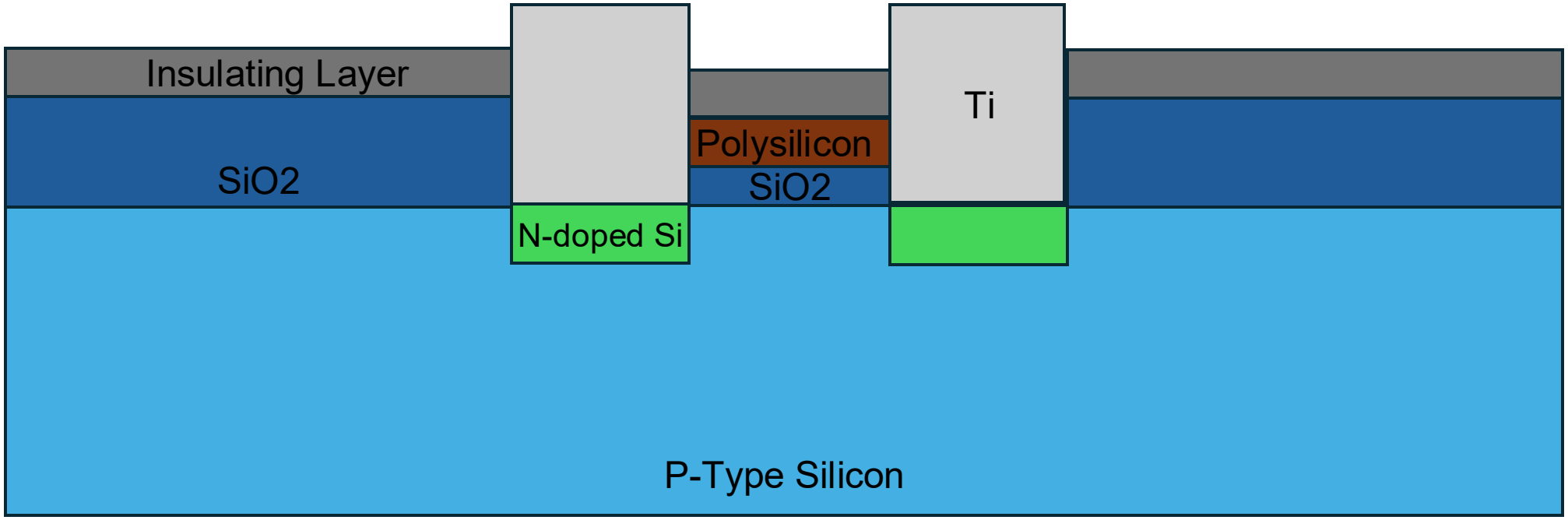
28) Resist developed, washed



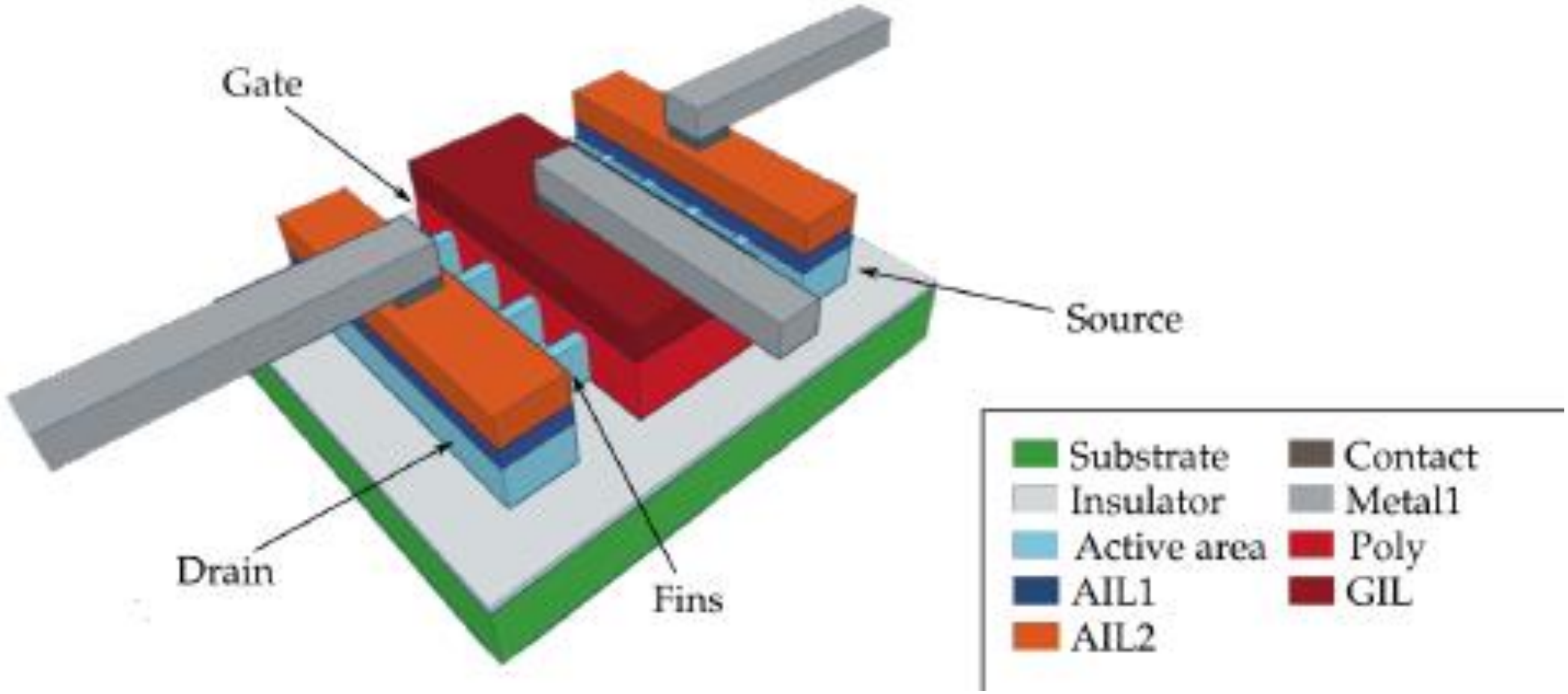
29) Ti etched away



30) Photoresist washed off, revealing “finished” MOSFET



How do we control the gate?

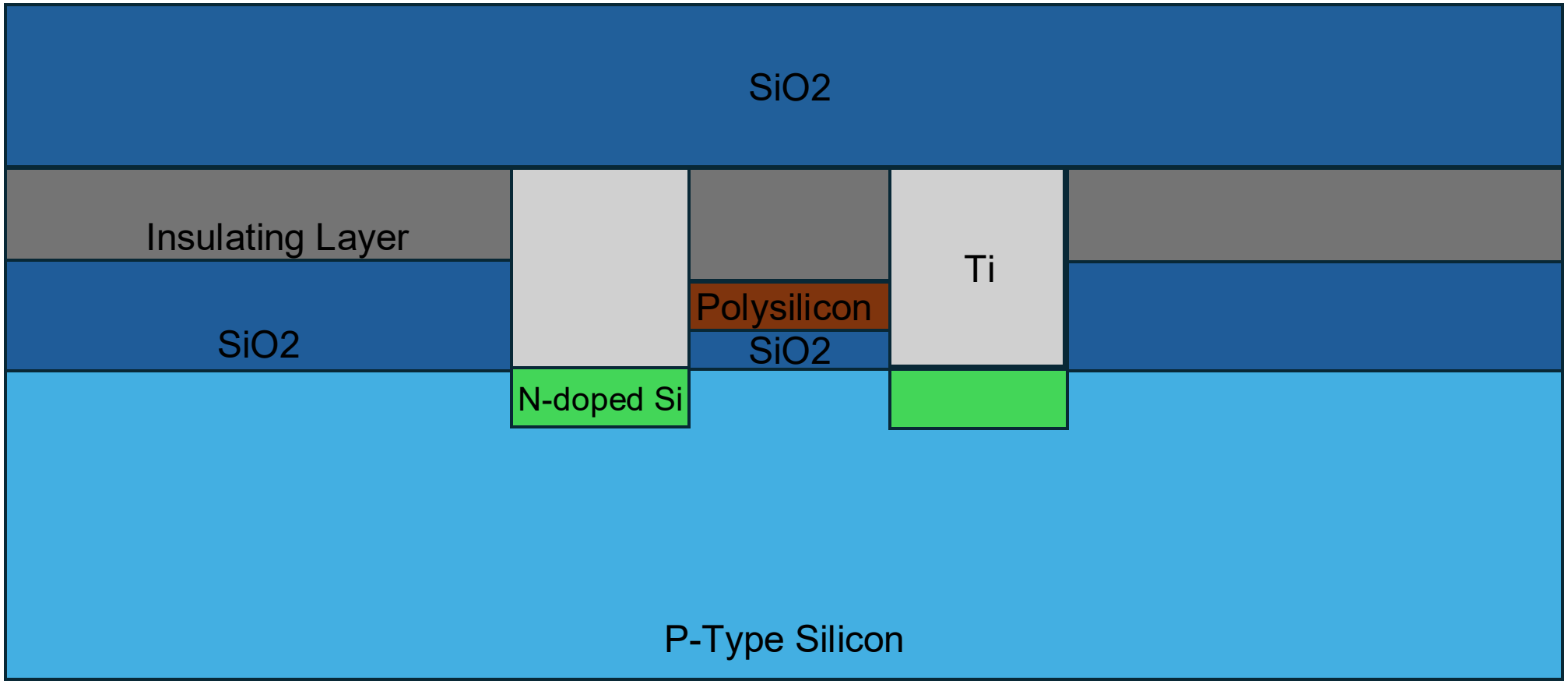


The end!

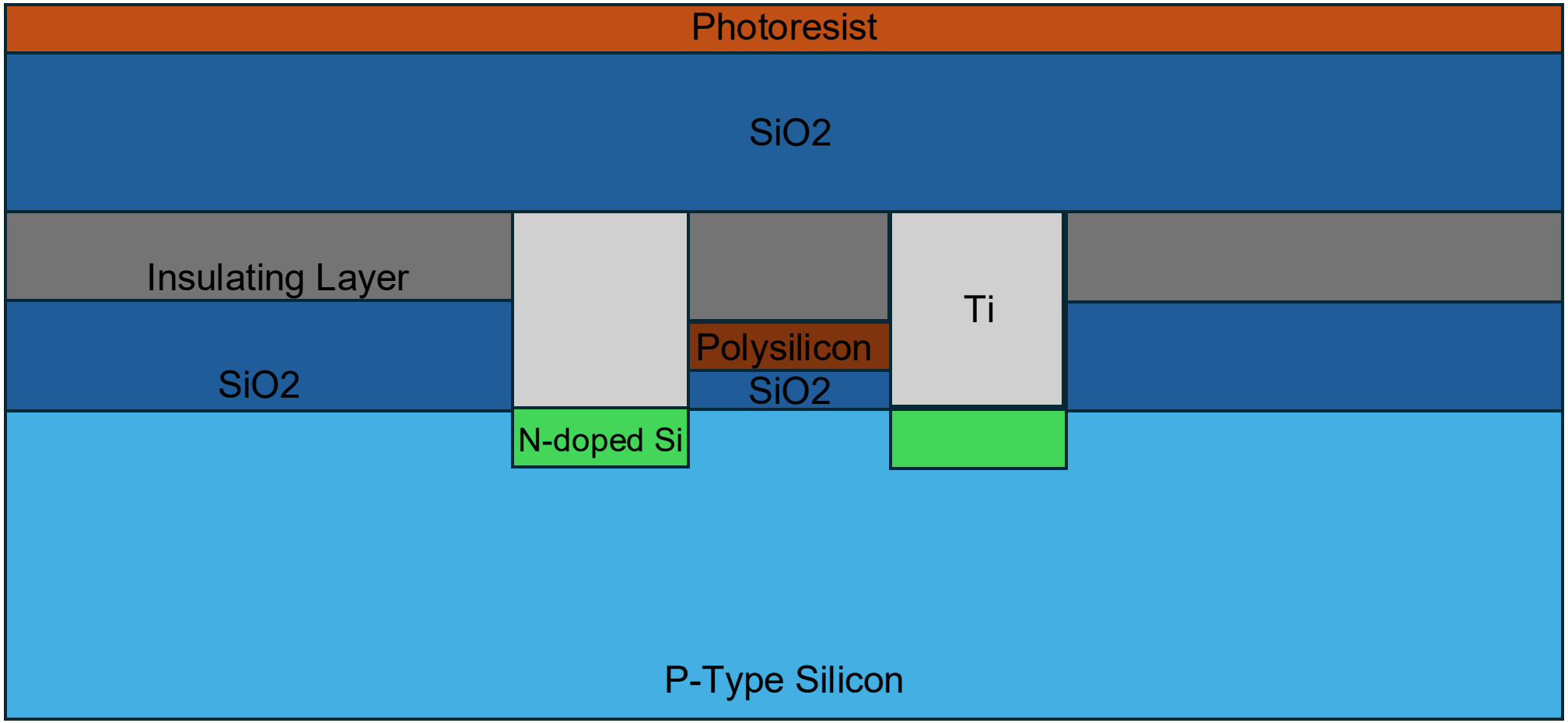
Unless…

Dual Damascene-The real metallization

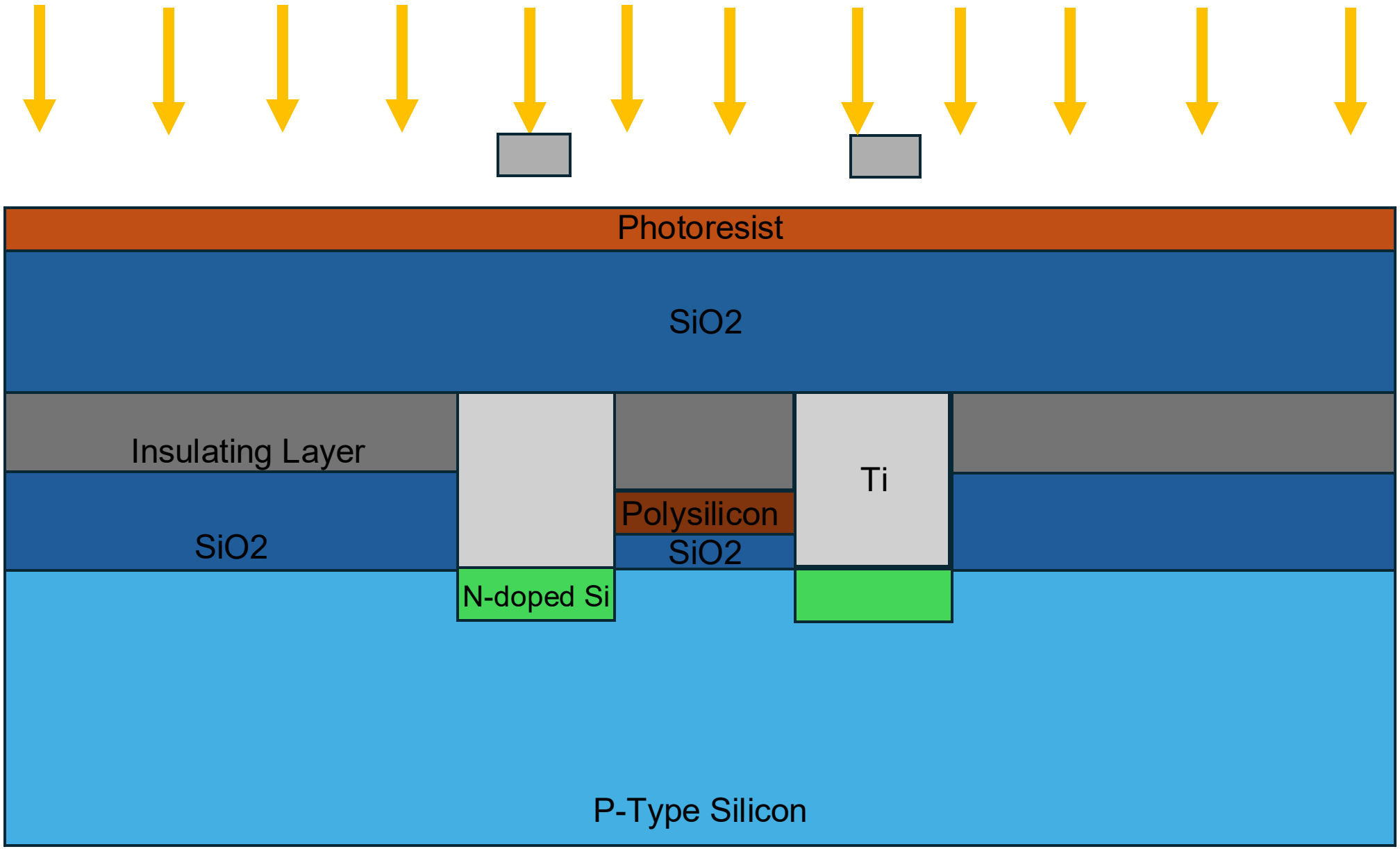
31) Grow Electrical Insulator (SiO2)



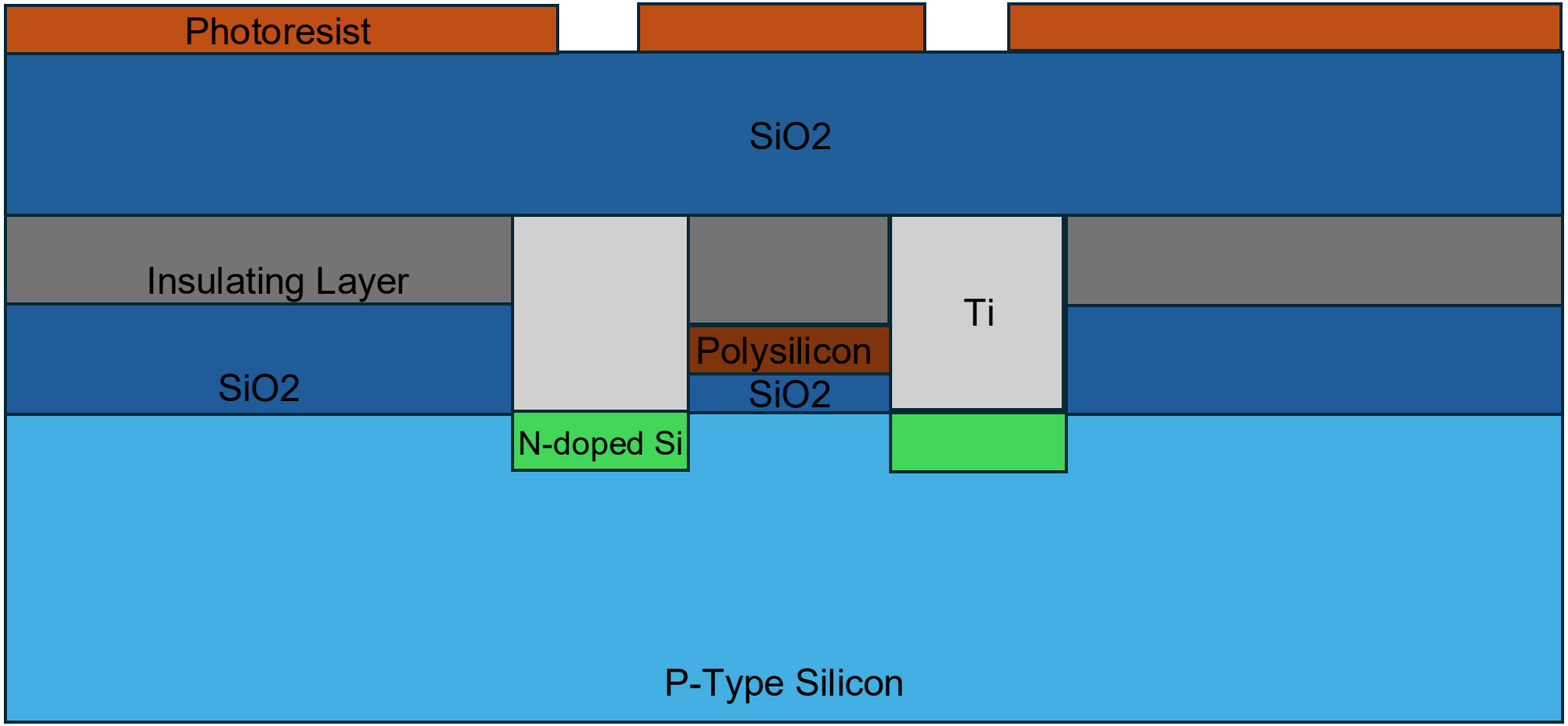
32) Spin on Photoresist



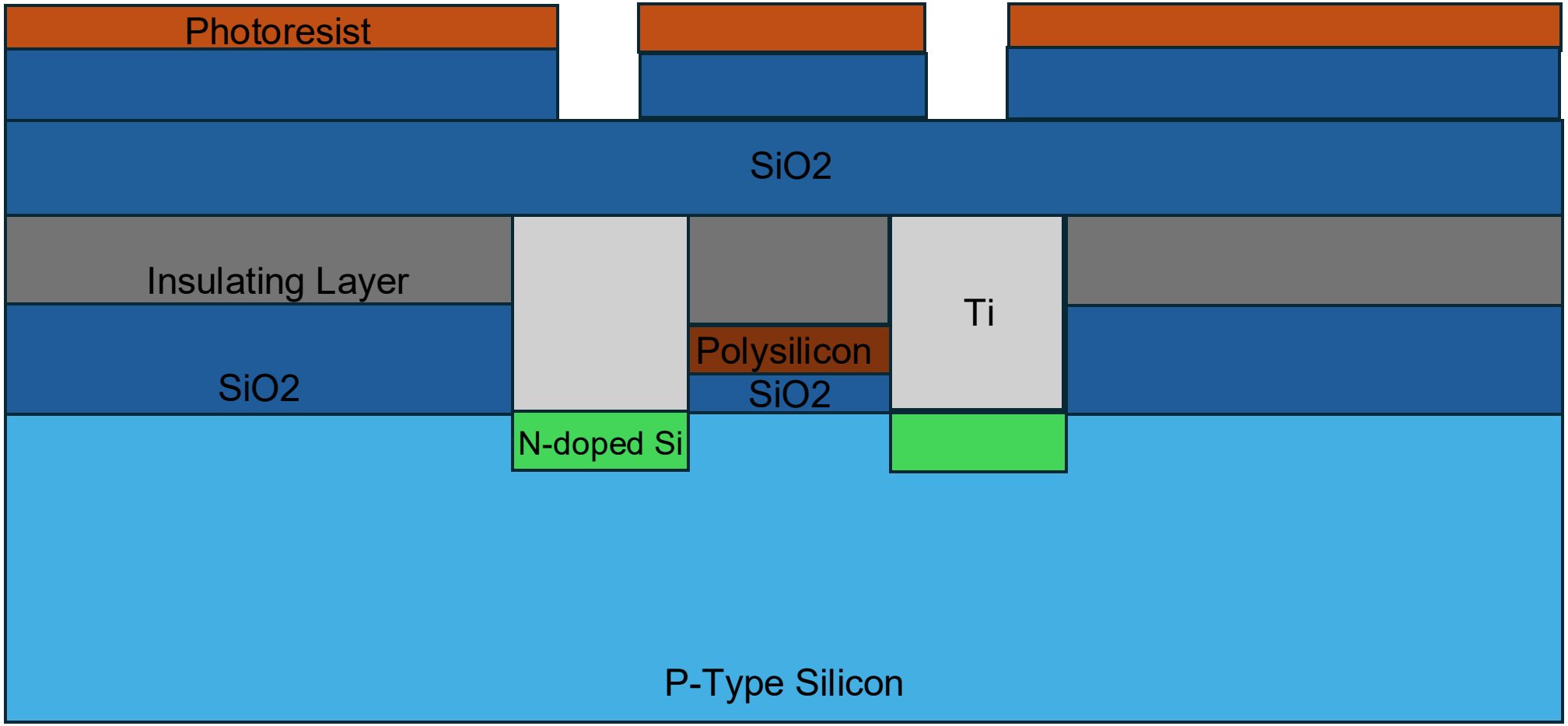
33) Pattern Vias



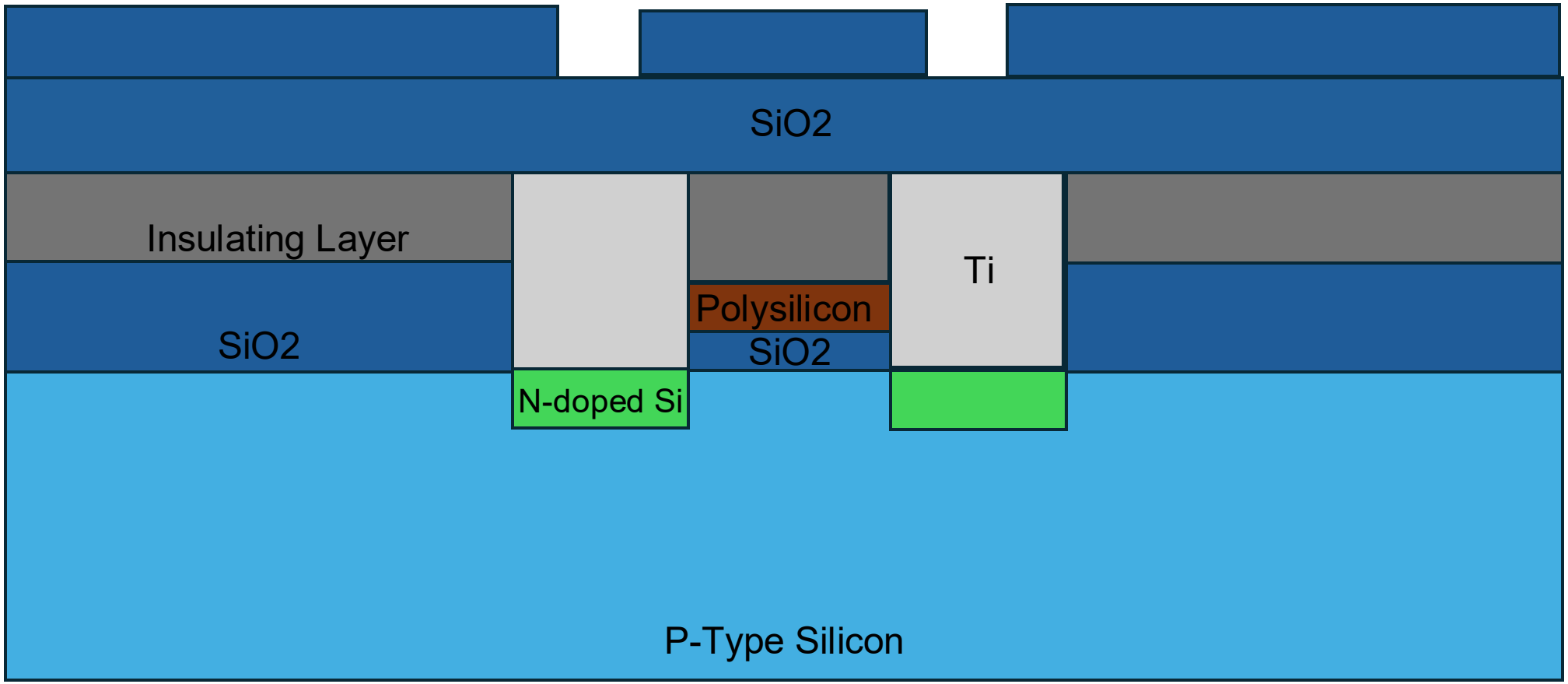
34) Develop Photoresist



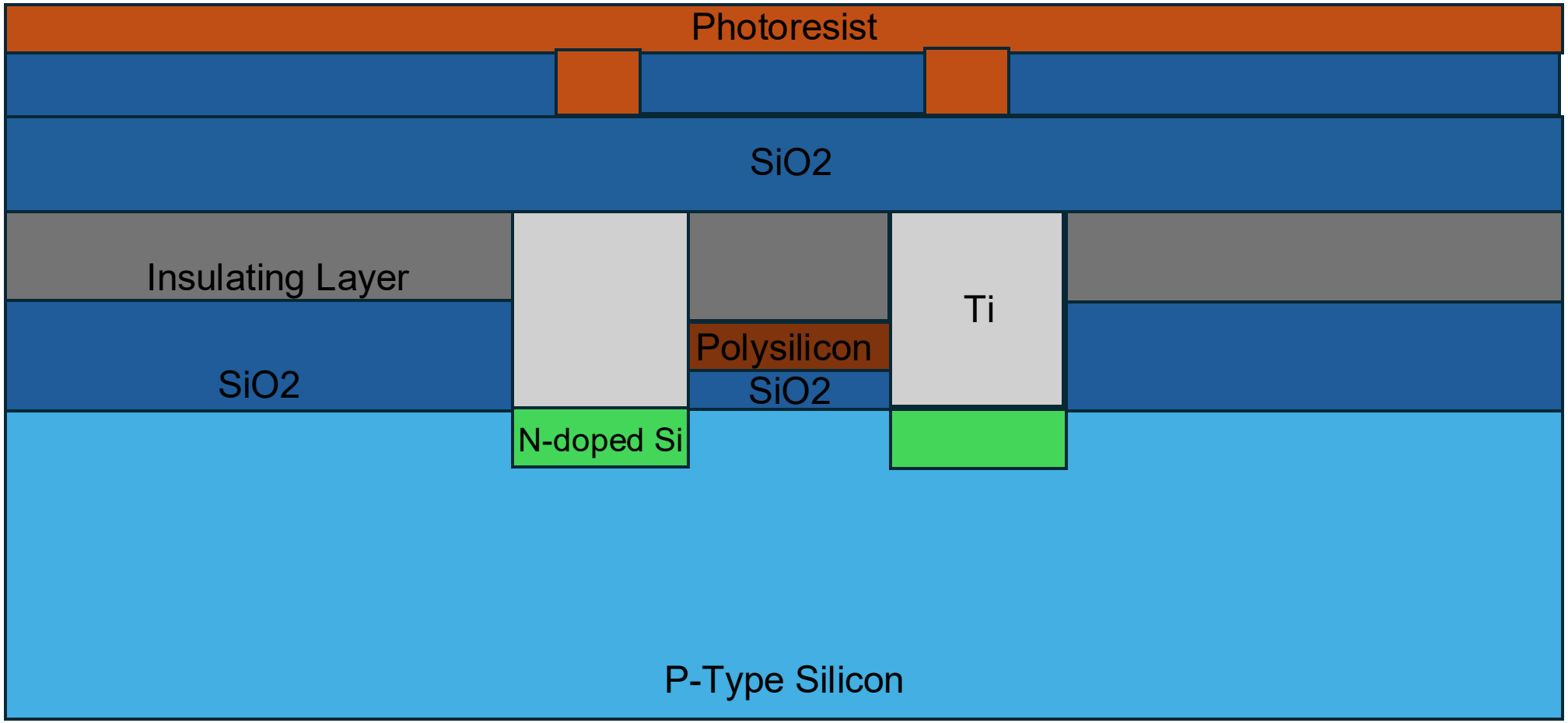
35) Anisotropic Etch of Vias



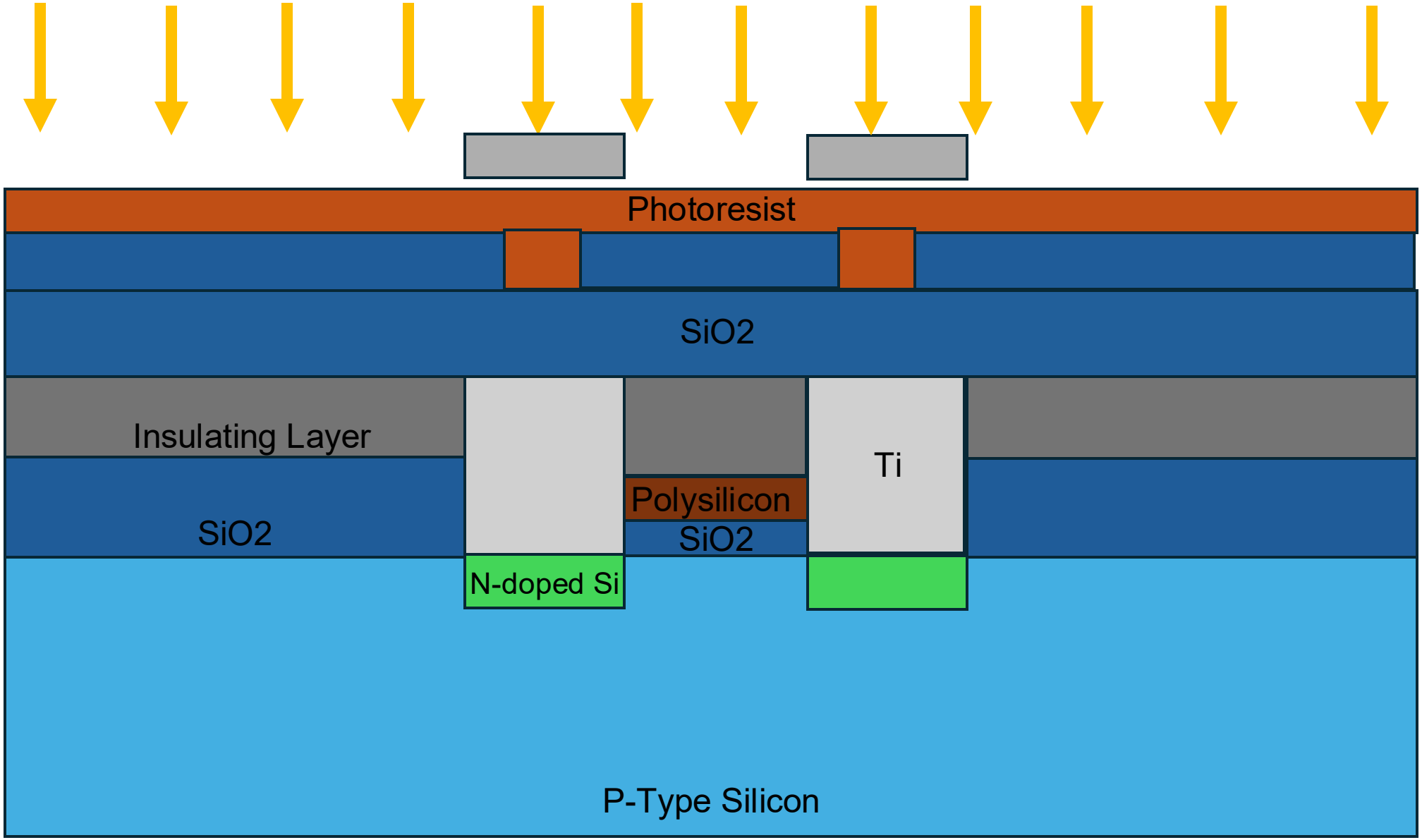
36) Remove Photoresist



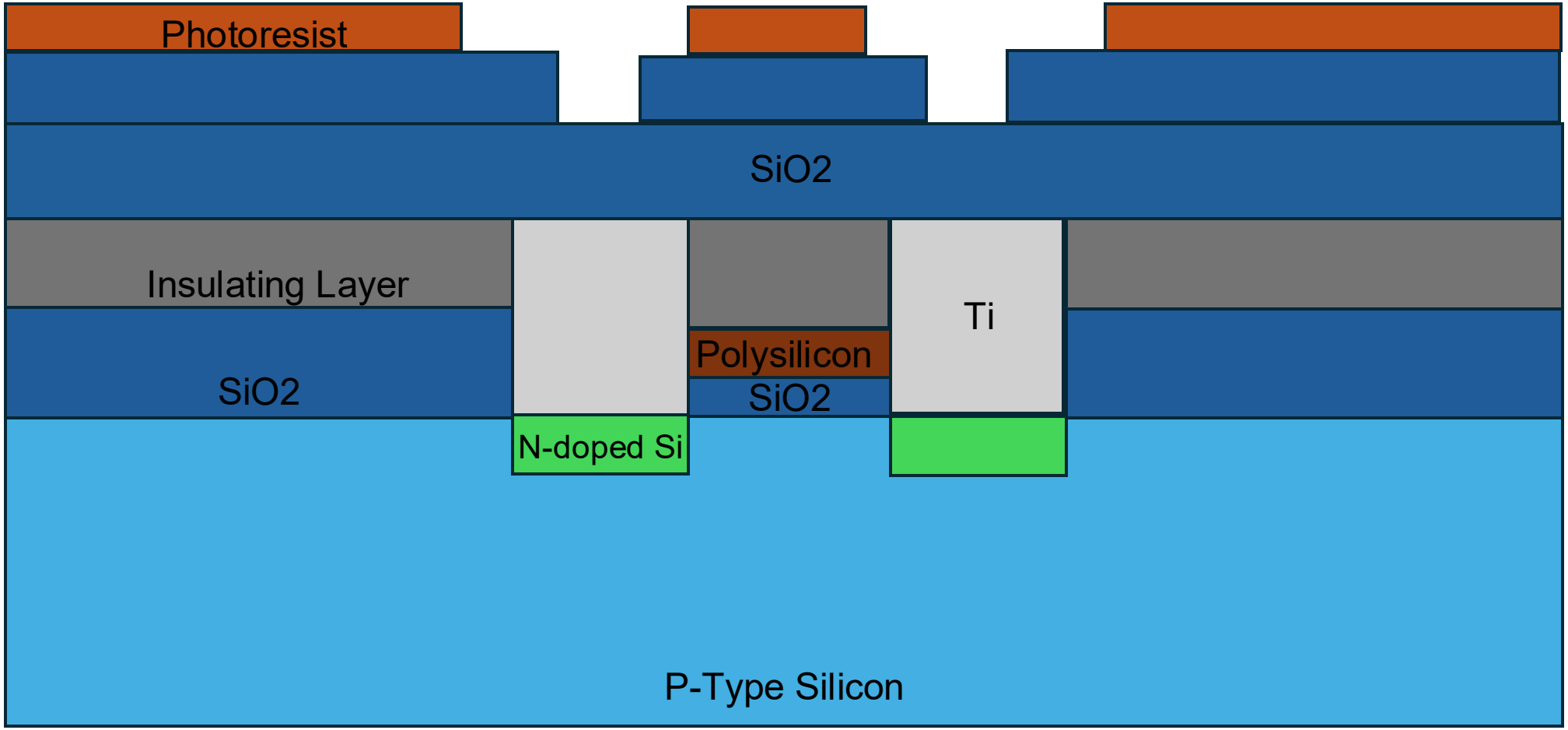
37) Put even more photoresist



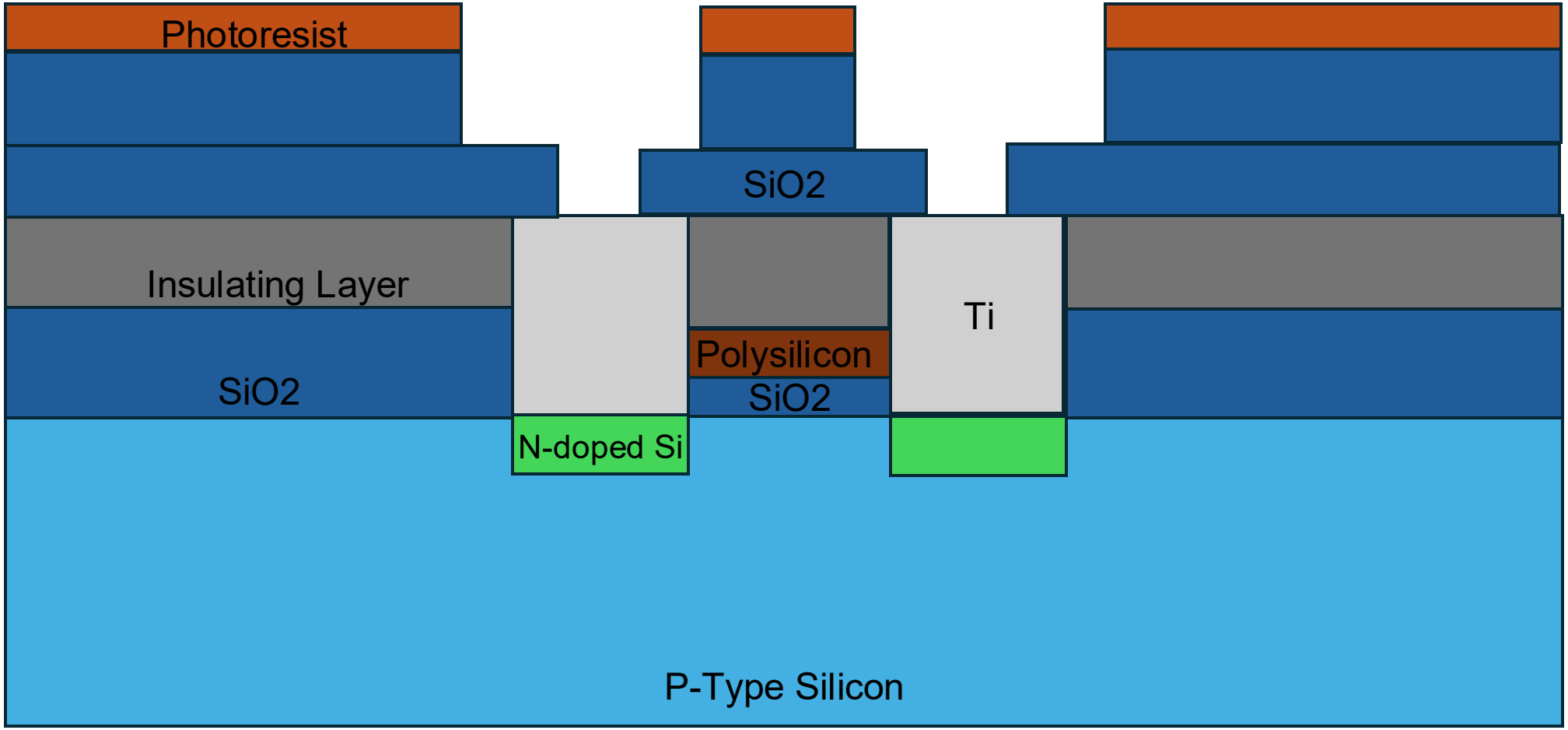
38) Pattern next metal layer



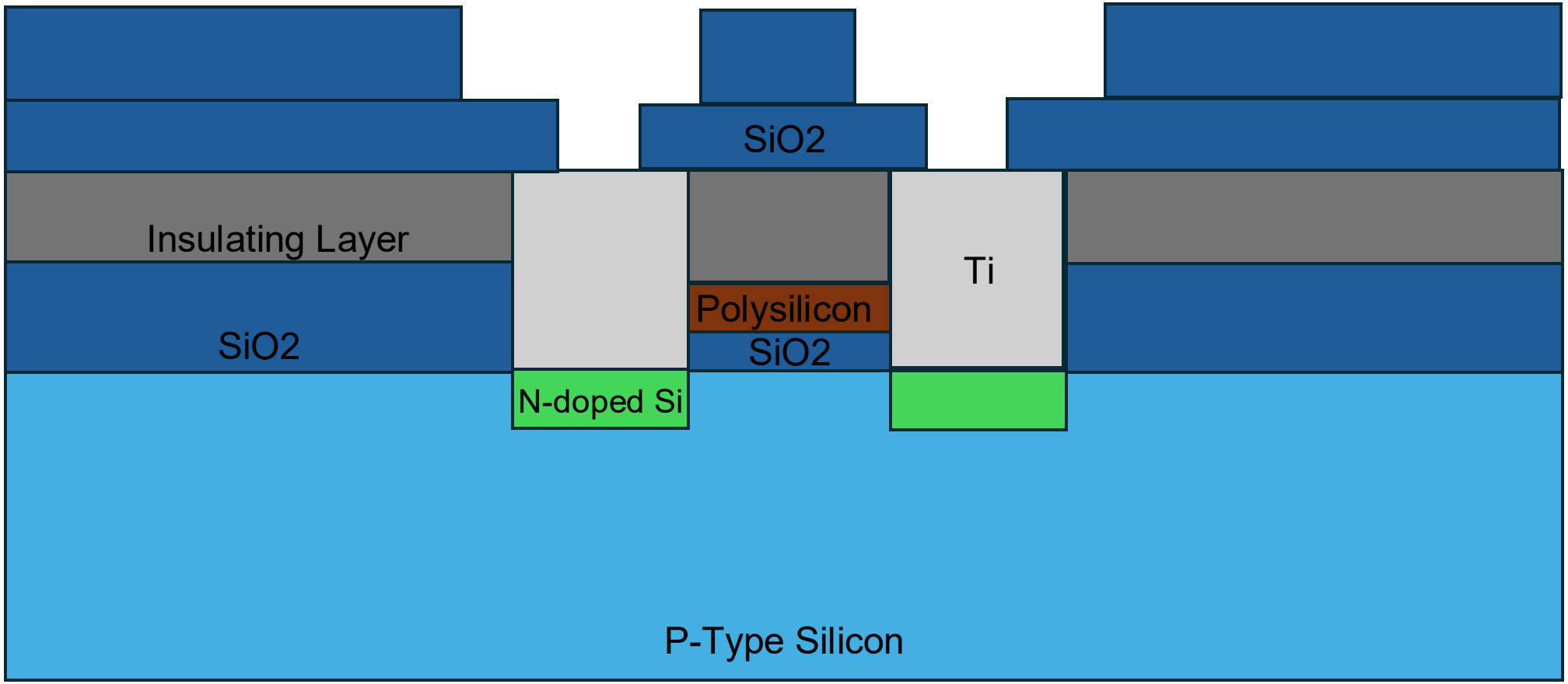
39) Pattern next metal layer



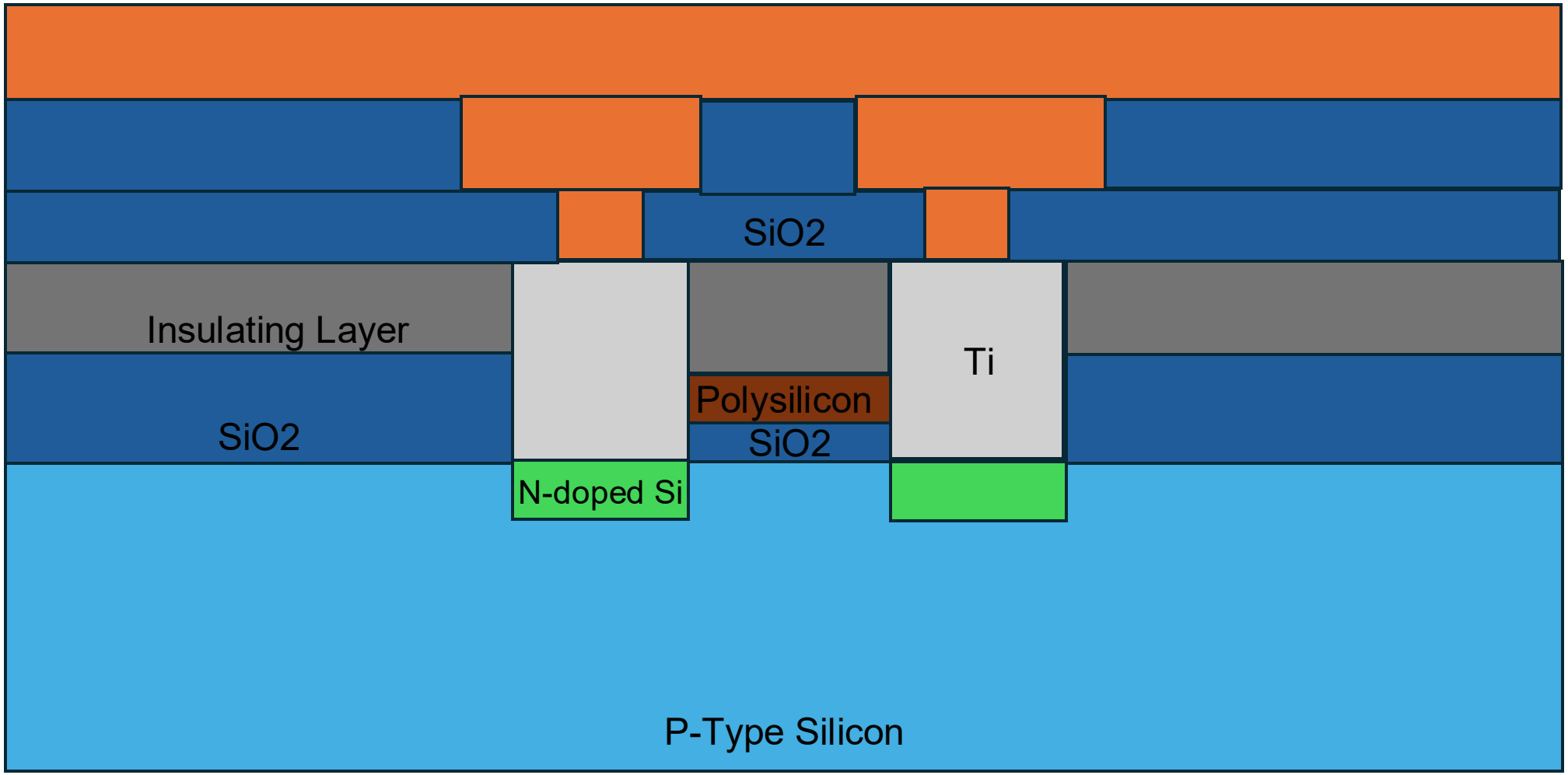
40) Etch metal layer/Via (again)



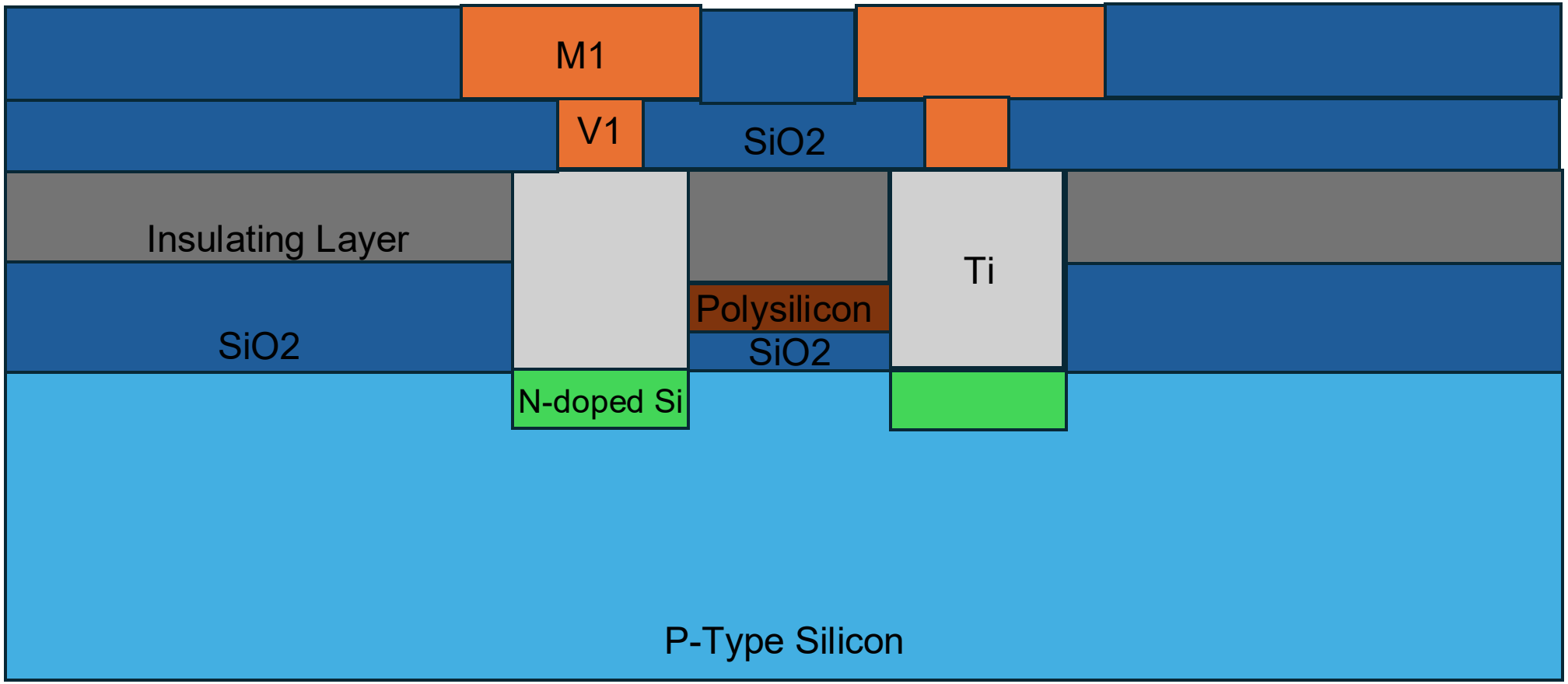
41) Remove Photoresist



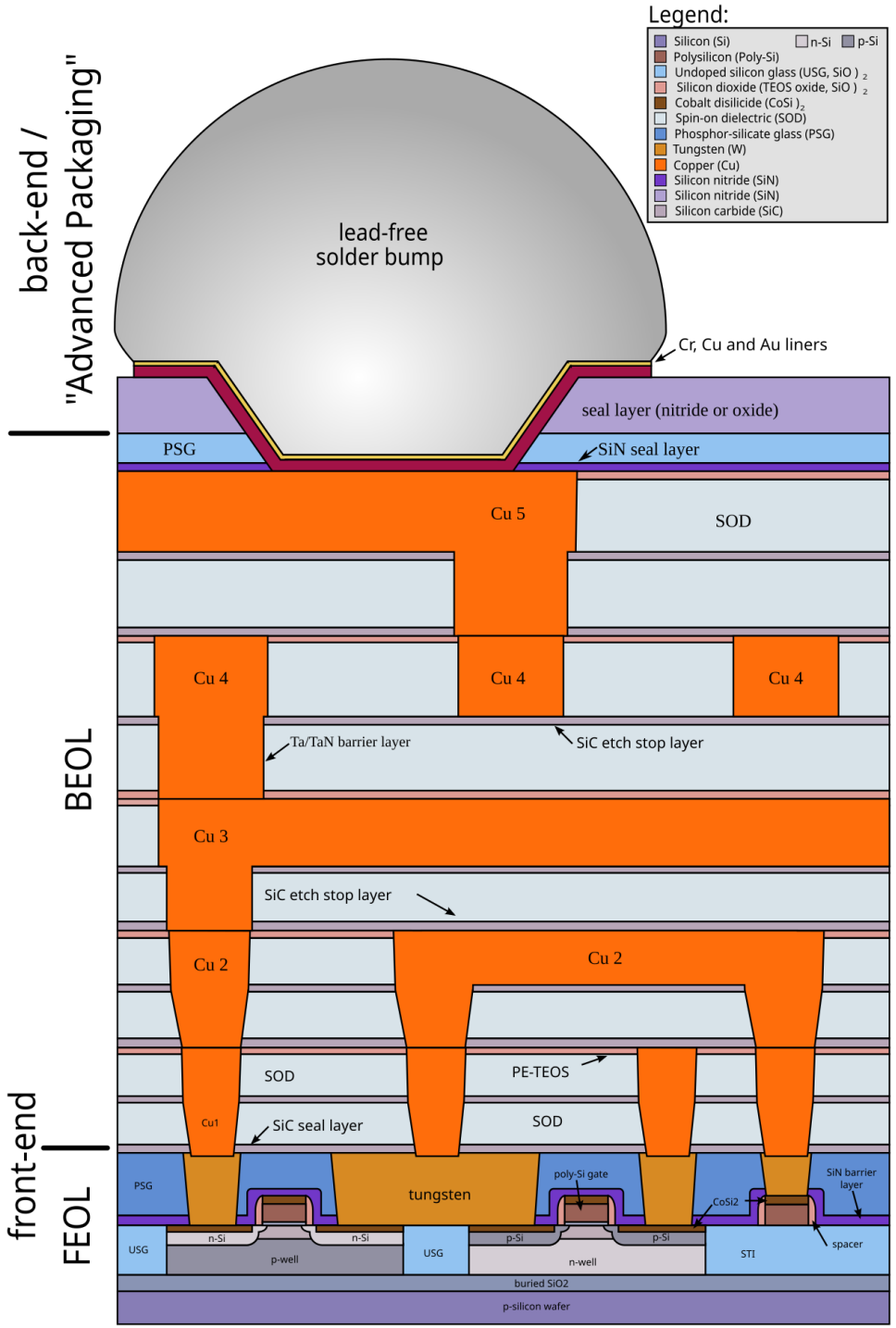
42) Electroplate with Copper



43) CMP to remove excess copper



$(\text{Repeat})^{15}$


Legend:
Silicon (Si)
n-Si
p-Si
Polysilicon (Poly-Si)
Undoped silicon glass (USG, SiO 2)
Silicon dioxide (TEOS oxide, SiO 2)
Cobalt disilicide (CoSi 2)
Spin-on dielectric (SOD)
Phosphor-silicate glass (PSG)
Tungsten (W)
Copper (Cu)
Silicon nitride (SiN)
Silicon nitride (SiN)
Silicon carbide (SiC)
back-end / "Advanced Packaging"
lead-free solder bump
Cr, Cu and Au liners
seal layer (nitride or oxide)
PSG
SiN seal layer
Cu 5
SOD
BEOL
Cu 4
Cu 4
Cu 4
Ta/TaN barrier layer
SiC etch stop layer
Cu 3
SiC etch stop layer
Cu 2
Cu 2
SOD
PE-TEOS
Cu1
SiC seal layer
SOD
front-end
FEOL
PSG
tungsten
poly-Si gate
CoSi2
SiN barrier layer
n-Si
n-Si
p-Si
p-Si
USG
p-well
USG
n-well
STI
spacer
buried SiO2
p-silicon wafer

Questions?

GBM Attendance