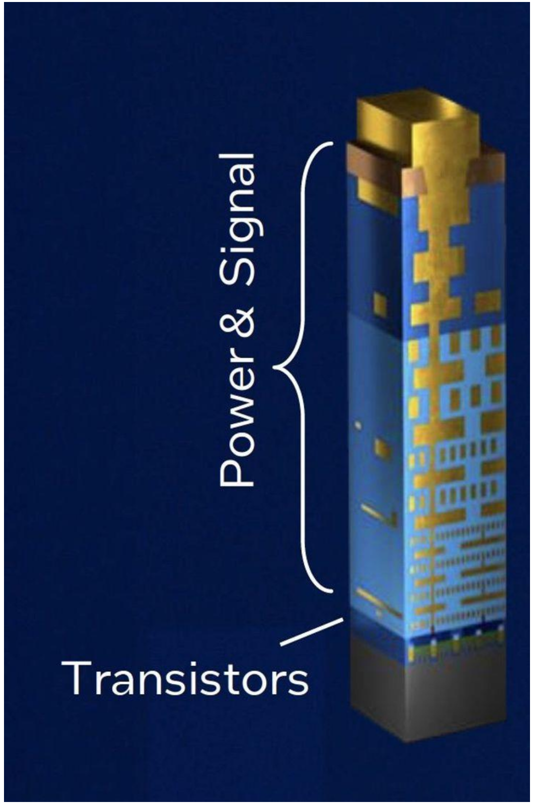
Backside Power Delivery Networks (BSPDN)

Jonas Kendra
IEEE/EPS | 17 Oct. 2024

Overview

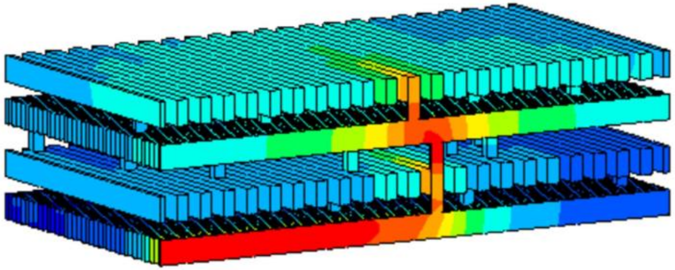
- Current problems
- Physics 101
- The Solution
- How do we do it?
- Challenges with the solution
- Overview

Overview: What is Back End of Line?



Current Problems

- Back end of Line (BEOL) processing involves complex, expensive patterning techniques that traverse 15+ layers
- Layers must provide power and communication from the transistor layer to motherboard layer
- Communication lines and power lines intermingle, causing interference
- Resistance in power lines is growing more and more difficult to manage, resulting in parasitic power losses



Current Problems

Transistors, wasting time trying to figure out what’s they were just told to do

Current Problems

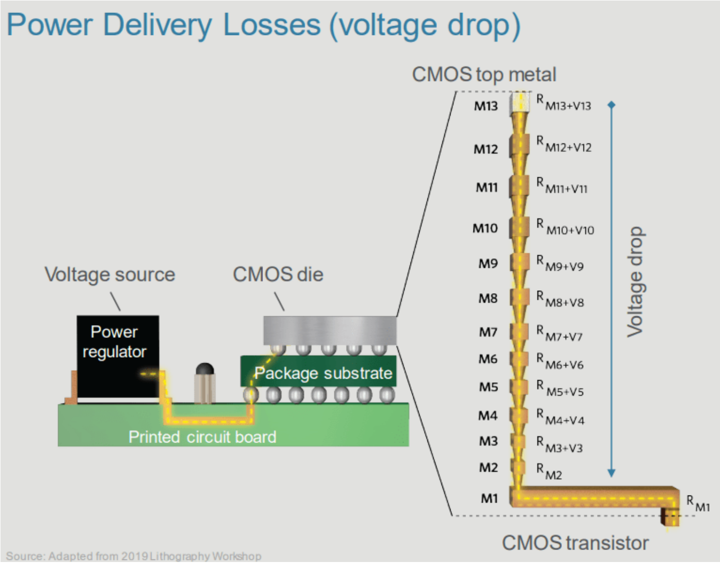
Thermal engineers dealing with yet another source of heat in the chips

Current Problems

Fabs, if they didn't have to build expensive BEOL

Physics 101: Resistivity

- Resistivity is a material property, and cannot be readily changed
- What can we do to reduce resistance in a wire?
- Which layer would lead to largest resistance?
- So… what can we do to reduce resistance in BEOL?



$$R = \frac{\rho L}{A}$$

ρ = resistivity
L = length
A = cross sectional area

Physics 101: Heat Generation

- Power losses lead to heat generation...
- High resistance in BEOL means more heat generation in addition to heat from the transistor

Ohm's Law

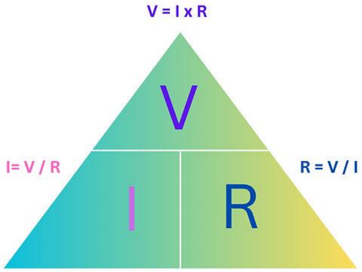
$E = IR$ $\quad I = \frac{E}{R}$ $\quad R = \frac{E}{I}$

Joule's Law

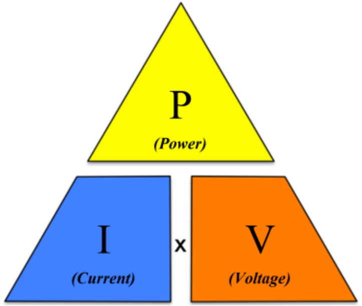
$P = IE$ $\quad P = \frac{E^2}{R}$ $\quad P = I^2R$

Where,

E = Voltage in volts
I = Current in amperes (amps)
R = Resistance in ohms
P = Power in watts



Ohm's Law Triangle
The relationship between voltage (V), current (I), and resistance (R)



The Power Triangle

(I promise we aren't the illuminati)

POP QUIZ

- ρ = 1 ohm*meter, V= 1 Volt (Given) L=1 meter
- A=0.01m^2 OR 0.02m^2

- How much heat is generated by each power line (in watts)

Ohm's Law

$E = IR \qquad I = \frac{E}{R} \qquad R = \frac{E}{I}$

Joule's Law

$P = IE \qquad P = \frac{E^2}{R} \qquad P = I^2R$

Where,

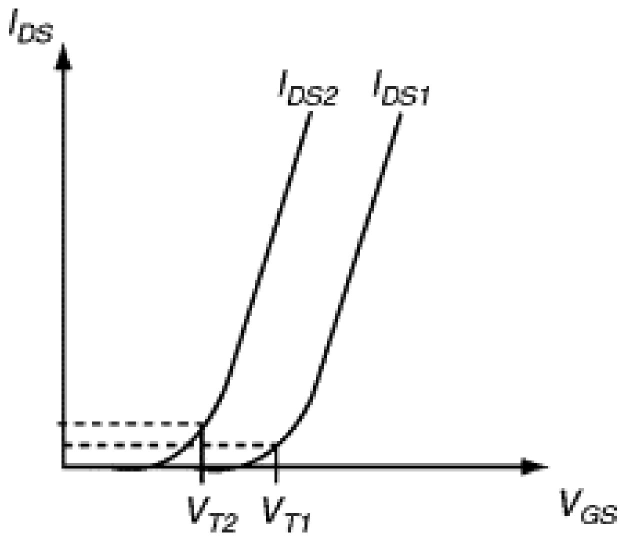
E = Voltage in volts
I = Current in amperes (amps)
R = Resistance in ohms
P = Power in watts

$$R = \frac{\rho L}{A}$$

ρ = resistivity
L = length
A = cross sectional area

Physics 101: Voltage=stability

- Each transistor may have a slightly different threshold voltage, depending on defectivity, geometry, etc.
- Clock speeds are limited by the slowest/worst transistor. Clock speeds can be improved slightly through overclocking (Artificially raising a device's internal clock speed). Due to the "weaker" transistors, this may cause stability, in which higher gate voltages can be applied
- However, higher device temperatures can reduce clock speeds. This is why you may have heard of "undervolting"
- Balance is needed between increasing voltage and increasing clock speed
- Simply, we want all of our input voltage to reach the gate, where it will do the most good for device performance- minimize other sources of losses

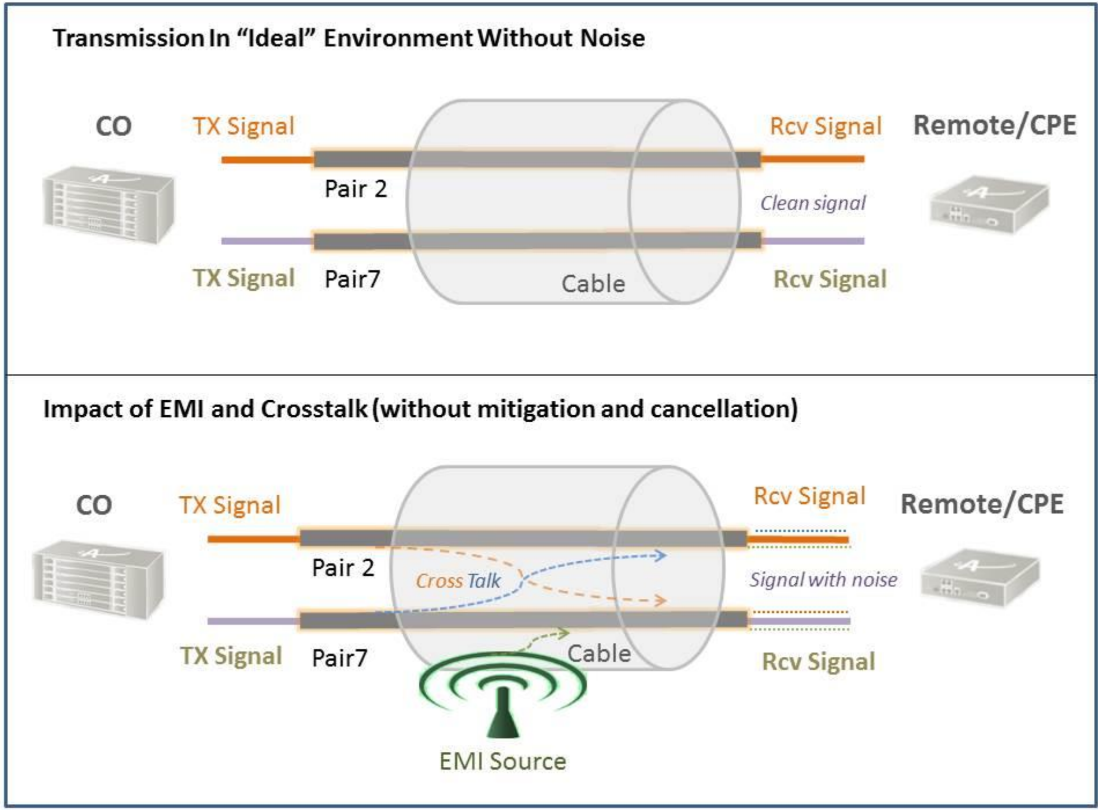


Physics 101: Crosstalk

RC Delay is increasingly important in lines as they get thinner and closer to one another

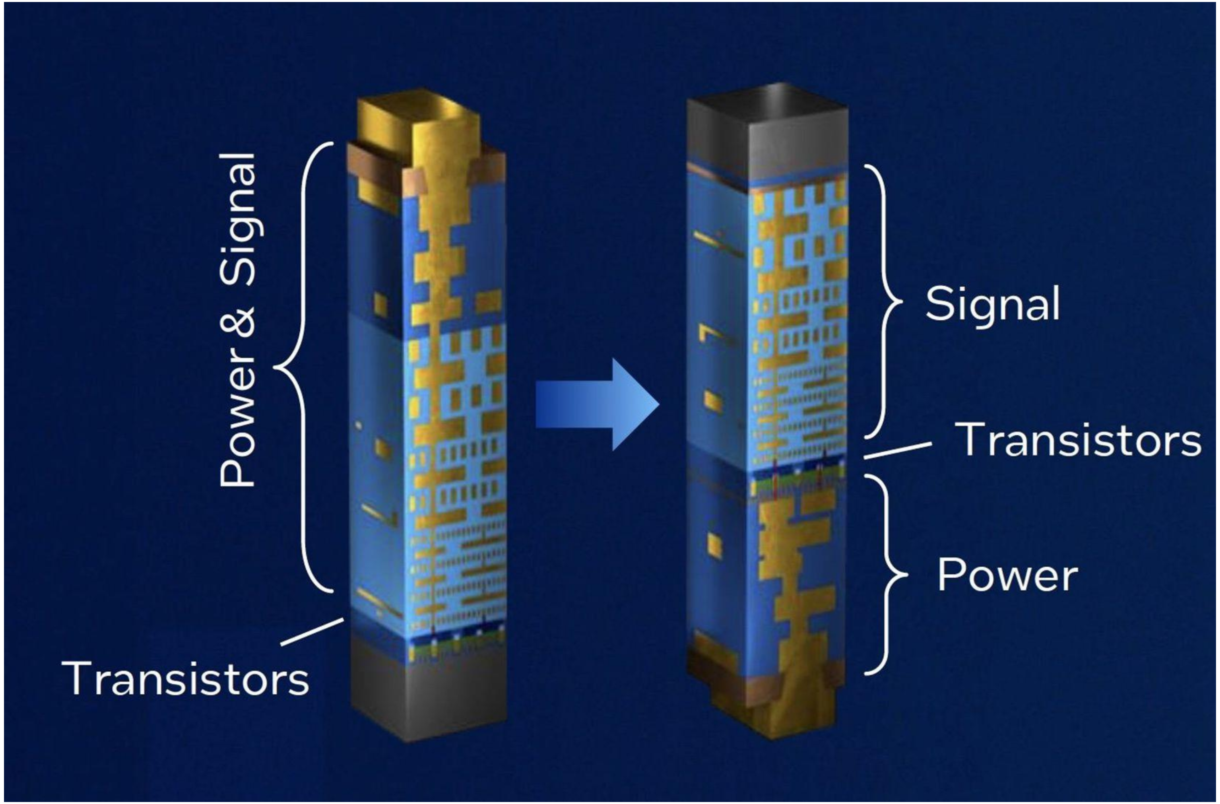
"The RC delay issues started a few nodes ago, and the problems are becoming worse. For example, a delay of more than 30% is expected when moving from the 10nm to the 7nm node."

-Zsolst Tokei, IMEC nano-interconnect program director

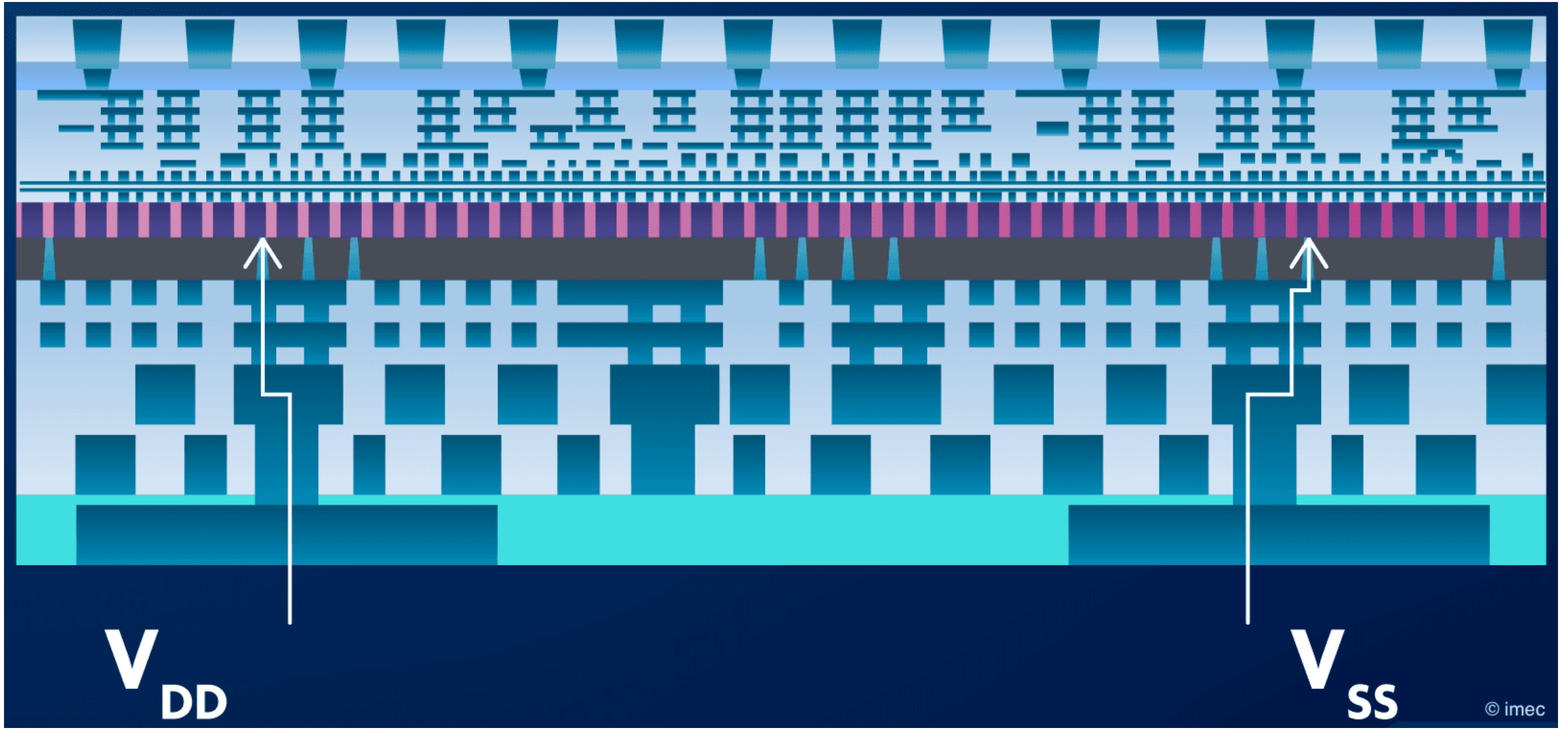


The Solution: BSPDN

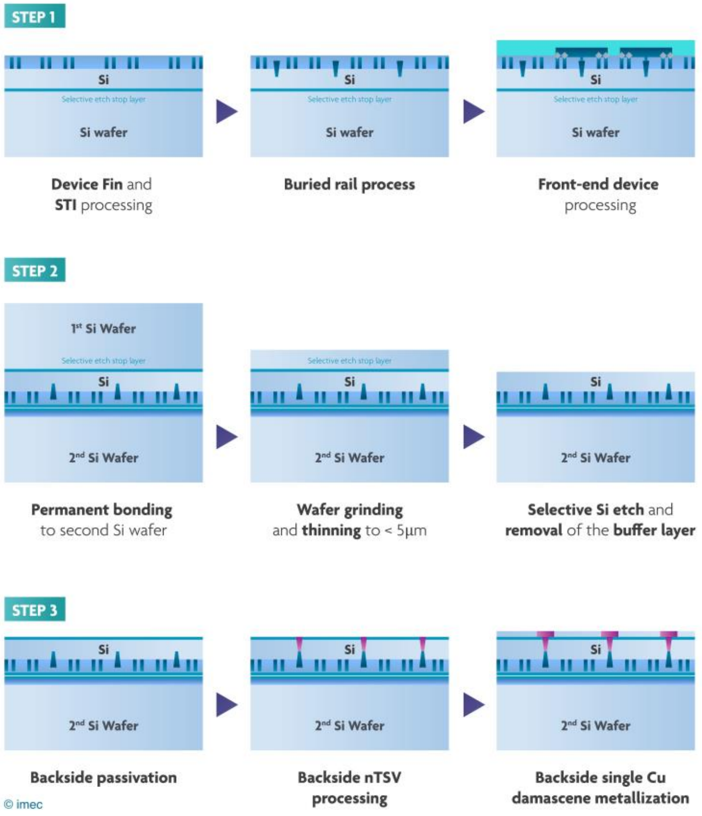
- Separate communication from power
- Decrease number of power metallization layers
- Increase spacing in signal lines, reducing interference
- Increase size of power lines, reducing resistive losses



How do we do it? (We lie?)

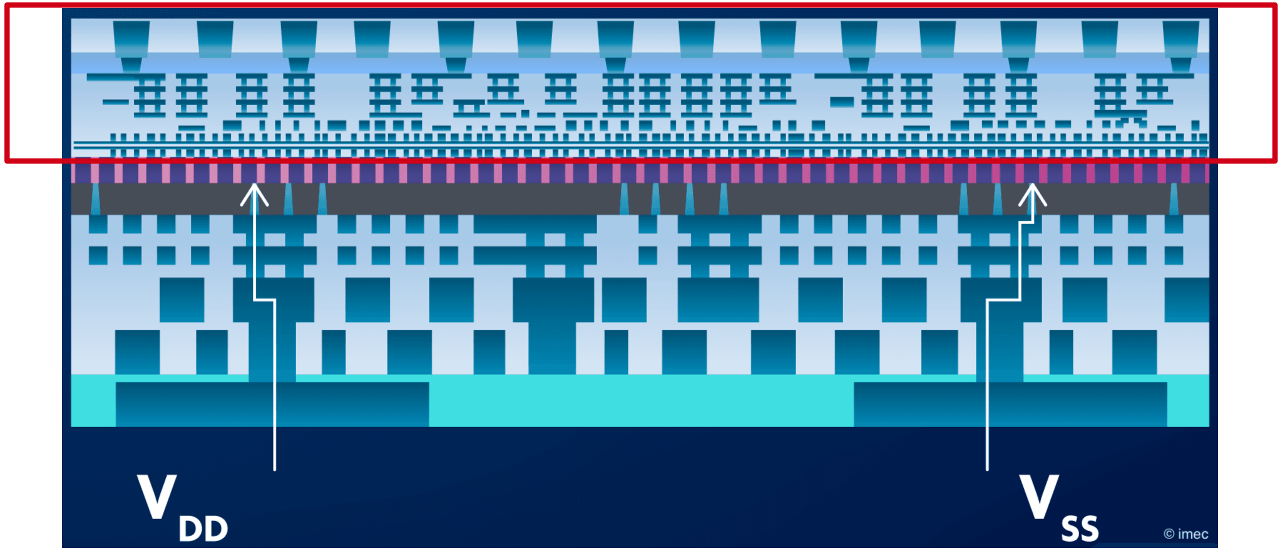


How do we do it- Wafer Processing



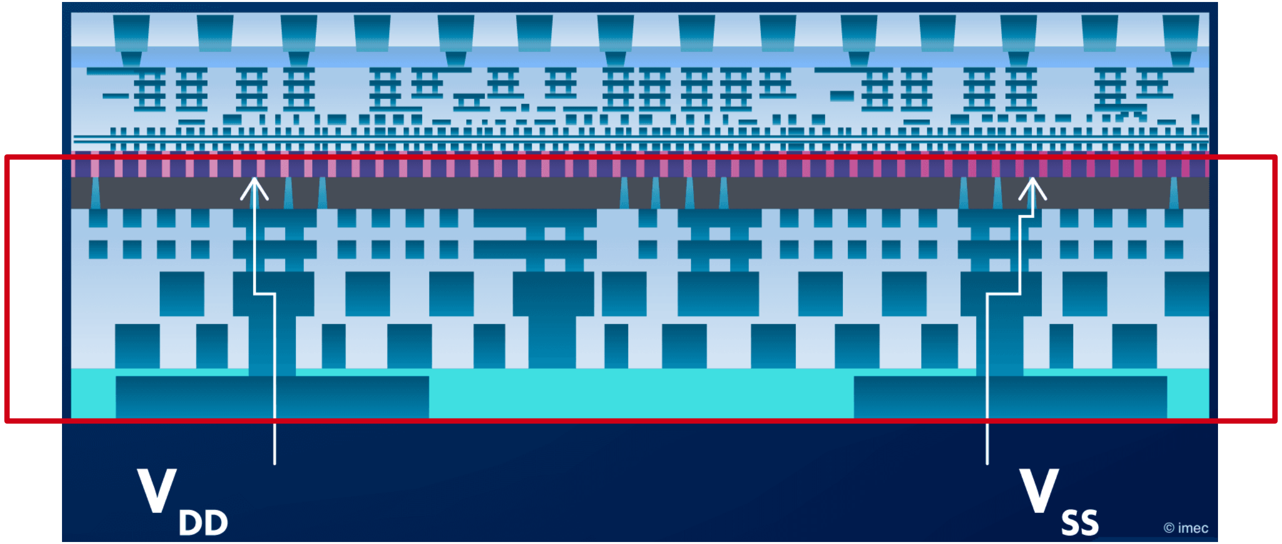
How do we do it- Wafer Processing

- All wafer processing in the top half is identical to current processing techniques (Just less metal in “BEOL”)
- When finished, grind away all silicon up until active region
- (Seen here, process from bottom up)



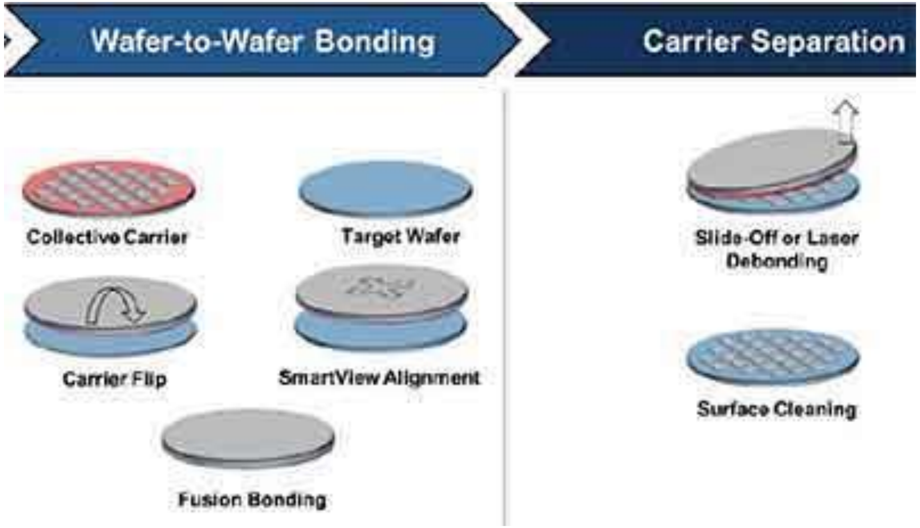
How do we do it- Wafer Processing

- Secondary wafer is prepared, and bonded to the first, with cutouts made for nTSV's (nano Through silicon vias)
- Copper power (and signal) lines are created on the secondary wafer as needed (Seen here, process at top down)



Challenges…

- Wafer bonding yield is still relatively poor, particularly near edges of wafer
- Reduction in yield offsets price savings from metallization layers
- Heavy R&D focus in wafer bonding yield to facilitate this new procedure. Whoever figures it out first wins $$$



Challenges…

- It is not well understood how introduction of secondary BEOL will influence thermal performance. Metallization layers and interconnects between FEOL and cooling solution seem problematic
- Intel claims this is insignificant, but this remains to be seen in practice

Overview

- BSPDN involves fundamental semiconductor architecture shift
- BSPDN is expected to cause several improvements to semiconductor performance (~5% boost in clock speed, ~25% reduction in IR losses in BEOL)
- Integration challenges remain to be seen: Critics believe yield and thermal losses may offset most of gains from this technique, unless further new innovations are made

Rensselaer

why not change the world?®