Rensselaer
IEEE Student Branch

Rensselaer Polytechnic Institute
EPS

BEOL

David King

GBM Attendance

General Updates

- DL Seminar Next Week
- Albany Nanotech Complex Tours

Albany Nanotech Complex Tour

- Albany Nanotech Complex
  - A state-of-the-art campus that brings together industry leaders, academia and international partners to develop next-generation chips and chip fabrication processes.
  - Major Companies:
    - IBM, Applied Materials, Tokyo Electron, Wolfspeed
  - Tour Dates:
    - February 26th (Wednesday), 11:30 AM – 1:30 PM
    - March 12th (Wednesday), 11:30 AM – 1:30 PM
- More tours are coming in the future!
- **<u>Tour attendees must be IEEE EPS members!</u>**

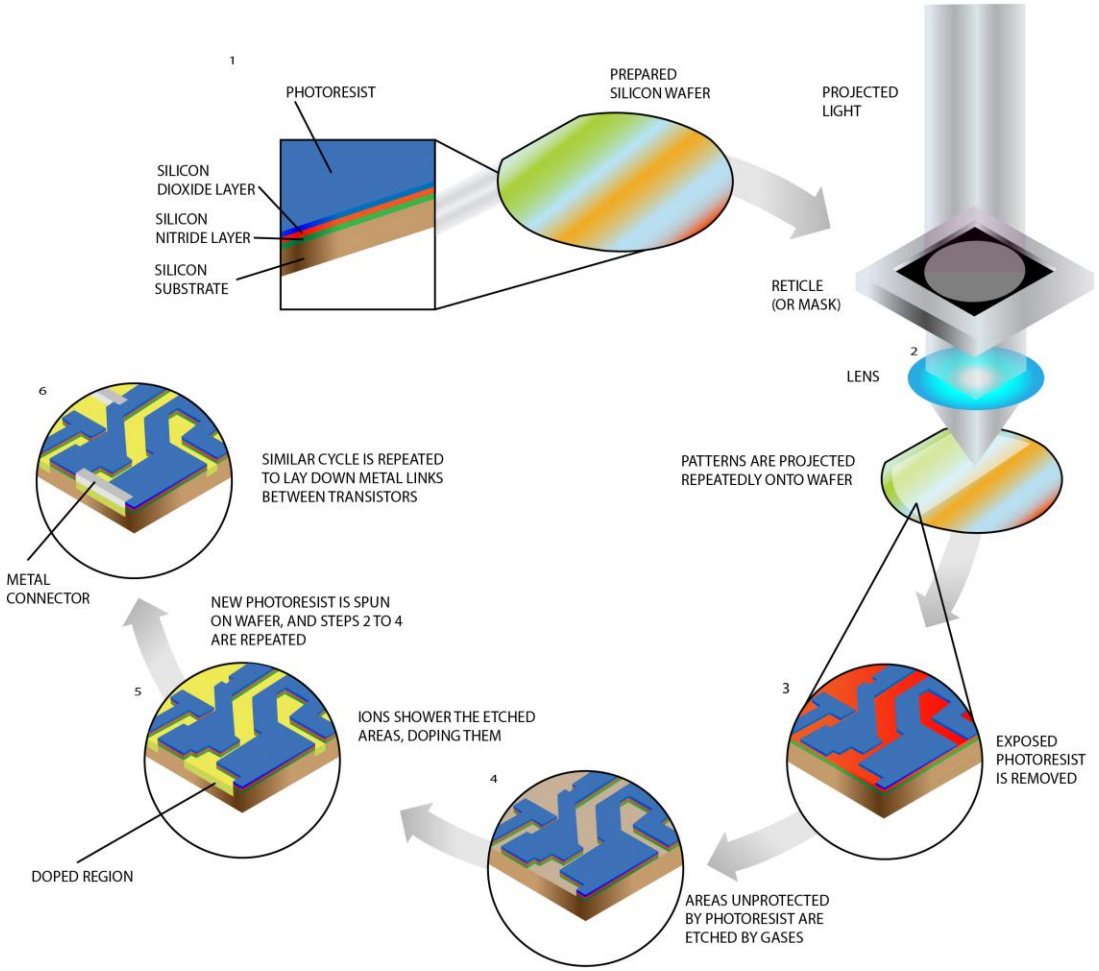
Distinguished Lecturer Seminar – Dr Eric Perfecto

- Distinguished Lecturer Seminar
  - When: Thursday, Feb 6th @ 6:00 PM
  - Where: LOW 3051
- Talk Highlights
  - Fundamentals of flip chip and Cu-pillar technology.
  - Evolution from wire bonding to Cu-pillar for fine pitch interconnects.
  - Use of advanced laminates, fan-out wafer-level packaging (FO-WLP), Si-bridges, interposers, and hybrid bonding.
- **PIZZA!** 

What are we covering today?

- FEOL
  - Basic Recap
  - The Transistor
  - PDKs and Logic Cells
- MEOL
  - Layer Overview
- BEOL
  - Layer Overview
  - Manufacturing Process

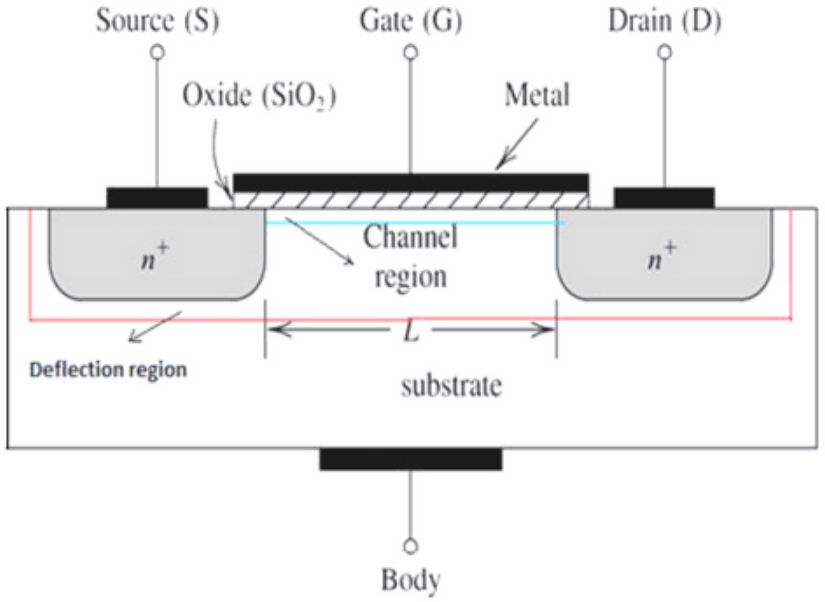
Lets Recap - FEOL

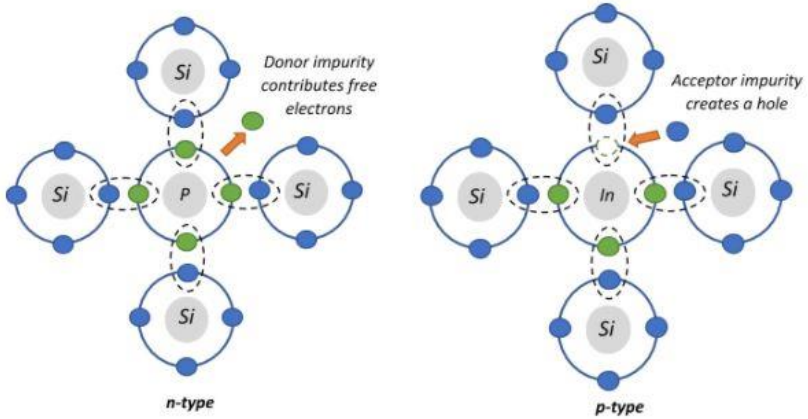


- In the last lecture, we covered the first stage of fabrication, referred to as front end of line (FEOL)
  - Focused on creating a layout of active devices.

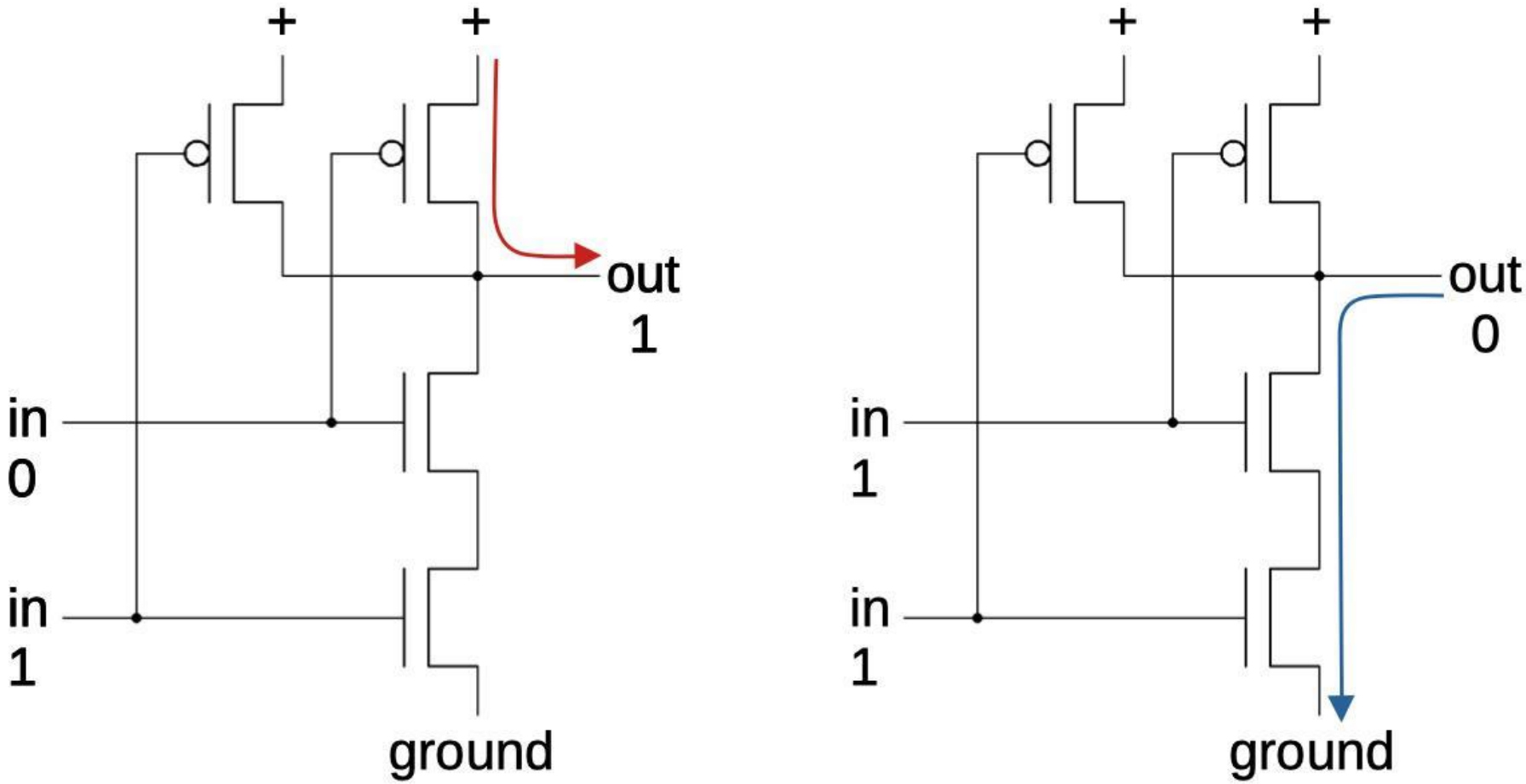
FEOL – The Transistor

The foundational building block of all logic gates

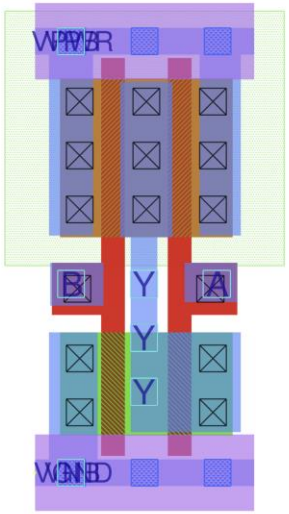


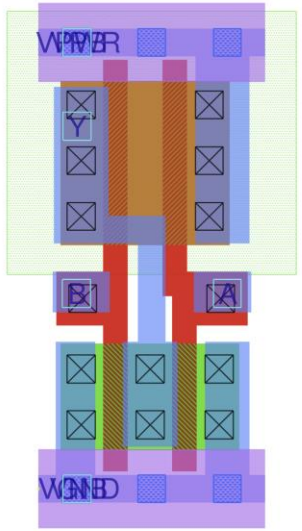


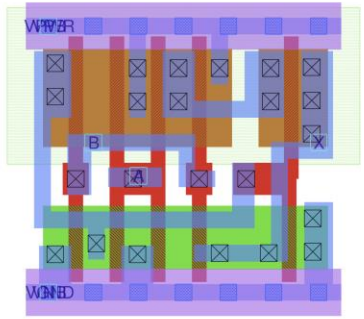
FEOL – An Example NAND gate

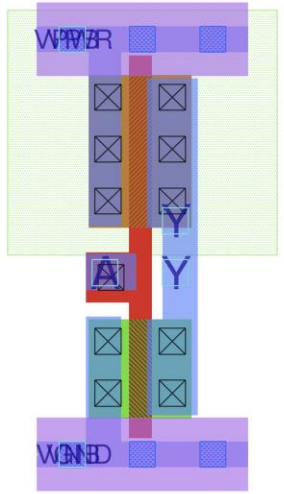


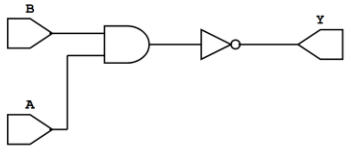
FEOL – Logic Standard Cells



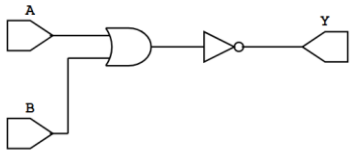




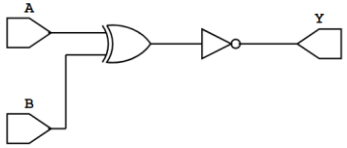




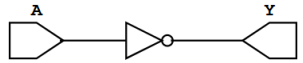
NAND



NOR

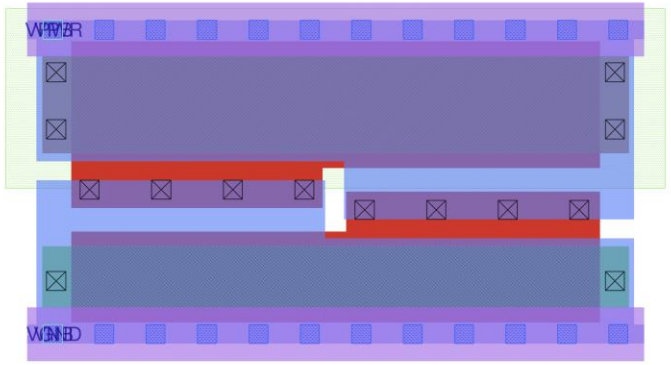


XNOR

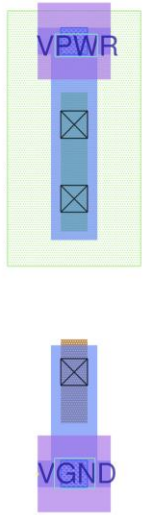


NOT

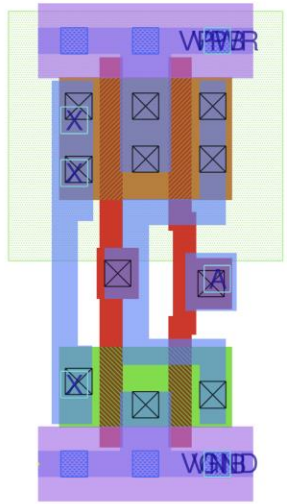
FEOL – Utility Standard Cells



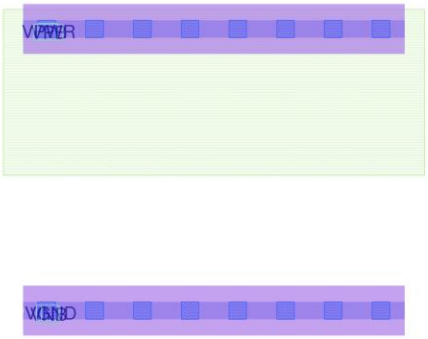
Decap



Well Tap



Clock Buffer



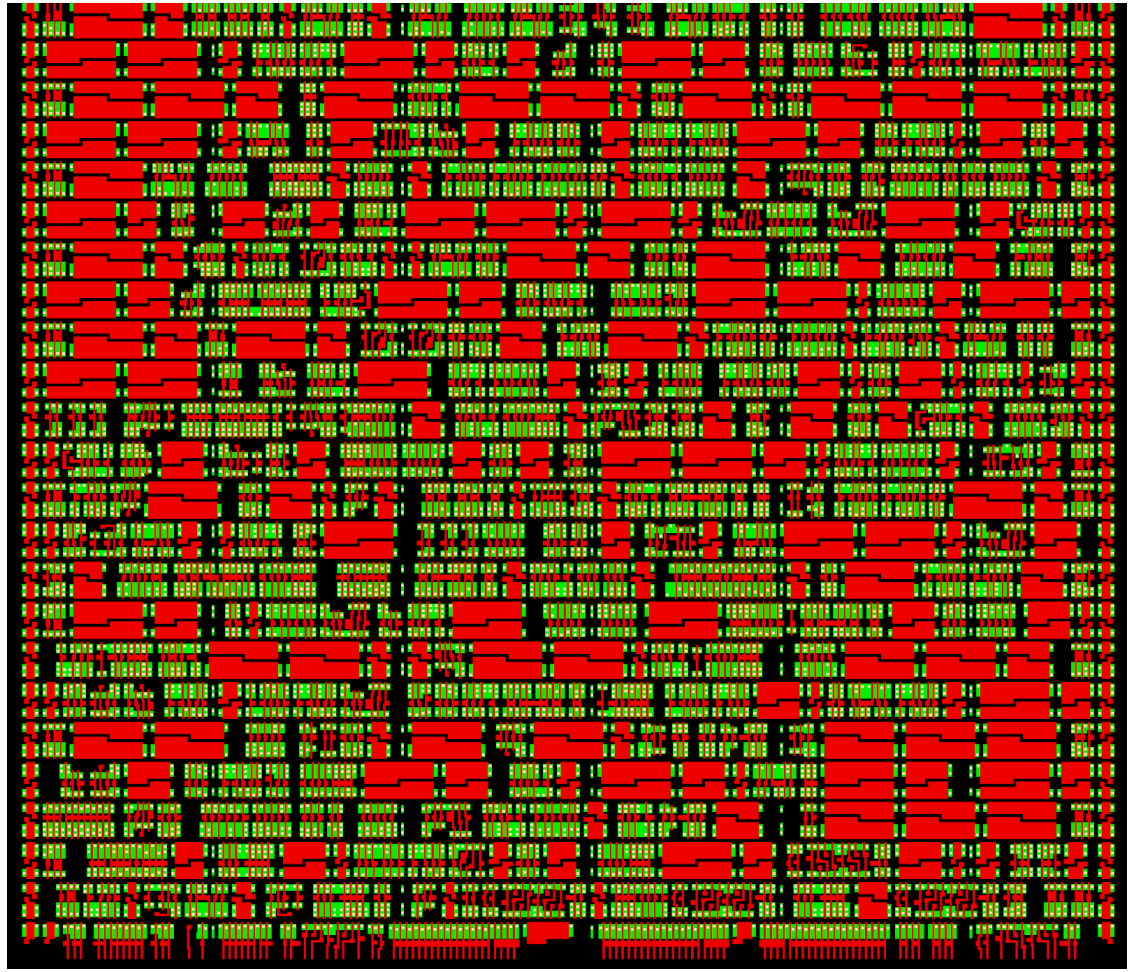
Fill

FEOL – What is the final product?

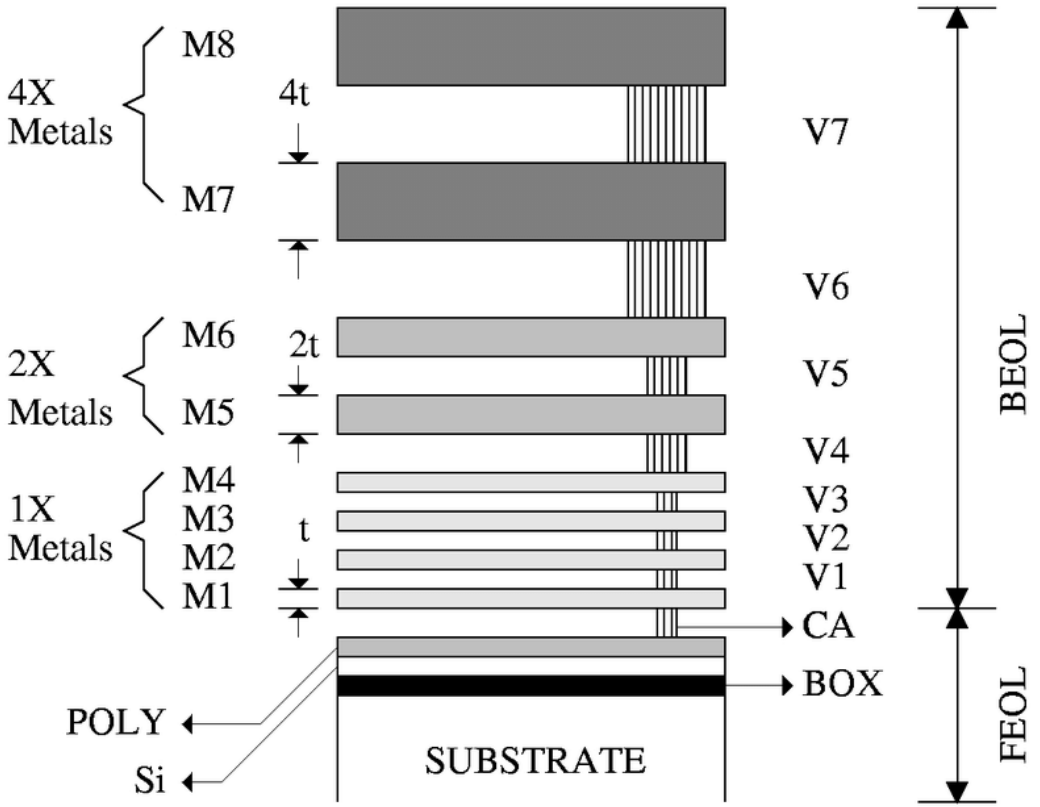
A big layout of active circuit elements

- Green: SOURCE and DRAIN materials
- Red: Polysilicon
- Gray: Channel

- How can we connect all of these devices?



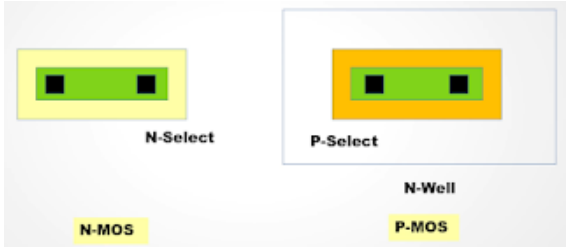
BEOL – Introducing the Interconnect

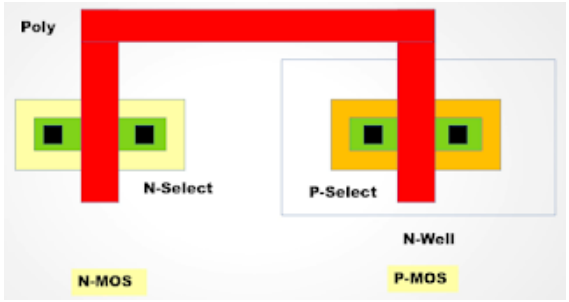


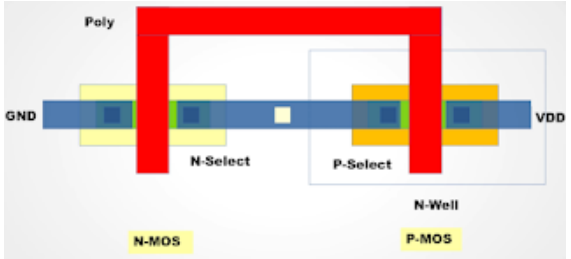
- Varying metal sizes:
  - 4X: Global Routing
  - 2X: Intermediate Routing
  - 1X: Local Routing
- Hierarchical Structure Optimizes:
  - Power
  - Area
  - Speed

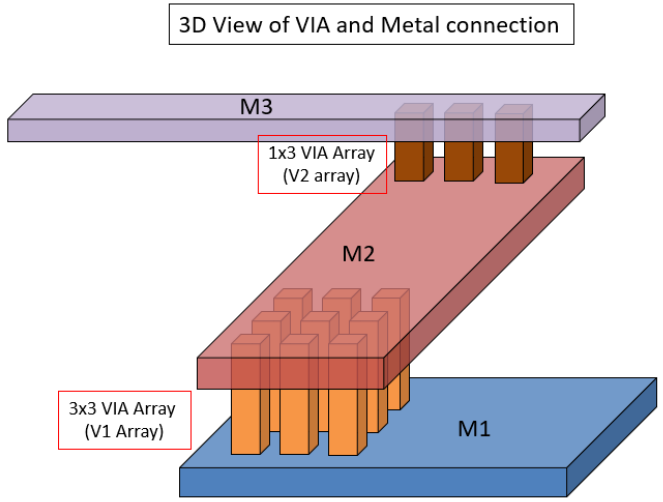
$$\rho = \frac{RA}{l}$$

BEOL – Anatomy – Vertical Connections







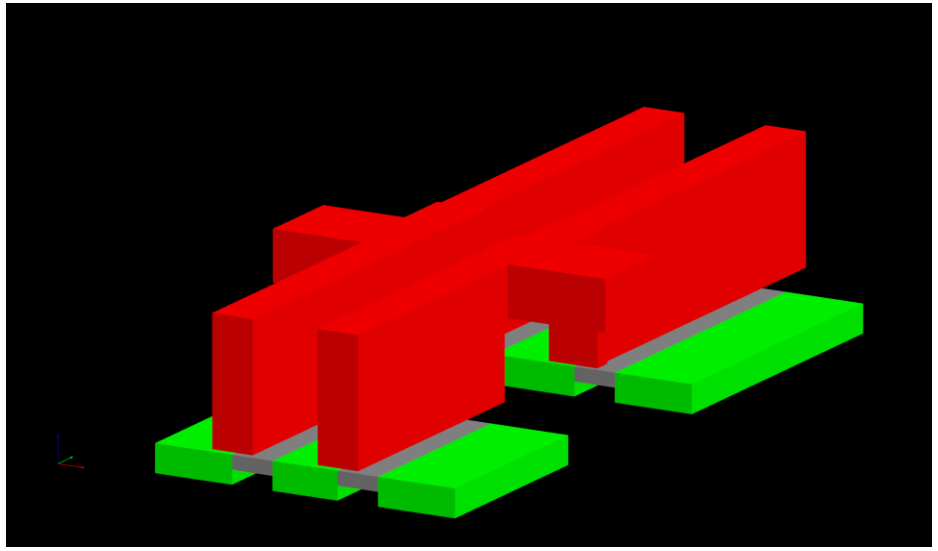


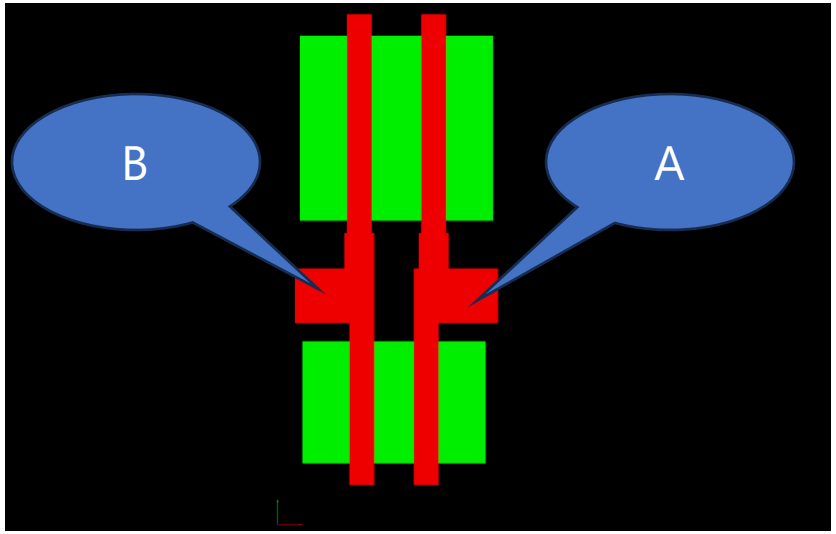
- Via: Usually refers to metal-metal connections between adjacent layers.
- Contact: A metal to lowest-level metal, n active, or polysilicon.

Design Considerations:

- Vias are usually only allowed between adjacent layers
- Vias are always the same size

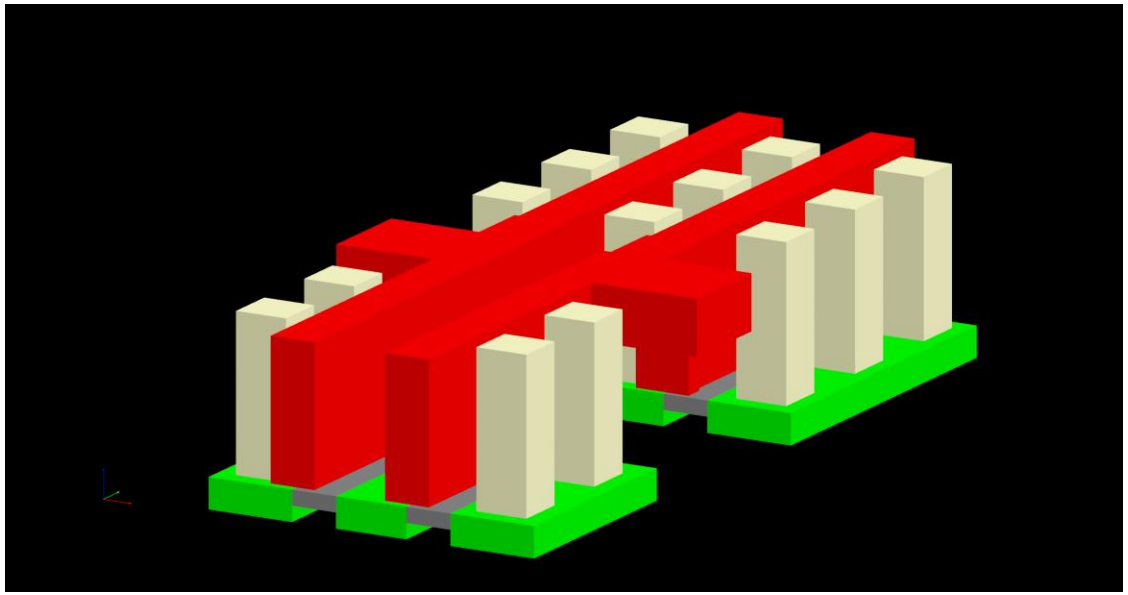
FEOL – The Finished Product





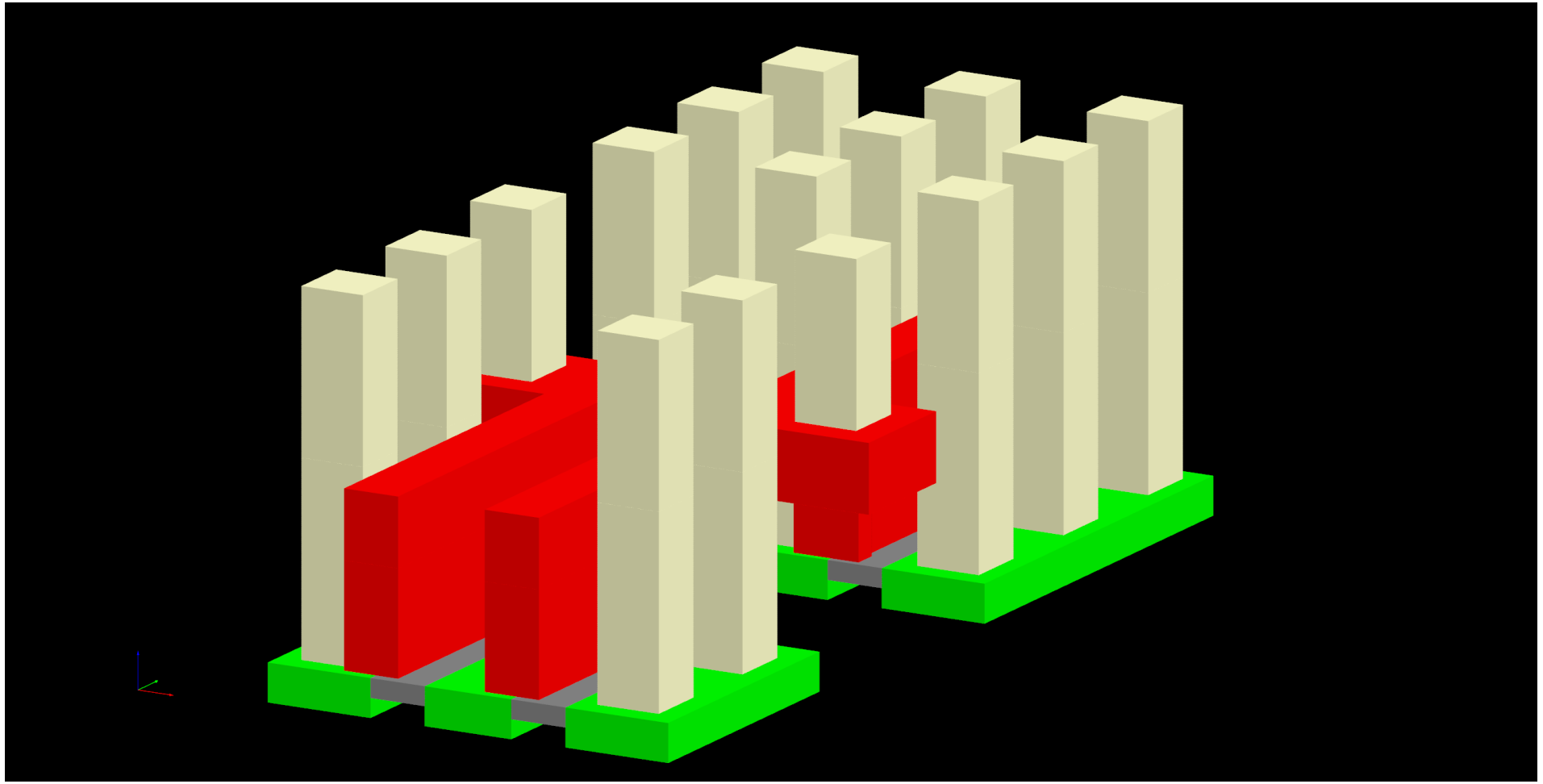
- This is a single logic standard cell produced by FEOL
  - Four transistors connected via polysilicon
  - Device functions but can't be powered or communicate

MEOL – First LICON

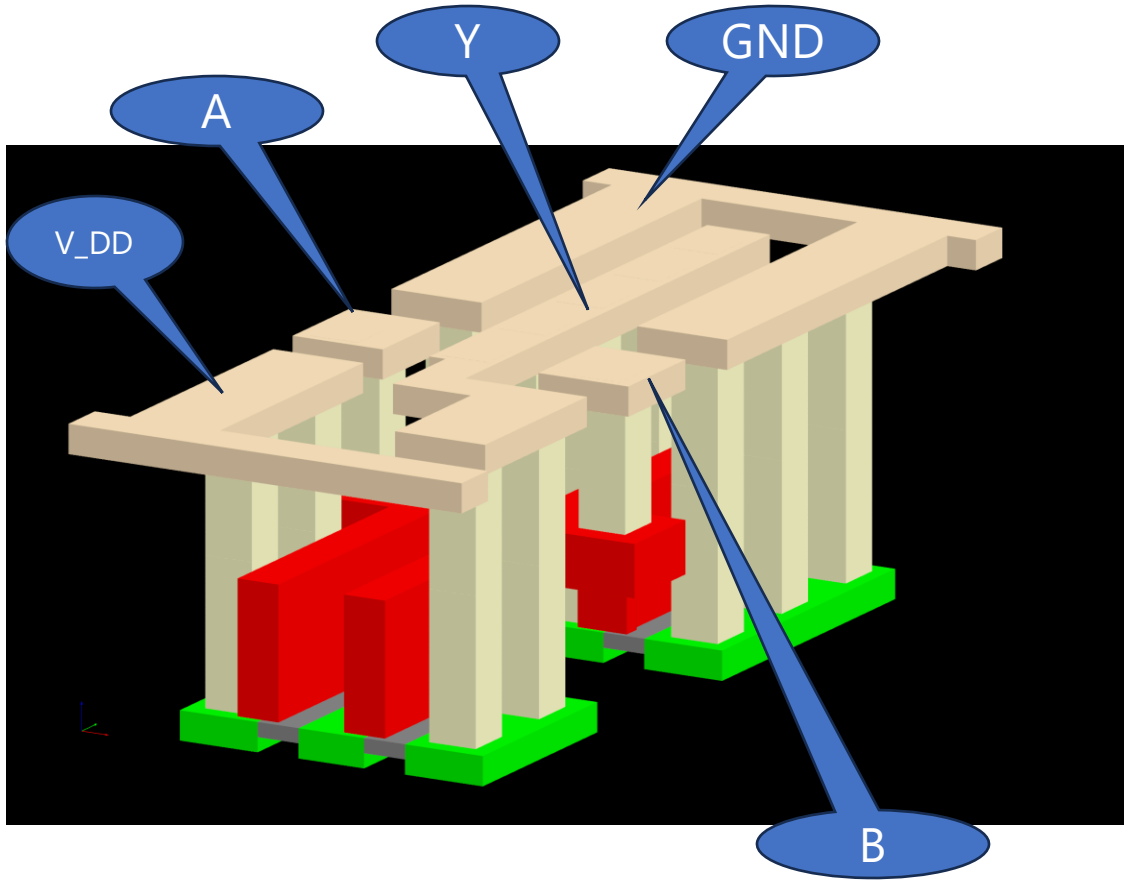


- These beige connections are called Local Interconnect Contacts (LICON) or W-Taps
  - They are typically made of Tungsten hence the W in W-Taps.
  - Tungsten is used because it acts as a barrier preventing copper from diffusing into the devices.
  - Tungsten also has good thermal properties

MEOL – Second Level LICON

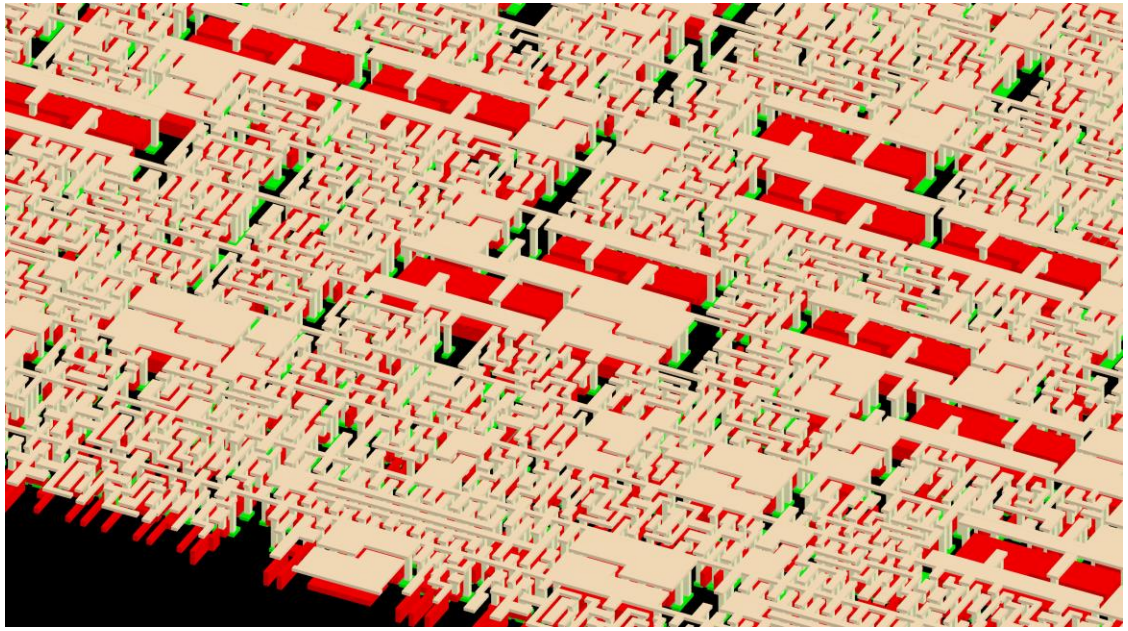


BEOL – Local Interconnect Layer 1 (LI1)



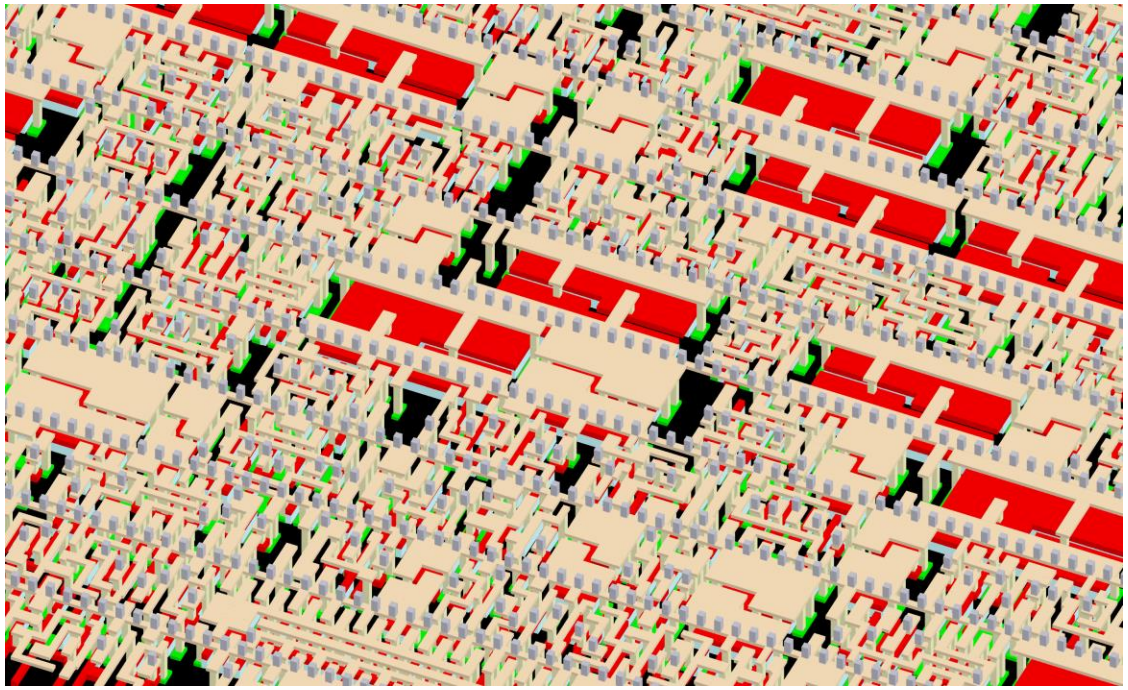
- This is a redistribution layer prepping for an increase in interconnect pitch size
- It also gives more room for via placement.

BEOL - Purpose



All of our standard cells are prepared to be connected globally.

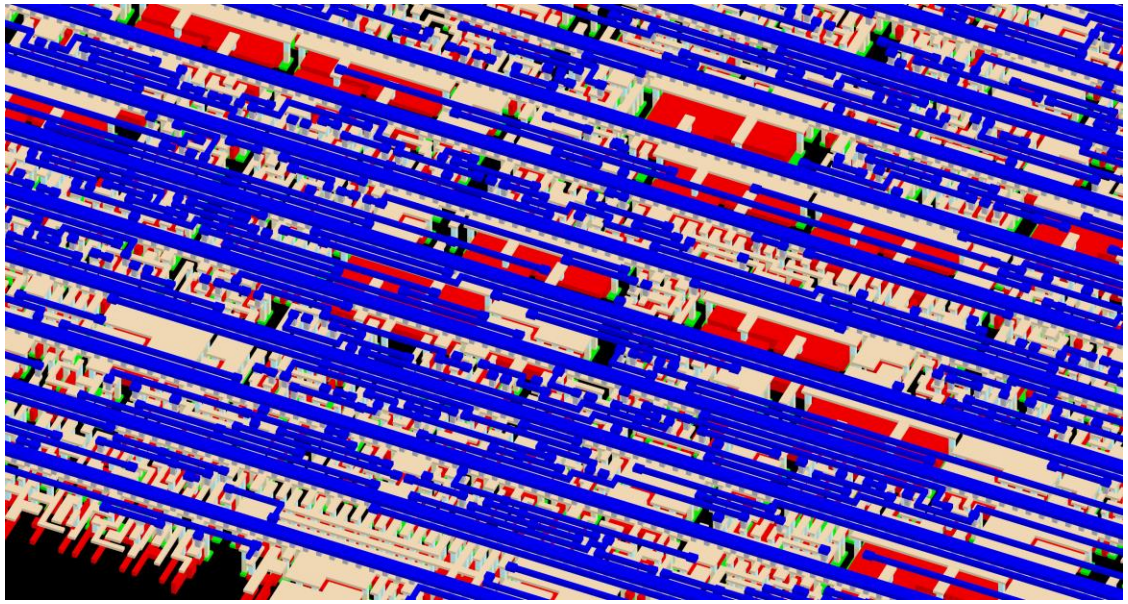
BEOL – MCON



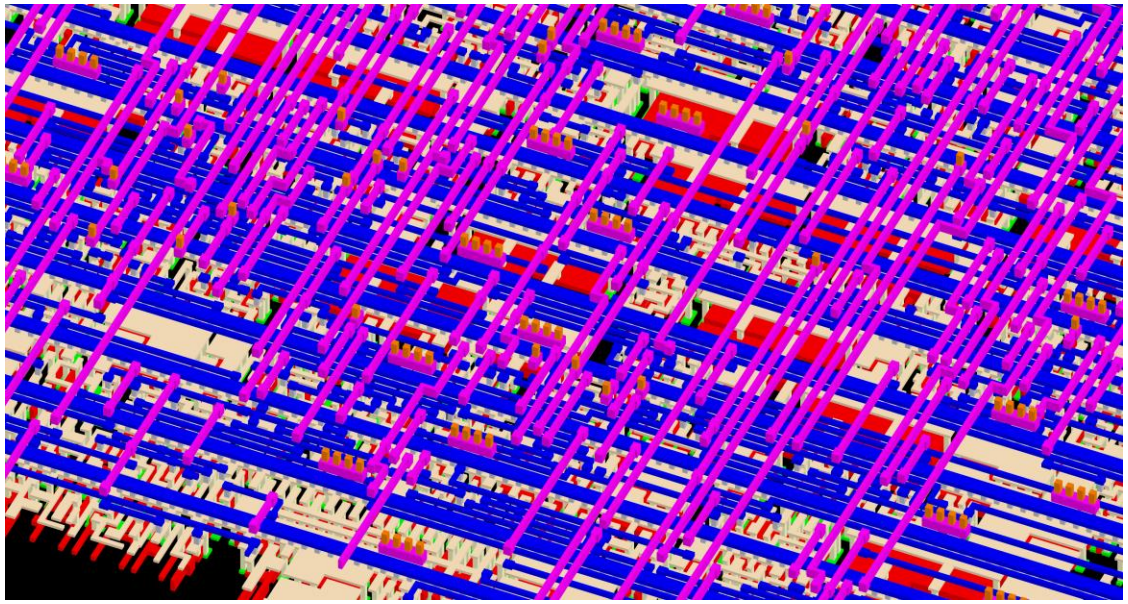
MCON prepares to connect LI1 to MET1 for local routing.

BEOL – MET1

MET1 handles connections in the X-axis.



BEOL – MET2 and VIA2

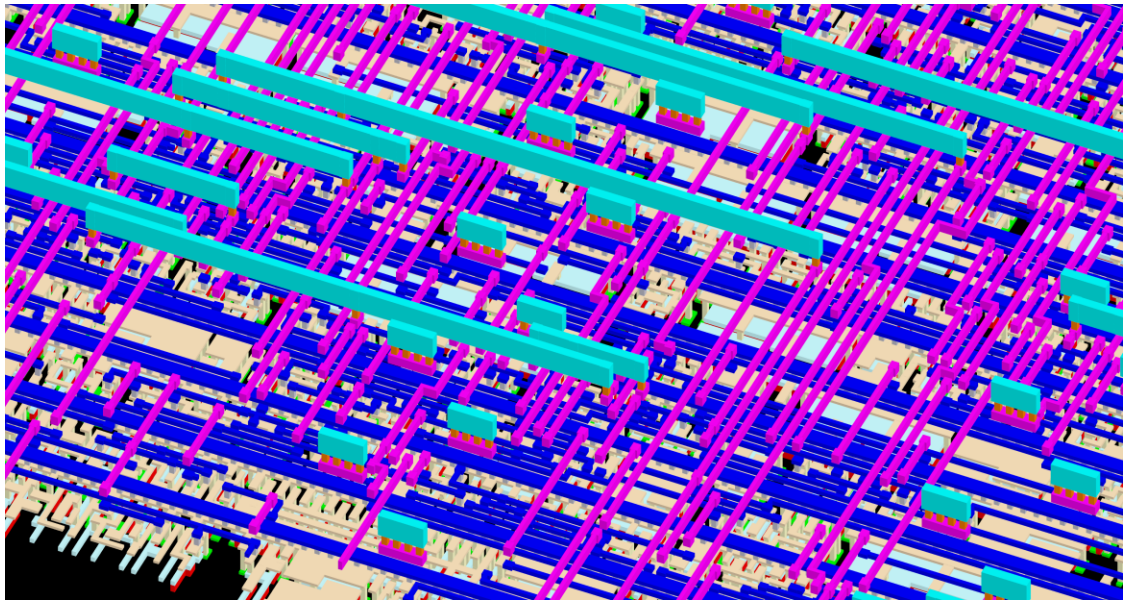


MET2 handles connections in the Y-axis.

NOTE:

- I accidentally put VIA2 before MET2 and I can't retake the picture, so now they share a slide.
- MET1 and MET2 are also connected through VIA1

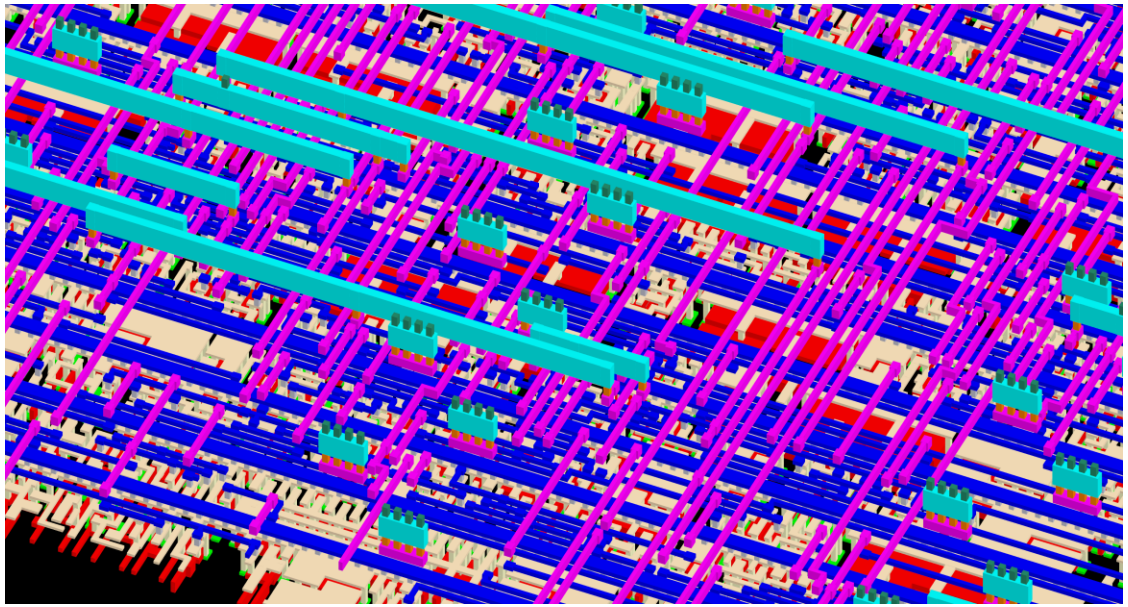
BEOL – MET3



MET3 handles global routing in the x-axis.

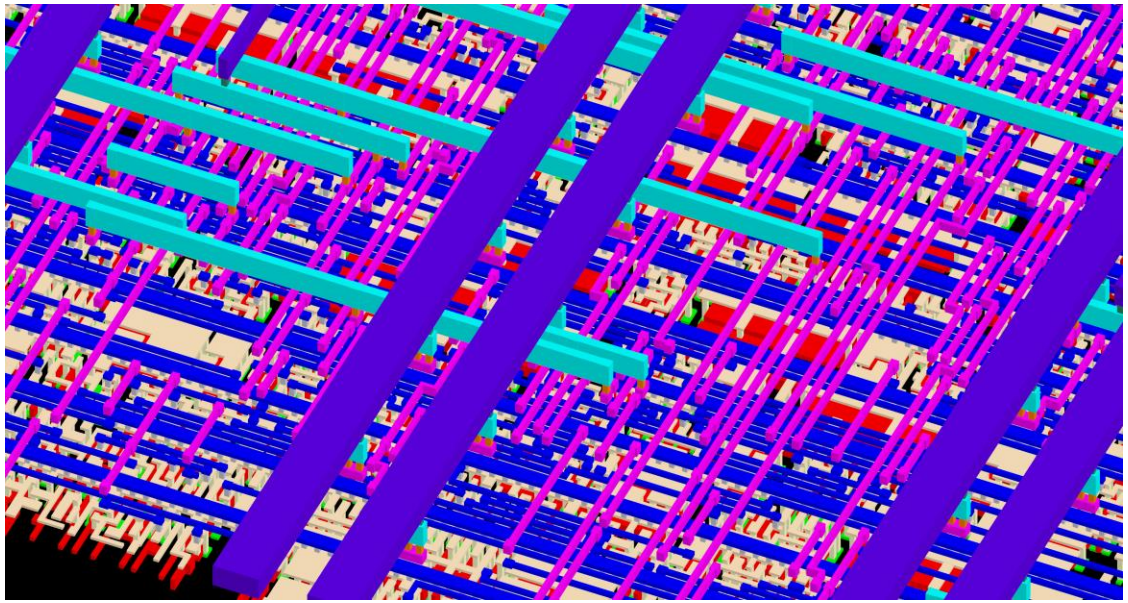
For some reason SkyWater doesn't have a y-axis.

BEOL – VIA3



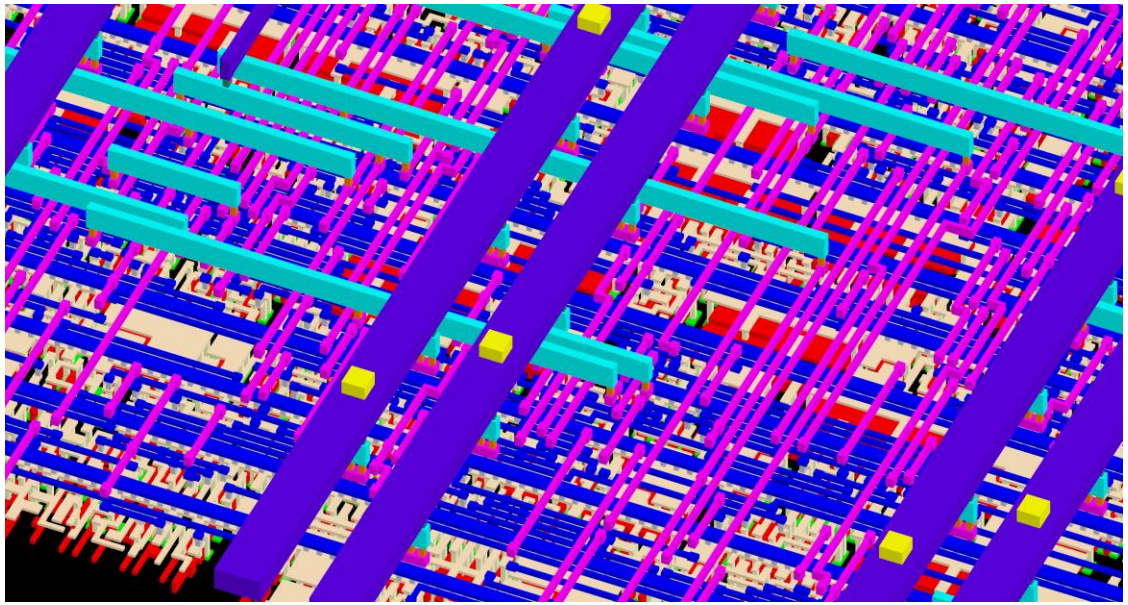
VIA3 connects MET3 to the power distribution network in MET4.

BEOL – MET4



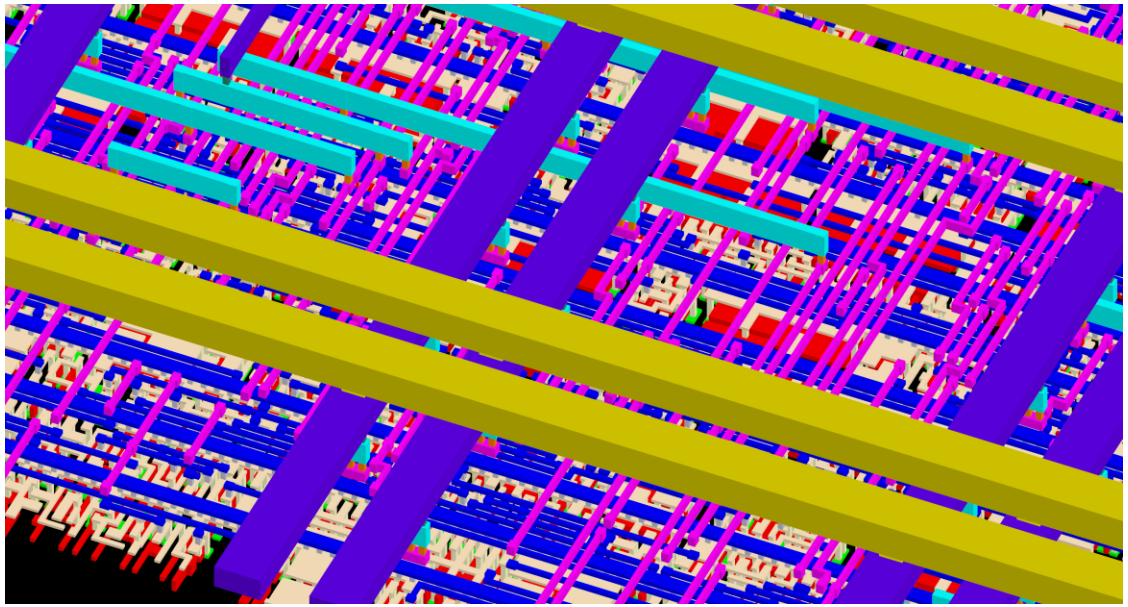
MET4 handles power distribution in the y-axis.

BEOL – VIA4



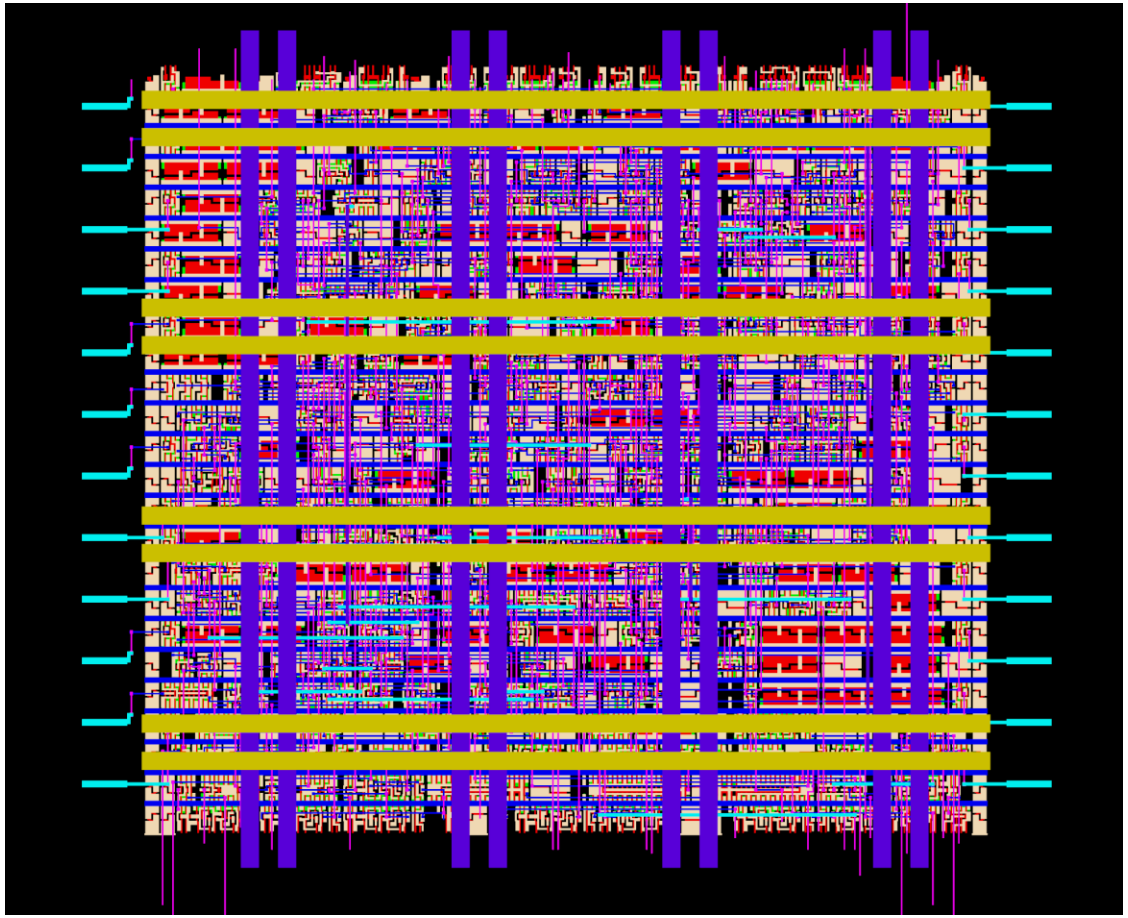
Connects the MET4 and MET5 power distribution networks.

BEOL – MET5



MET5 handles power distribution in the x-axis.

BEOL - PDN

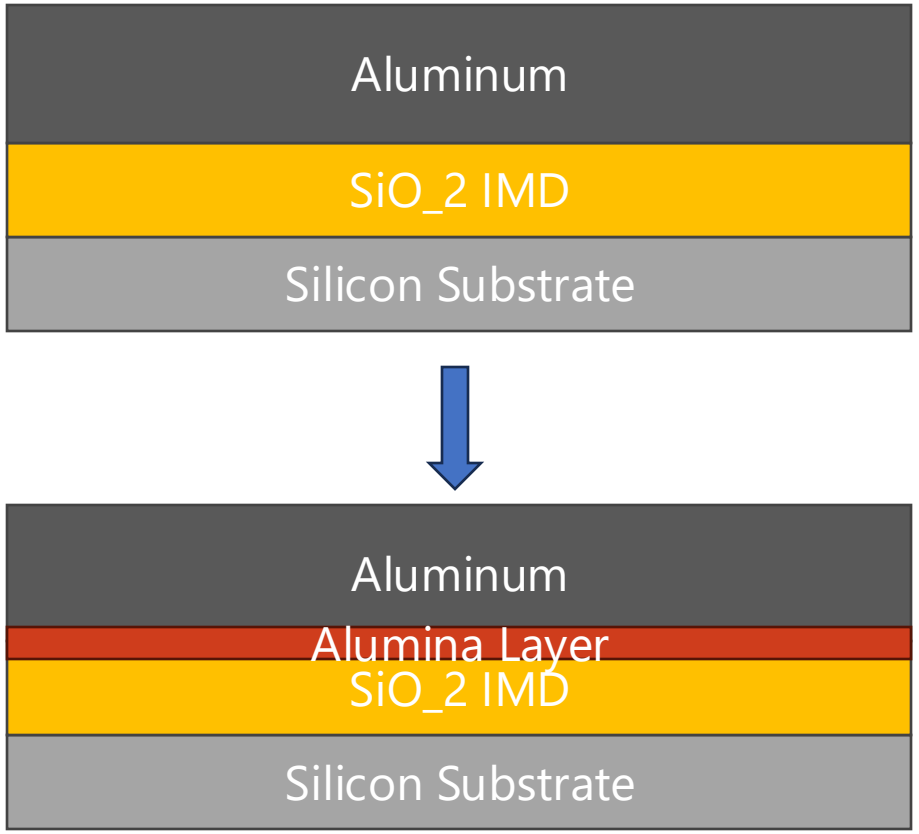


MET4 and MET5 create an intersecting pattern to ensure even distribution of power.

The First Interconnects

In the dark ages we used:

1. Silicon Dioxide as a dielectric
2. Aluminum as an interconnect

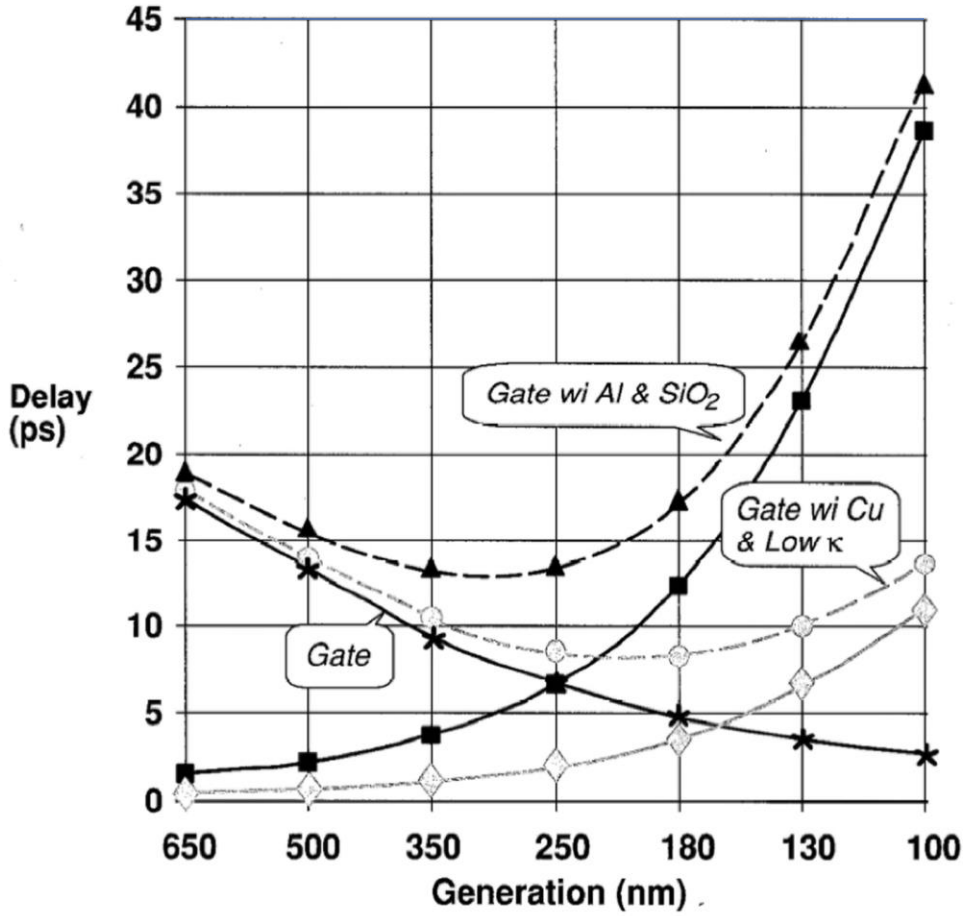


They were great:

- Silicon Dioxide easily deposited via CVD
- Aluminum has the fourth highest conductivity
- Aluminum is easily etched, with no volatile byproducts
- They were best friends (They create Aluminum Oxide)

Scaling Challenges on the Horizon

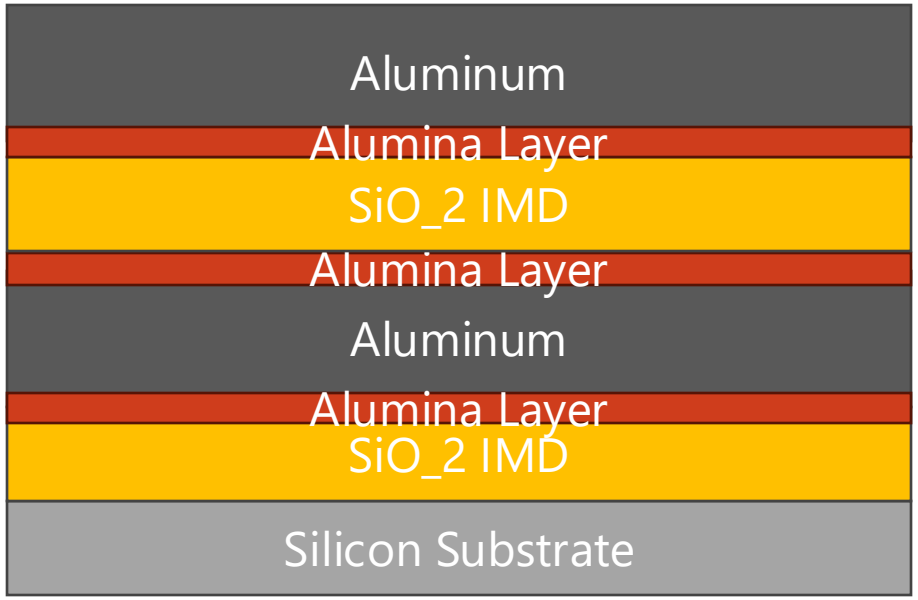
- Pitch Size Change:
  - 1978 M2: 20 um
  - 1994 Global: 1.8 um
- Challenges:
  - Resistance
  - RC Delay



More on RC Delay

$$\tau = RC = \left(\frac{\rho L}{A}\right) * \left(\frac{k\epsilon_0 A}{d}\right)$$

We can't increase the interconnect density

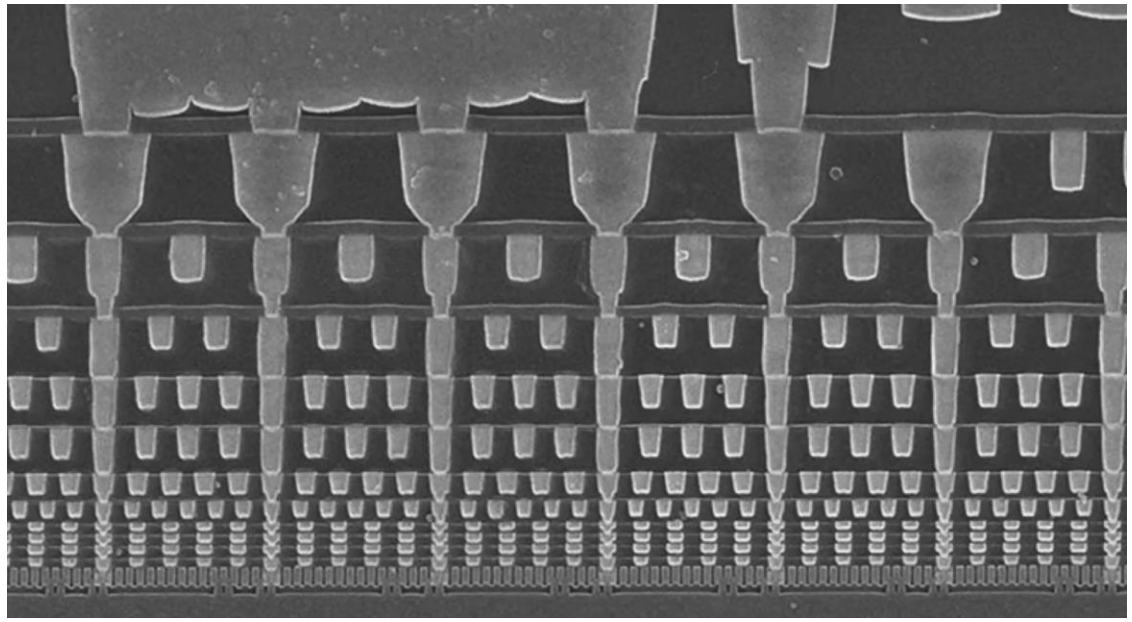


The Easy Solution

If we can’t increase the density on a layer

Why not just add more?

Yield



The Hard Solution

Changing the materials:

- Lower Resistance Metal
- Lower K Dielectric

Copper is an excellent choice:

- Lower resistance
- Lower electromigration

The industry also made a thing called Low-K dielectric.

How creative

- It can be literally any material; it just has to have a lower k then Silicon Dioxide.

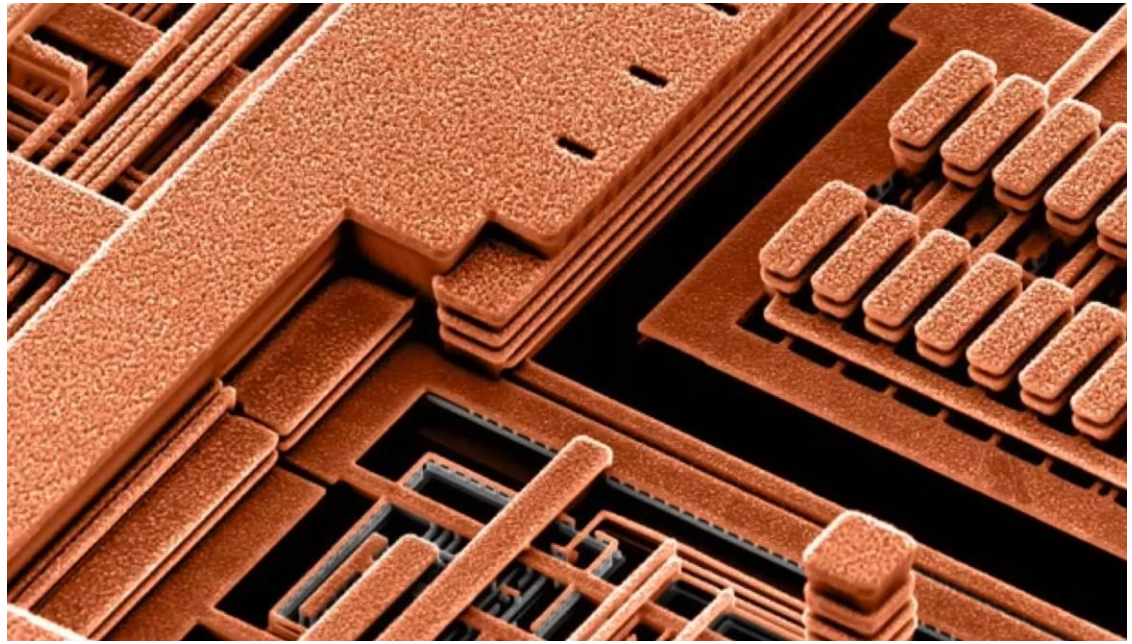
Conductors for Multilayer Interconnections:

Table 1 Properties of interconnect materials.

Material	Thin film resistivity ($\mu\Omega - cm$)	Melting point (˚C)
Cu	1.7-2.0	1084
Al	2.7-3.0	660
W	8-15	3410
PtSi	28-35	1229
$TiSi_2$	13-16	1540
WSi_2	30-70	2165
$CoSi_2$	15-20	1326
NiSi	14-20	992
TiN	50-150	~2950
$Ti_{30}W_{70}$	75-200	~2200
polysilicon (heavily doped)	500-1000	1410

Project Red Aluminum

- IBM wanted to create the first copper interconnect
- They had a team of engineers working 18 hours a day
    - For 15 years



"There was a real period of time when we lost all track of time… they couldn't pay someone enough to make them do it. It has to be a different sense of motivation" – Ron Goldblatt, IBM Engineer

Why did it take them so long?

- Plasma/Dry etching doesn't work on copper
  - Reaction products are not volatile
  - Subtractive patterning doesn't work
- Copper will diffuse into everything
- Whatever will we do?

Dual Damascene Process

- IBM pioneered a new fabrication process to use copper
- Damascene process – named for the decorative inlay metal process made famous is Damascus
- Additive instead of the typical subtractive process’

Dual Damascene Process – SiC Deposition

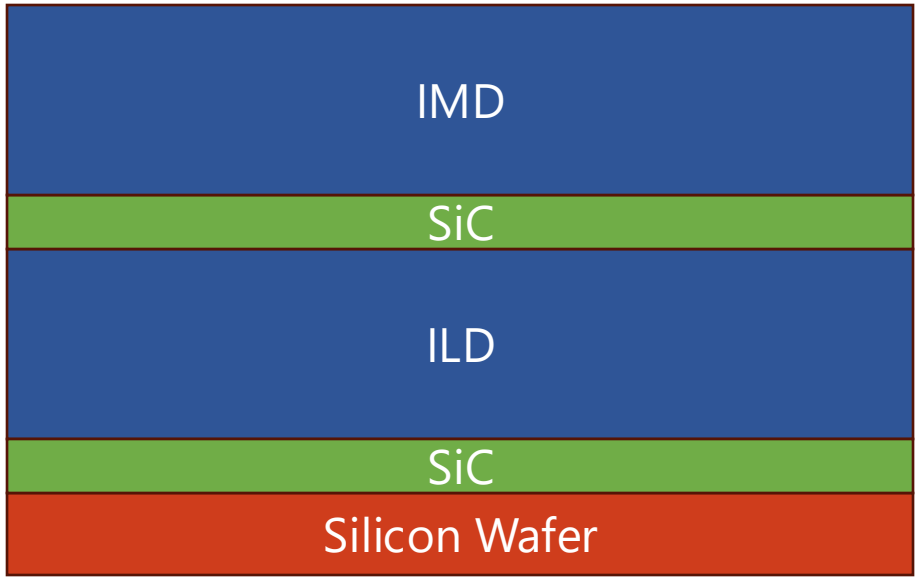
Cobalt Silicate is deposited to act as an etch stop

Dual Damascene Process – Dielectric Deposition

Deposit:

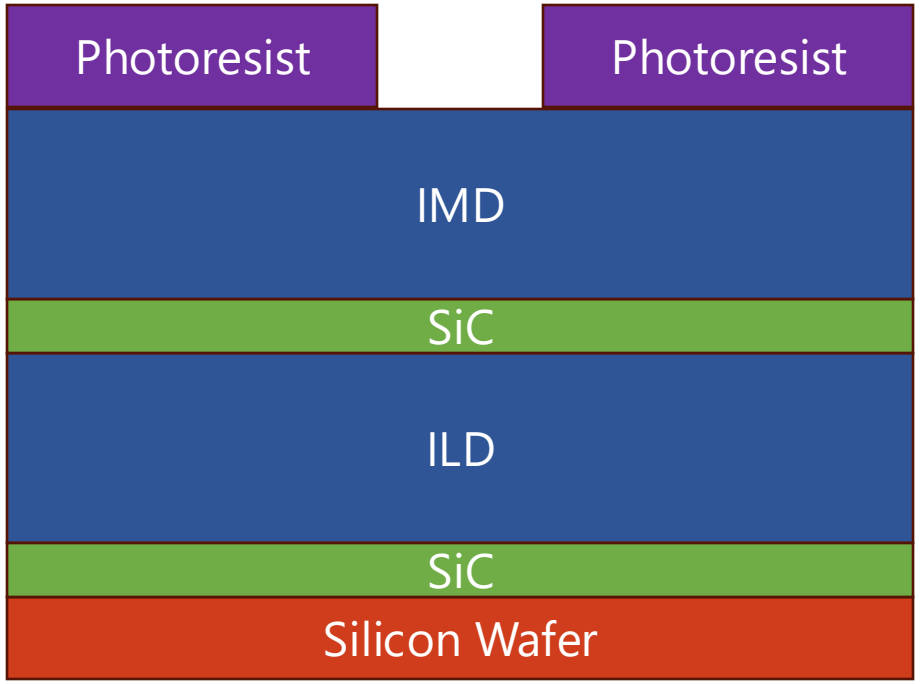
- Inter Layer Dielectric
- SiC
- Inter Metal Dielectric

ILD and IMD are usually made of the same material and are sometimes both referred to as IMD.



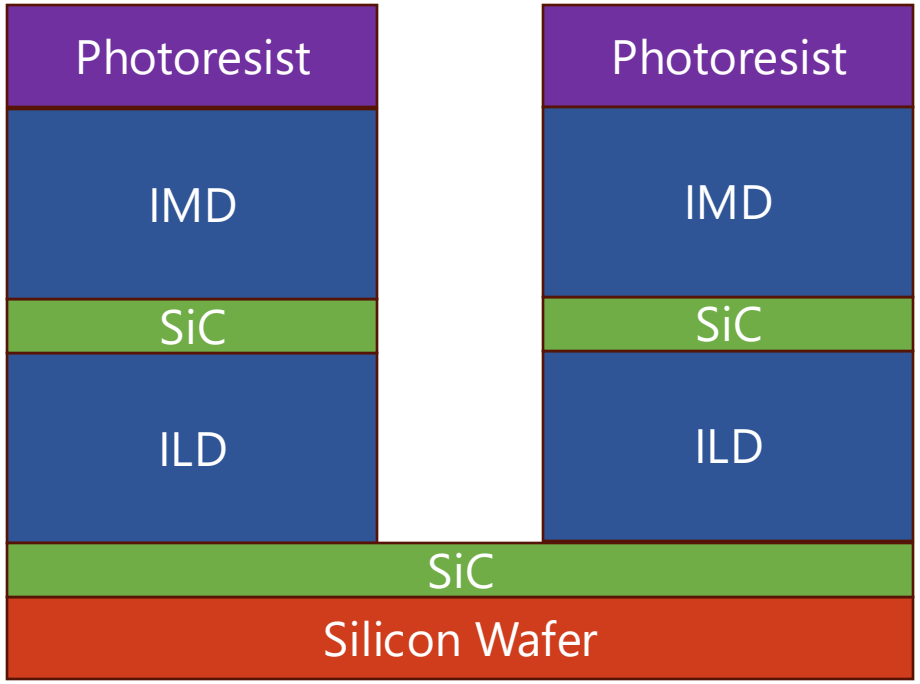
Dual Damascene Process – Etch Via

1. Photoresist is deposited
2. Patterning is done
3. IMD and ILD are etched creating the via
4. Strip Photoresist



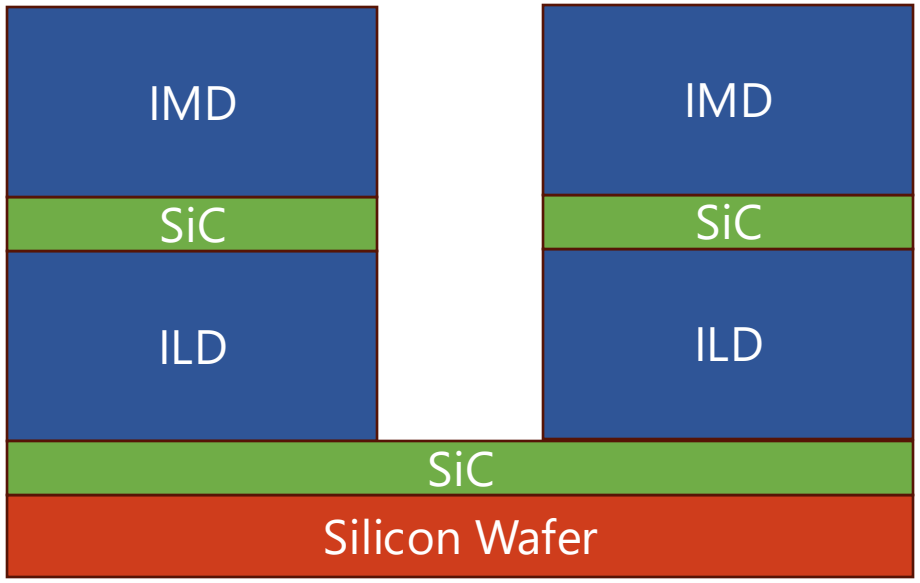
Dual Damascene Process – Etch Via

1. Photoresist is deposited
2. Patterning is done
3. IMD and ILD are etched creating the via
4. Strip Photoresist



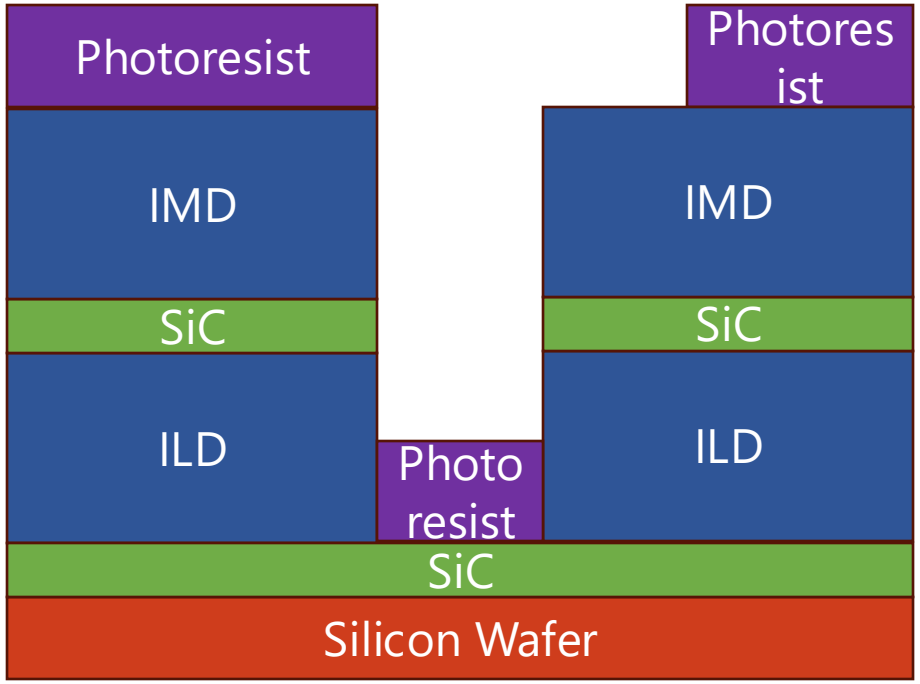
Dual Damascene Process – Etch Via

1. Photoresist is deposited
2. Patterning is done
3. IMD and ILD are etched creating the via
4. Strip Photoresist



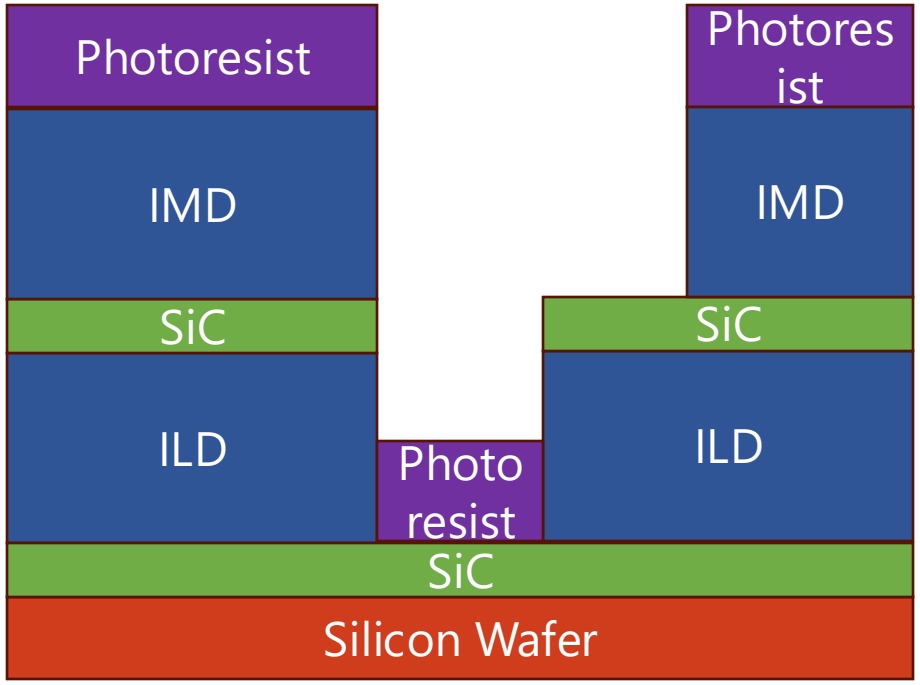
Dual Damascene Process – Etch Trench

1. Photoresist is deposited
2. Patterning is done
3. IMD is etched forming trench
4. Strip Photoresist



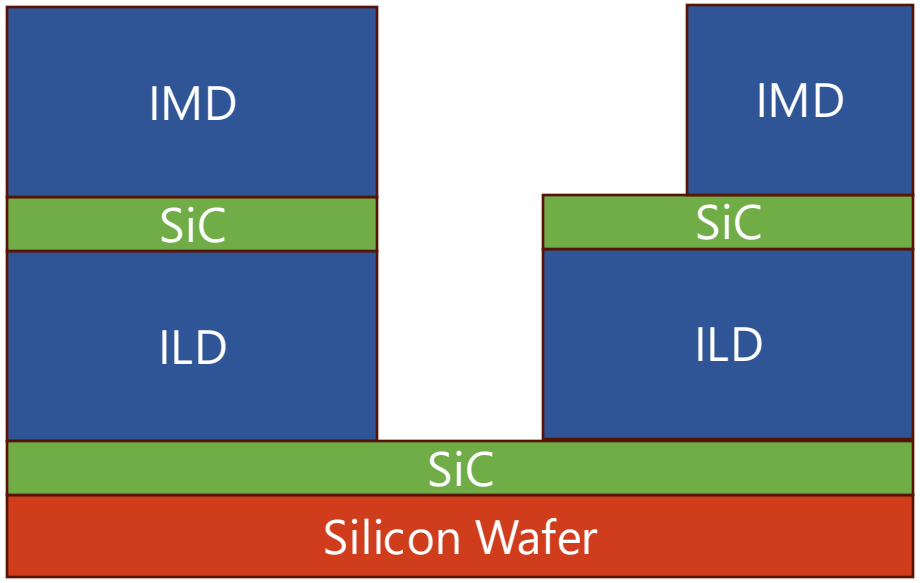
Dual Damascene Process – Etch Trench

1. Photoresist is deposited
2. Patterning is done
3. IMD is etched forming trench
4. Strip Photoresist



Dual Damascene Process – Etch Trench

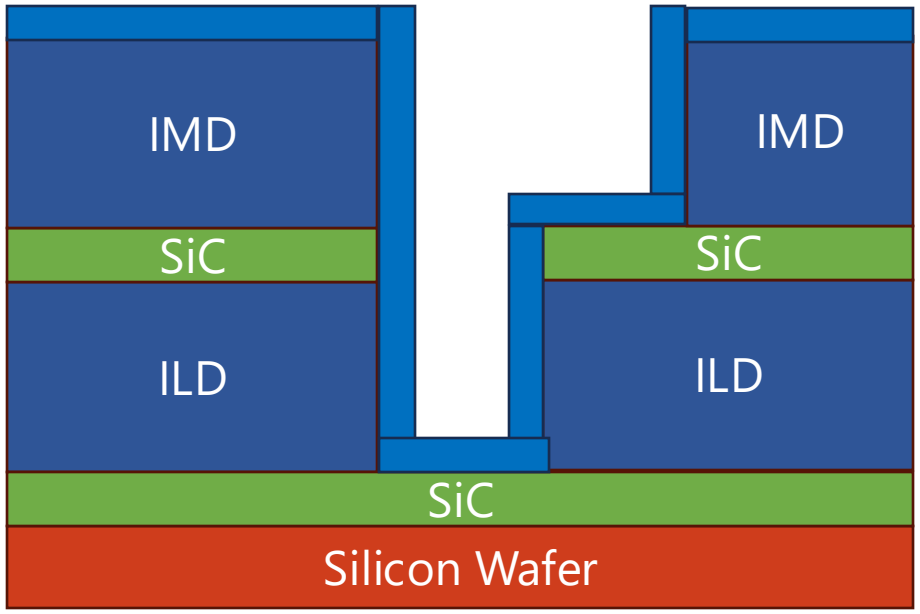
1. Photoresist is deposited
2. Patterning is done
3. IMD is etched forming trench
4. Strip Photoresist



Dual Damascene Process – Barrier Deposition

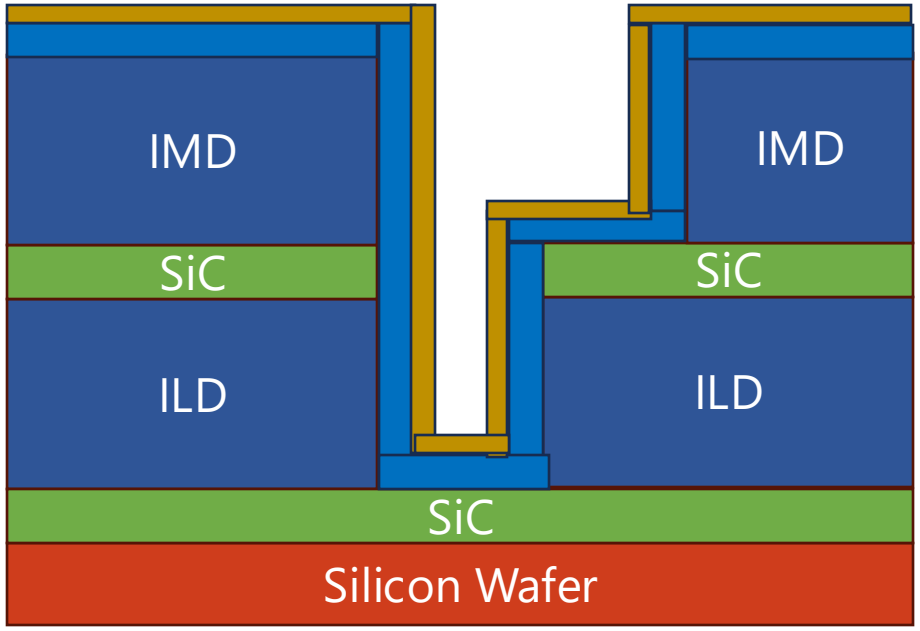
A barrier material such as TiN or Ta is deposited

This prevents copper from diffusing into any of the silicon based materials.

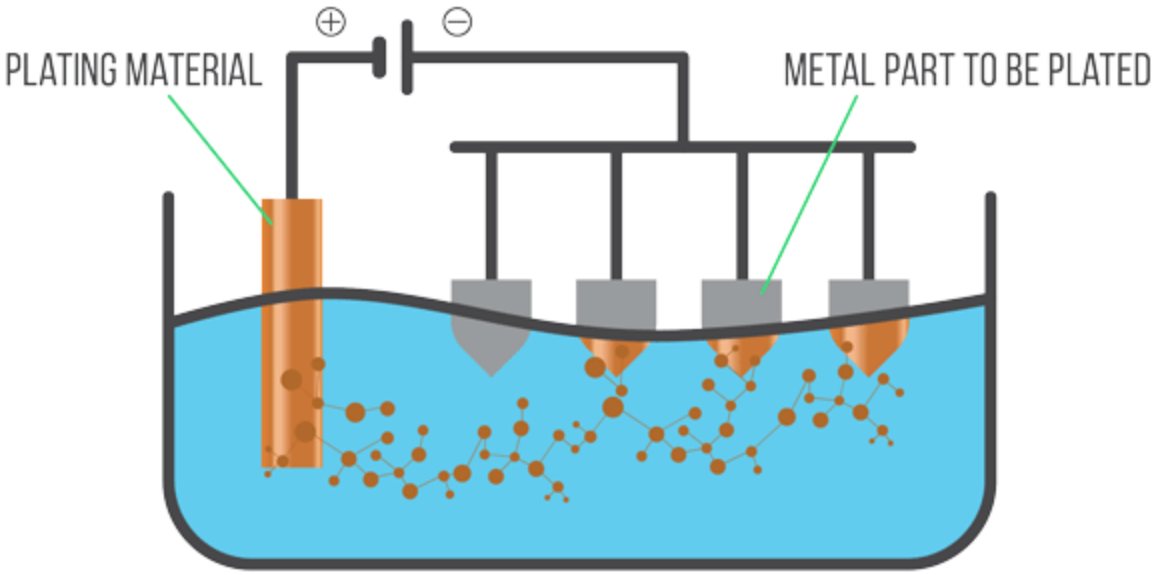


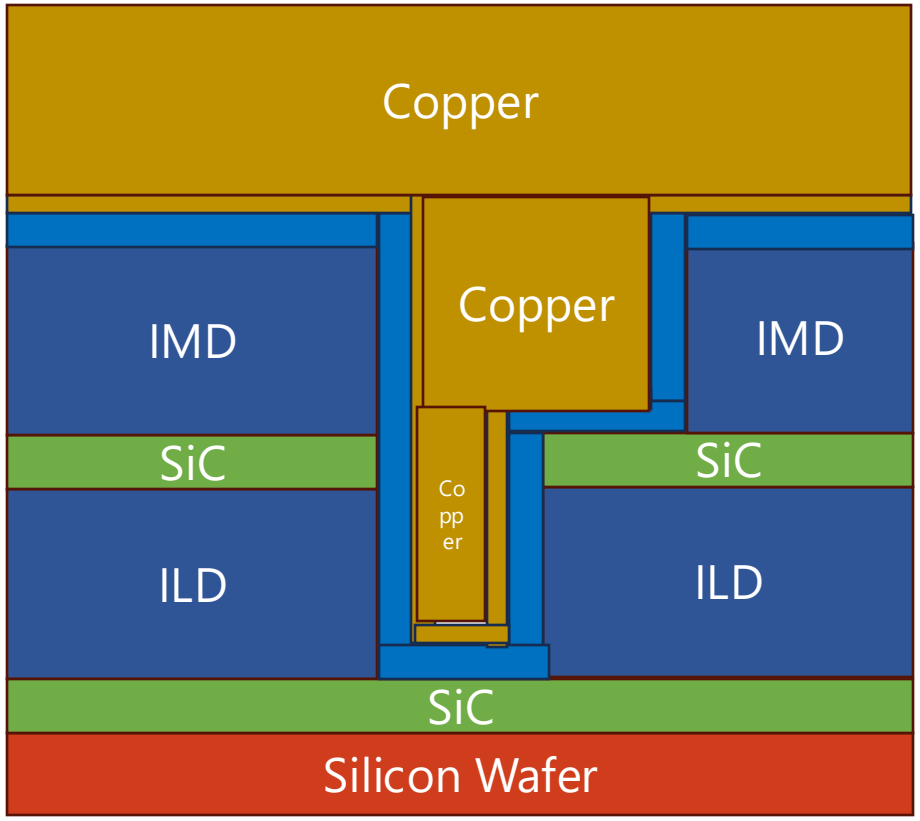
Dual Damascene Process – Copper Seed Layer Deposition

A copper seed level is deposited to promote electroplating adhesion.



Dual Damascene Process – Copper Electroplating

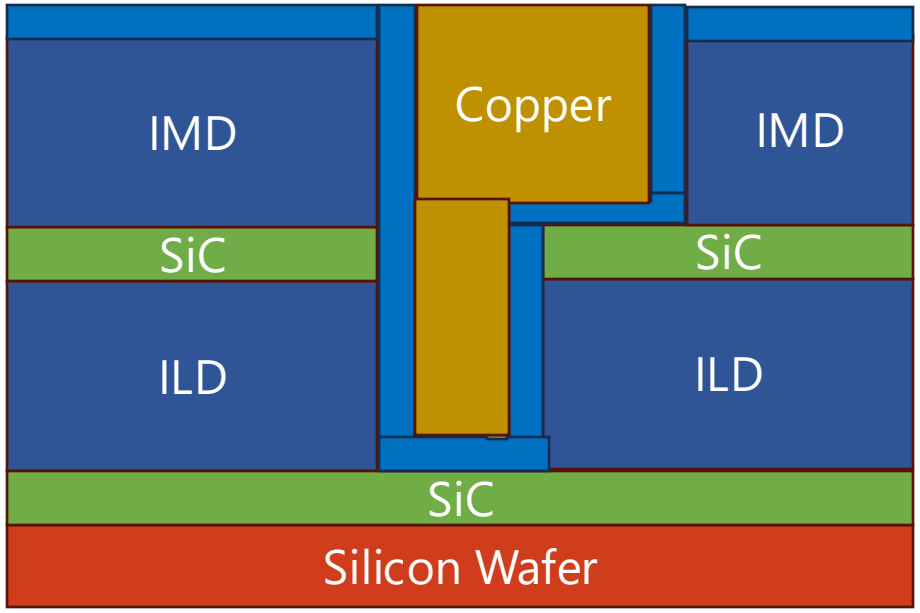




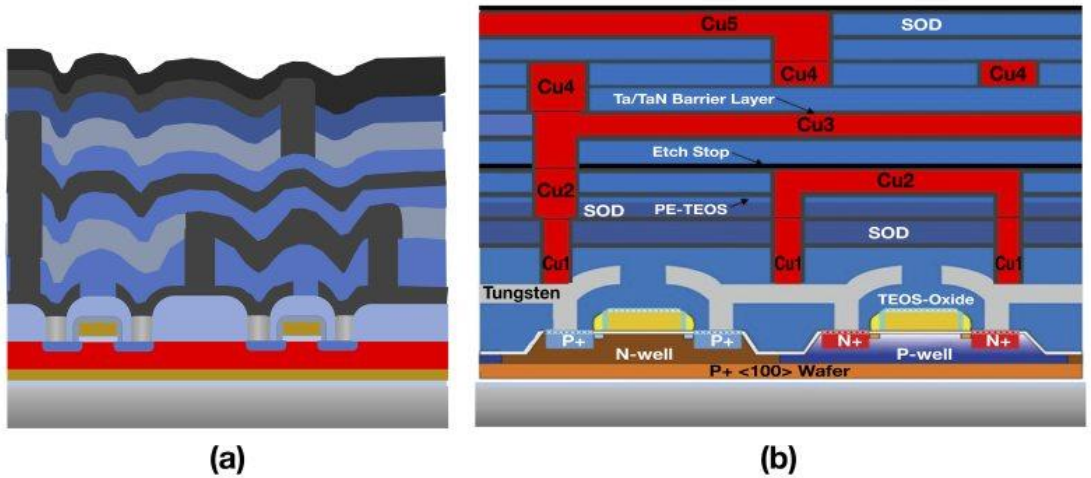
Dual Damascene Process – Chemical Mechanical Planarization

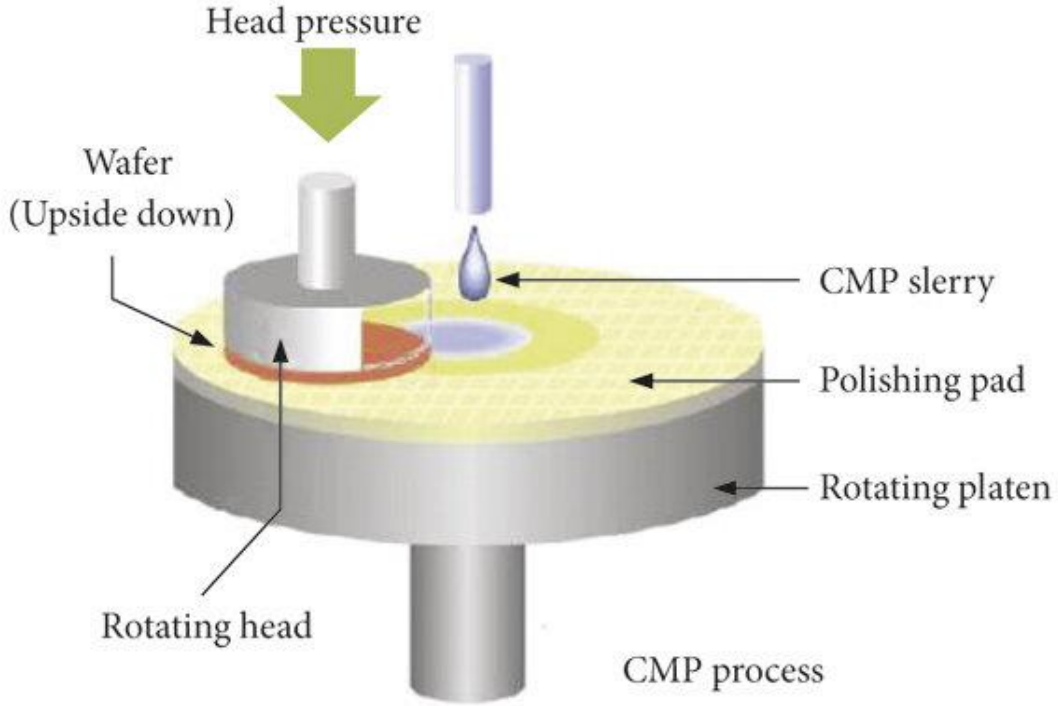
Acts as a subtractive step to remove any extra copper

Also ensures planarity across layer, allowing for better stacking and higher yield



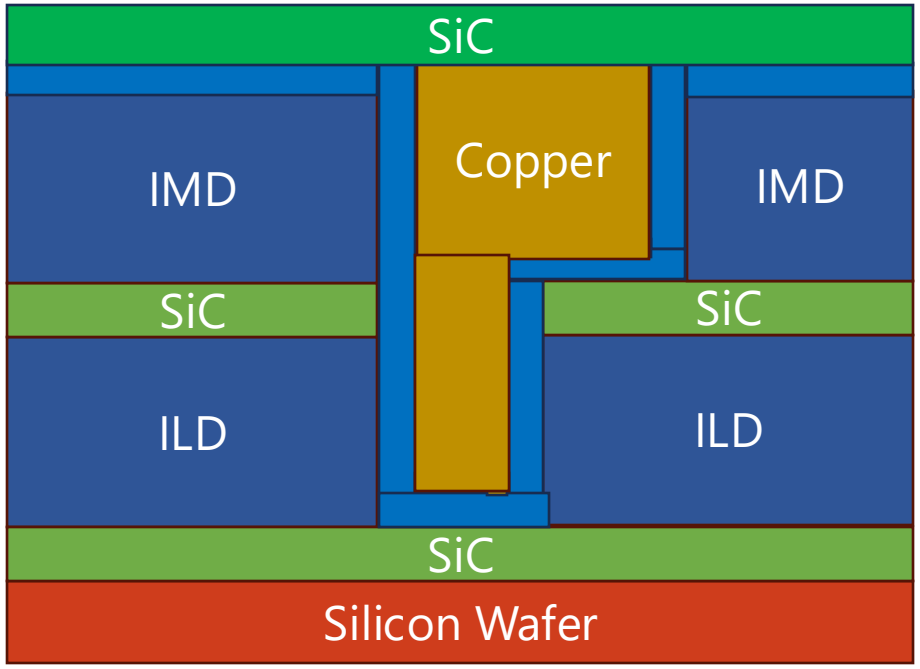
More on Chemical Mechanical Planarization





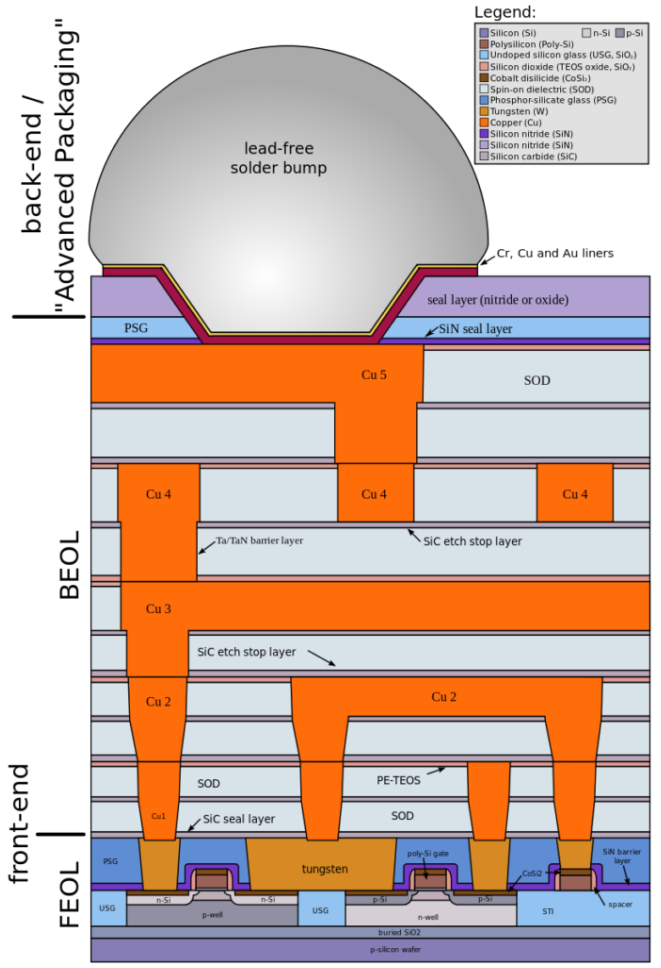
Dual Damascene Process – Cap Deposition

Cobalt Silicate is deposited to act as an etch stop for the next layer



Dual Damascene Process - Repeat

This process is repeated



That’s all!

Thanks for showing up!

GBM Attendance