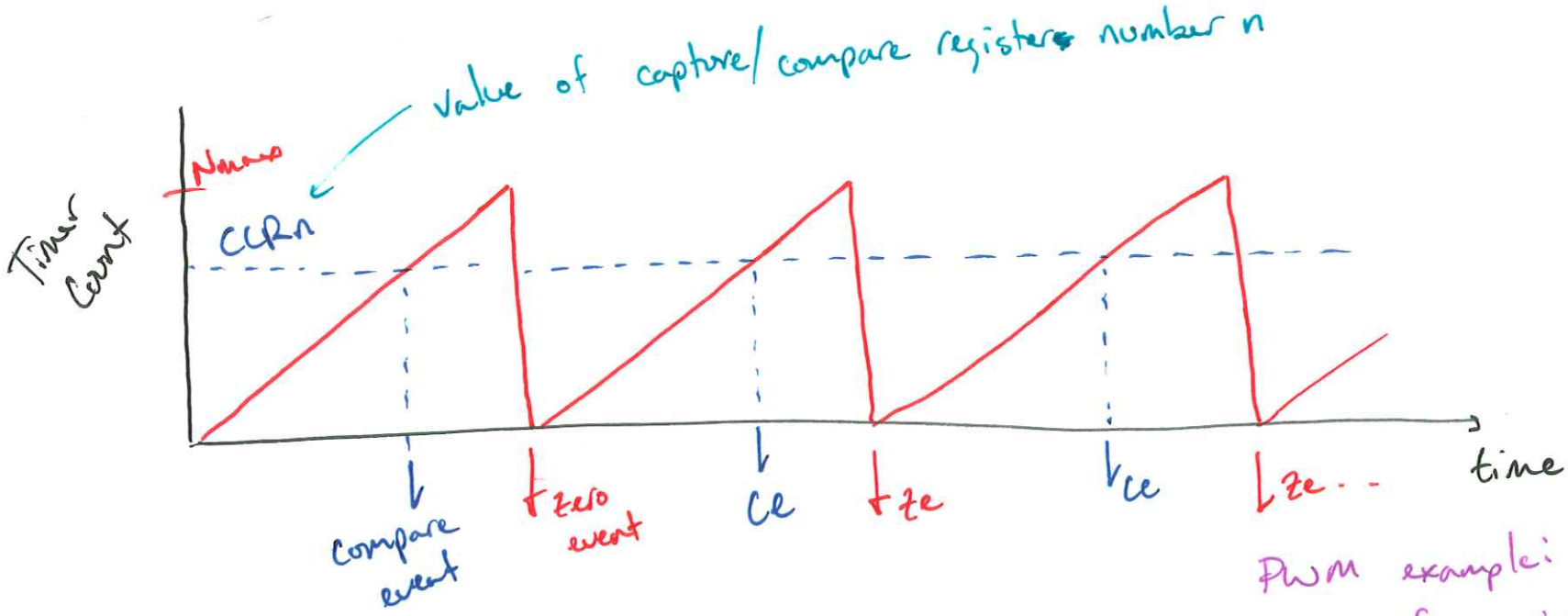
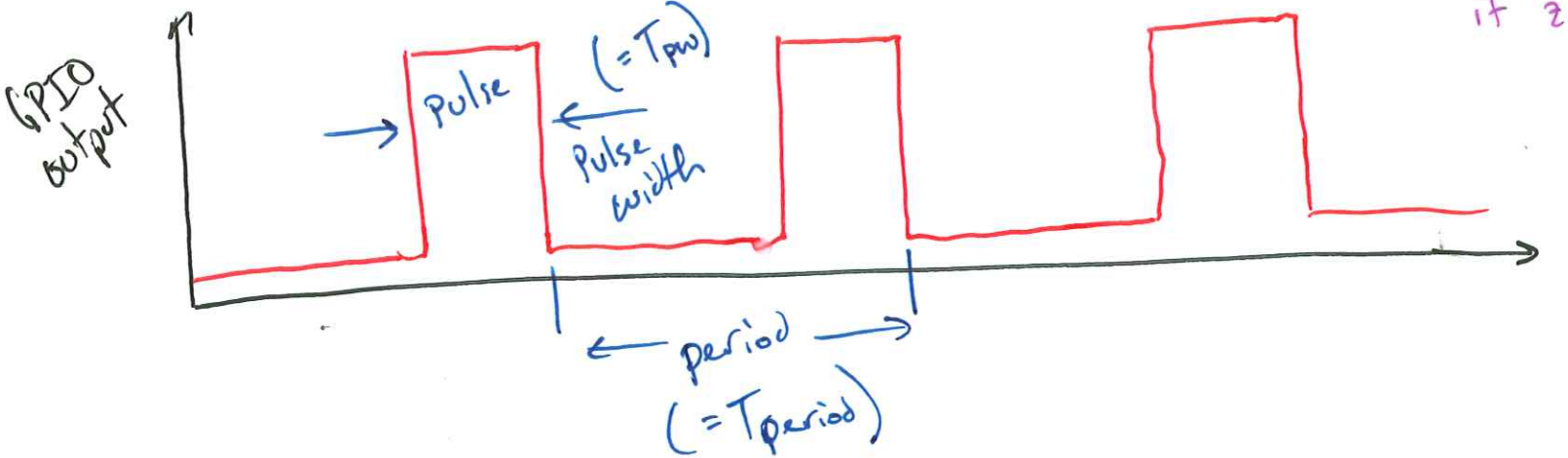
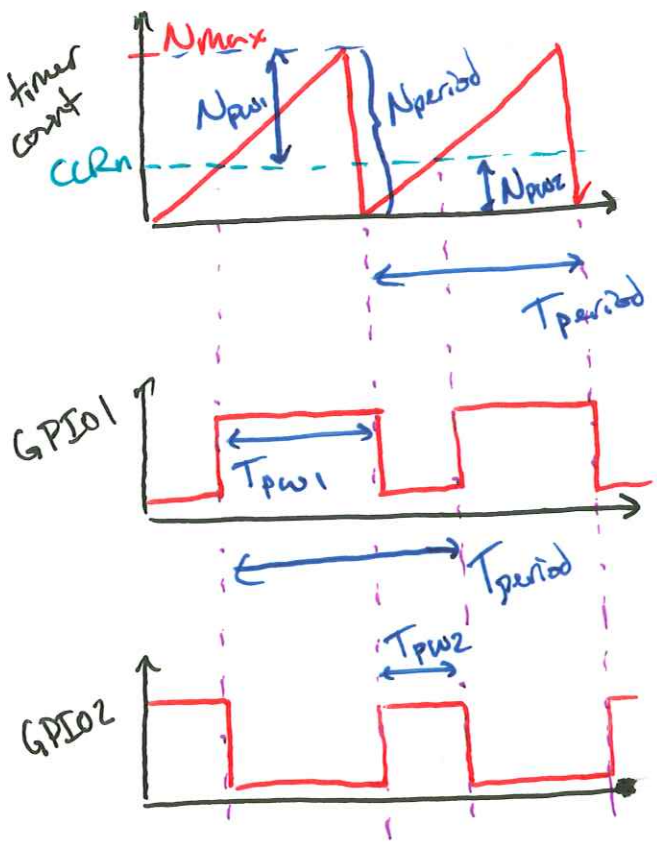


PWM example:
if ce: set pin high
if ze: set pin low



PWM Compare Math



Note:

$GPIO1 = !\ GPIO2$

$T_{period} = T_{PW1} + T_{PW2}$

known: $T_{TIMCLK} \rightarrow f_{TIMCLK} = 1/T_{TIMCLK}$

$T_{period} = T_{TIMCLK} N_{period}$

$N_{period} = N_{max} + 1$

$$\begin{cases} N_{PW1} = N_{period} - CCRn \\ T_{PW1} = T_{TIMCLK} N_{PW1} \end{cases}$$

$$\begin{cases} N_{PW2} = CCRn \\ T_{PW2} = T_{TIMCLK} N_{PW2} \end{cases}$$

Note: $T_{PW1}, T_{PW2} \leq T_{period}$

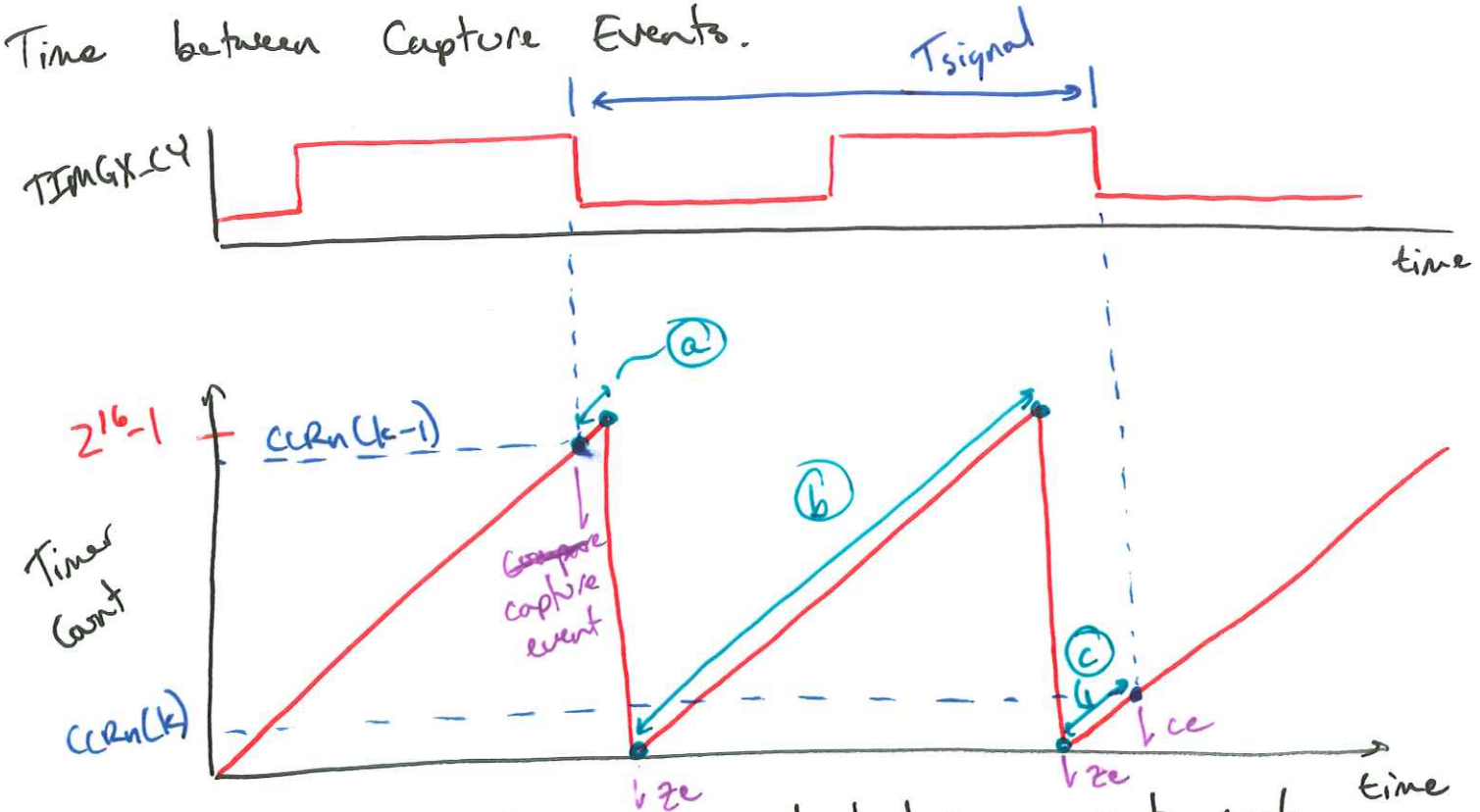
$N_{PW1}, N_{PW2} \leq N_{period}$

$$\text{Duty Cycle, } DC[\%] = \frac{\text{on time}}{\text{Total time}} \cdot 100\%$$

$$= \frac{T_{PW}}{T_{period}} \cdot 100\% = \frac{N_{PW}}{N_{period}} \cdot 100\%$$

DC capped to 0% – 100%

Time between Capture Events.



have: T_{TIMCLK}

$N_{period} = 2^{16}$

want: # of Timer counts between events such that: $T_{signal} = T_{TIMCLK} N_{counts}$

ⓐ : $(2^{16}) - (CCRn(k-1))$

ⓑ : 2^{16}

ⓒ : $CCRn(k)$

$N_{counts} = ⓐ + ⓑ + ⓒ = 2^{16} - CCRn(k-1) + 2^{16} + CCRn(k)$

$= CCRn(k) - CCRn(k-1) + 2 \cdot 2^{16}$

Generalized: $N_{counts} = CCRn(k) - CCRn(k-1) + N_{resets} \cdot 2^{16}$