

Exam 1 in 2 weeks 2/25, 10 AM - 11:50 AM Room TBA

Closed-Book, Closed Notes.

1 Crib sheet (front & back) PROVIDED - Also on webex

Bring Calculators!

Last semester Exam (to be) posted on webex.

for code:

Can shorthand code such that we still understand function/variable...  
intended for use.

Pseudocode is not accepted unless explicitly asked for.

Content:

Everything up to and including timers & interrupts.

Ex. 1

$$f_{\text{clock}} = 12 \text{ MHz}$$

$$N_{\text{DIV}} = 4$$

$$f_{\text{TIMCLK}} = 12 \text{ MHz} / 4 = 3 \text{ MHz}$$

$$T_{\text{TIMCLK}} = 1 / f_{\text{TIMCLK}} = 333 \text{ ns}$$

$$N_{\text{period}} = \frac{T_{\text{period}}}{T_{\text{TIMCLK}}} = 300 \text{ counts} \rightarrow N_{\text{max}} = N_{\text{period}} - 1 = 299$$

$\rightarrow$  • period = 299

interrupt:

- $\rightarrow$  Enable ZERO or LOAD event
- $\rightarrow$  Enable TIMG# interrupt
- $\rightarrow$  write function for it:

```
void TIMG#_IRQHandler(void) {  
     $\rightarrow$  Clear the event/interrupt flag.  
    resets++;  
}
```

$$A) \frac{500 \text{ ms}}{100 \mu\text{s}} = 5000 \text{ resets per } 500 \text{ ms}$$

```
resets = 0;  
while (resets < 5000);
```

Ex 1)  
A.i)

$$f_{\text{TIMERCLK}} = 12\text{MHz} / 64 = 187.5\text{kHz}$$

$$\text{period} = 50000 \rightarrow N_{\text{period}} = 50001$$

$$T_{\text{period}} = N_{\text{period}} / f_{\text{TIMERCLK}} = 2.67\text{s}$$

← way to large for 500ms delay.

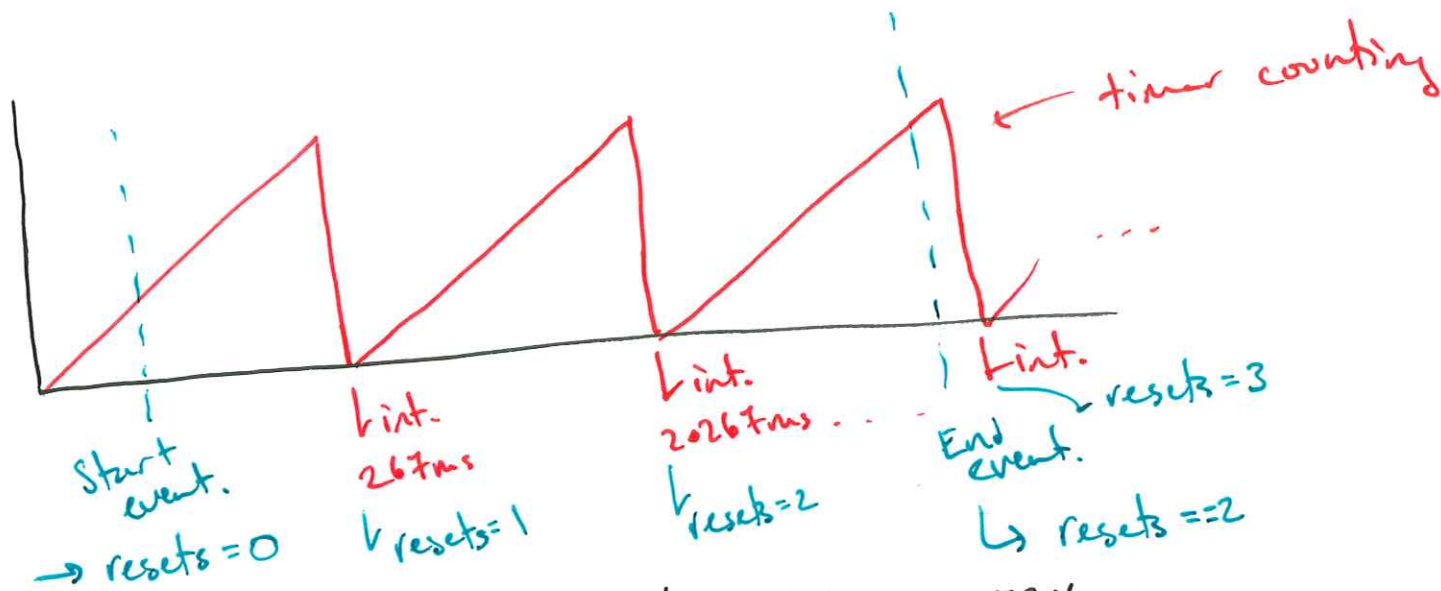
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$$\text{period} = 5000$$

$$\rightarrow T_{\text{period}} = 267\text{ms}$$

← can get rough 500ms program delay.

B.i)

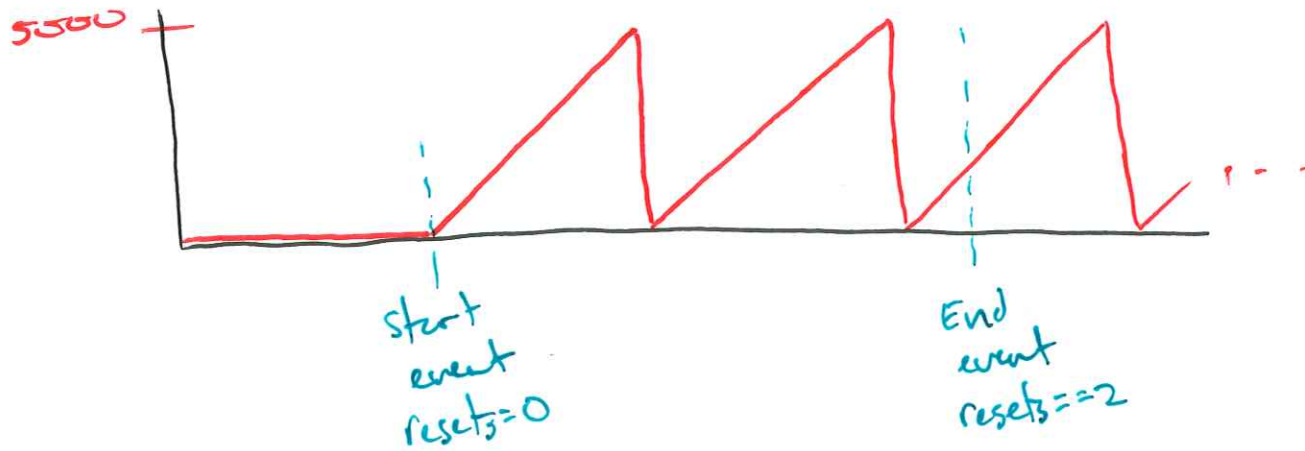


$$\text{Total time} = \text{resets} \cdot 267\text{ms} = 534\text{ms}$$

By diagram: Large error!

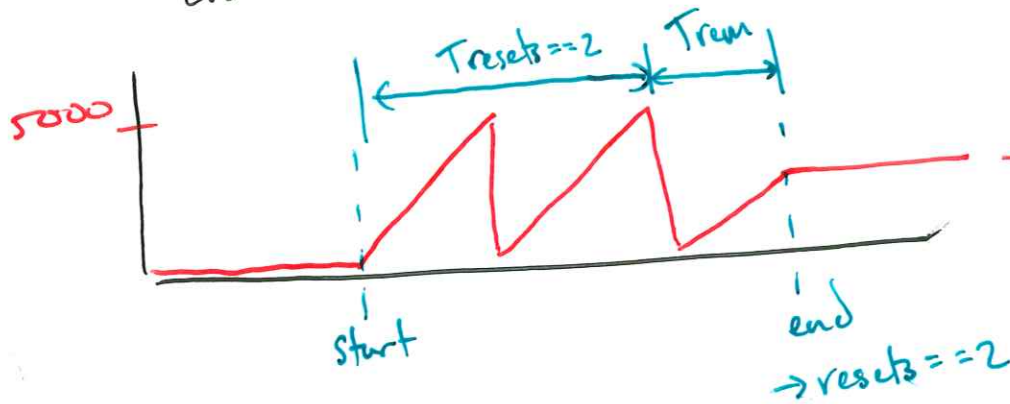
$$\text{Error} \pm 267\text{ms}.$$

Improve on Error a little bit:  
 Start timer at start event:



Reduced error to ~~approx~~  $0 \leq \text{error} \leq 26 \text{ fms}$

B ii | Improve on error a lot.  
 End timer at end event:



$T_{\text{event}} = T_{\text{resets}} + T_{\text{rem}}$   
 $T_{\text{rem}}$ : from value of timer counter.  
 → timer count reg.

$T_{\text{rem}} = \text{Timer count reg} \cdot T_{\text{inclk}}$

known easily as  $\text{resets} \cdot 26 \text{ fms}$ .

Ex 2

Smallest divider for  $T_{\text{period}} = 10\text{ms}$

$$f_{\text{CLK}} = 32\text{MHz}$$

Assume TIMER in up-mode

↳ 16-bit timer. → Max  $N_{\text{period}} = 65536 (=2^{16})$

with max possible counts, what is required  $N_{\text{div}}$ ?

$$T_{\text{period}} = 10\text{ms} = N_{\text{period}} \cdot T_{\text{TIMCLK}} \rightarrow T_{\text{TIMCLK}} = 152.6\text{ns}$$

$$\rightarrow f_{\text{TIMCLK}} = 6.55\text{MHz}$$

$$f_{\text{TIMCLK}} = f_{\text{CLK}} / N_{\text{div}} \rightarrow N_{\text{div}} = 4.883$$

$N_{\text{div}}$  must be an integer! Must Round UP

$$N_{\text{div}} = 5$$

$$\rightarrow f_{\text{TIMCLK}} = 6.4\text{MHz} \rightarrow T_{\text{TIMCLK}} = 156.3\text{ns}$$

$$T_{\text{period}} = 10\text{ms} = N_{\text{period}} \cdot 156.3\text{ns}$$

$$\rightarrow N_{\text{period}} = 64000 \rightarrow \text{period} = 63999$$

$$\text{Resolution} = T_{\text{TIMCLK}} = 156.3\text{ns.}$$