ENGR-2300

Electronic Instrumentation

Quiz 3

Spring 2025

Solution

Print: Name _____ **RIN** _____

Section _____

I have read, understood, and abided by the Collaboration and Academic Dishonesty statement in the course syllabus. The work presented here was solely performed by me.

Signature: _____

Date: _____

On all questions: SHOW ALL WORK. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS. No credit will be given for numbers that appear without justification. Unless otherwise stated in a problem, provide 3 significant digits in answers. Read the entire quiz before answering any questions. Also, it may be easier to answer parts of questions out of order.

1. Comparators and Schmitt Triggers. (20 points)

A. Following circuit in Fig. 1 is built to compare the response of the two OP amp applications from the identical signal source with high frequency noise. Both applications have the same reference voltage of 1V . Vin1 is the main signal with 3V amplitude and Vin2 is representing a noise with higher frequency. Assume that LTC6752 is a typical OP amp which needs +- 5V power input.

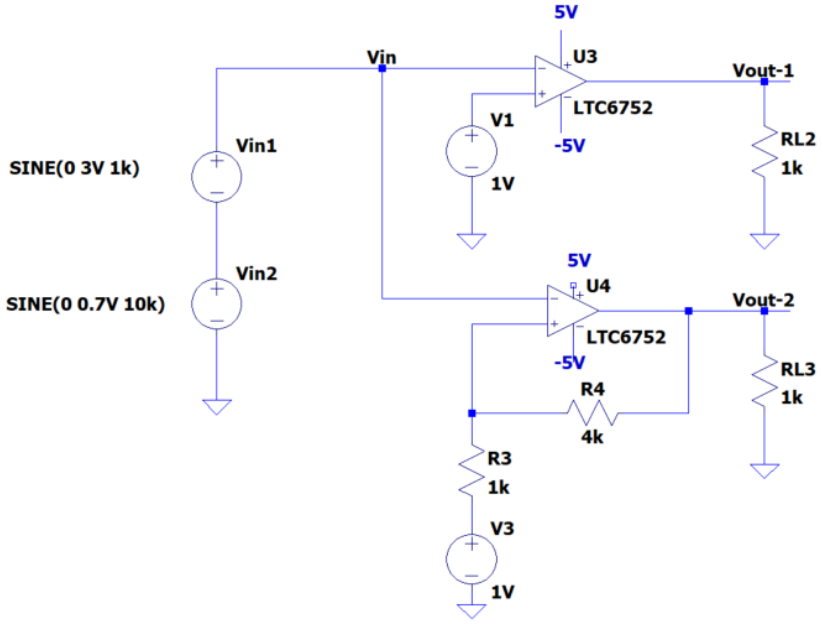


Fig. 1

1. Identify the name or the function of the upper part of OP amp application for the output, Vout-1 ? [1 pts]

Comparator (or inverting comparator)

2. Identify the name or the function of the lower part of OP amp application for the output, Vout-2 ? [1pts]

Schmitt Trigger

3. Calculate two trigger voltages for the Vout-2 application. [5 pts]

$$V_{T1} = (5V - 1V) \cdot \frac{1K}{1K + 4K} + 1V = \boxed{1.8V}$$

$$V_{T2} = (-5V - 1V) \cdot \frac{1K}{1K + 4K} + 1V = \boxed{-0.2V}$$

4. Sketch the Vout-1 waveform on the graph given in Fig.2. Give clear annotations for the key crossing points. You can ignore the initial state of the input cycle: Draw the waveform from the second cycle. [5 pts]

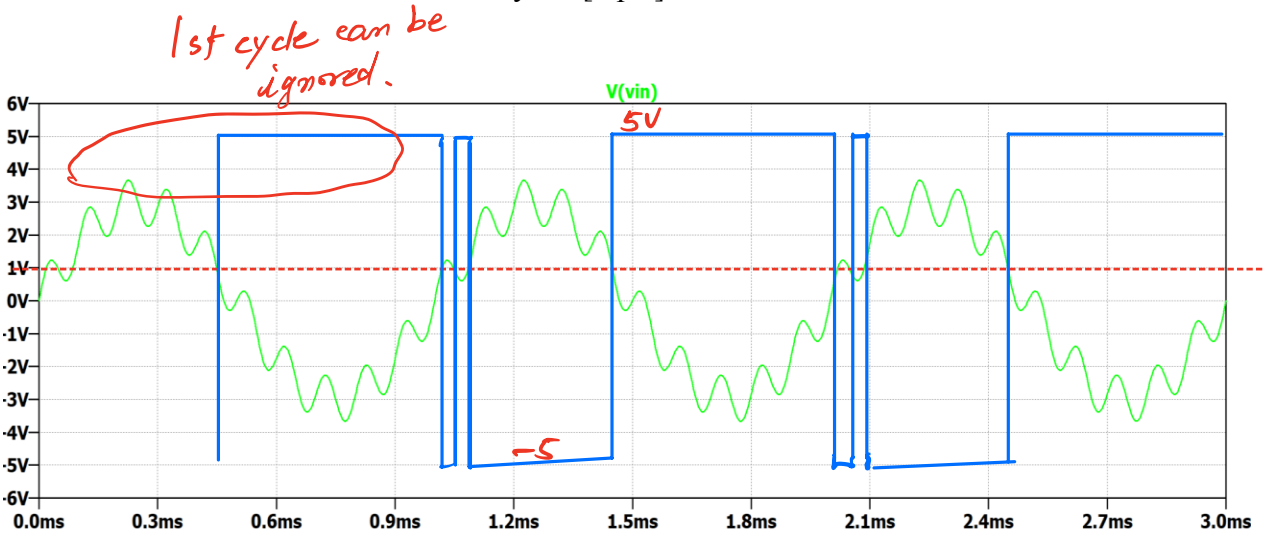


Fig.2

5. Sketch the Vout-2 on the graph given in Fig.3. Give clear annotations for the key crossing points. You can ignore the initial state of the input cycle: Draw the waveform from the second cycle. [5 pts]

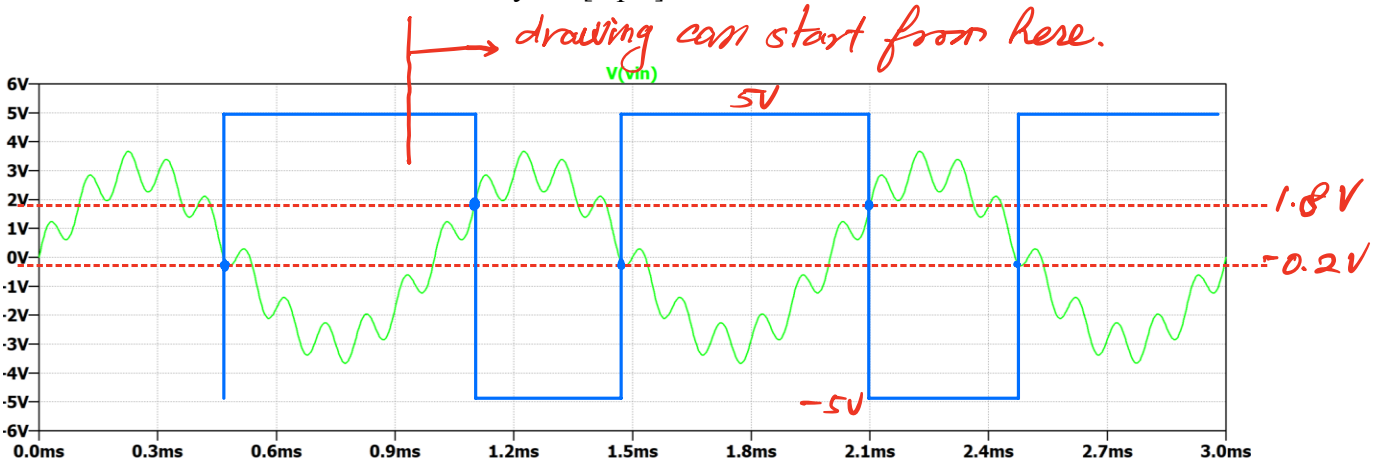


Fig.3

6. Describe the advantage of the circuit operation leading to Vout-2 compared to the other one to Vout-1? [2 pts]

Vout-2. (Schmitt Trigger) is less vulnerable to the presence of noise.

7. If you disconnect the feedback loop from Vout-2, which is R4 (4kΩ), i.e. if you remove the R4, what would be the results on Vout-1 and Vout-2. Evaluate the following statement: "Both outputs of Vout-1 and Vout-2 will be identical". [1pts]

A: [TRUE] B: [FALSE]

No positive feedback ⇒ just a comparator

2. Digital Logic Circuits: Combinational and Sequential Logic. (20 points)

A. Consider the combinational logic circuit below.

1. Give a Boolean logic expression to represent what is happening at points P1, P2, and Q. [2 pts]

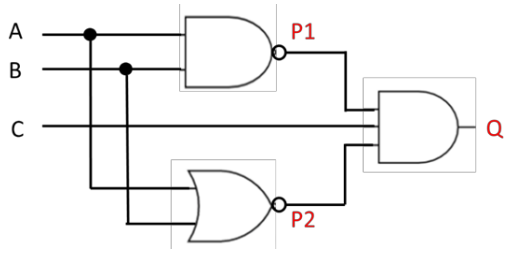


Fig. 4

P1: $\overline{A \cdot B}$

P2: $\overline{A+B}$

Q: $P1 \cdot P2 \cdot C$ or $\overline{A \cdot B} \cdot \overline{A+B} \cdot C$

2. Fill in the truth table below for P1, P2 and Q. [3 pts]

C	A	B	P1	P2	Q
0	0	0	1	1	0
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	1	0	0
1	1	0	1	0	0
1	1	1	0	0	0

B.

1. The timing diagram of the JK Flip-flop is shown below in Fig.5. Assume that CLR bar is held high for the run (meaning that CLR is not activated.) Also assume that this flip-flop changes state on the *falling edge* of the clock. The shaded area in the beginning of the run is the unknown state. Sketch the timing diagram of Q and Q-bar on the appropriate lines of the plot. [4 pts]

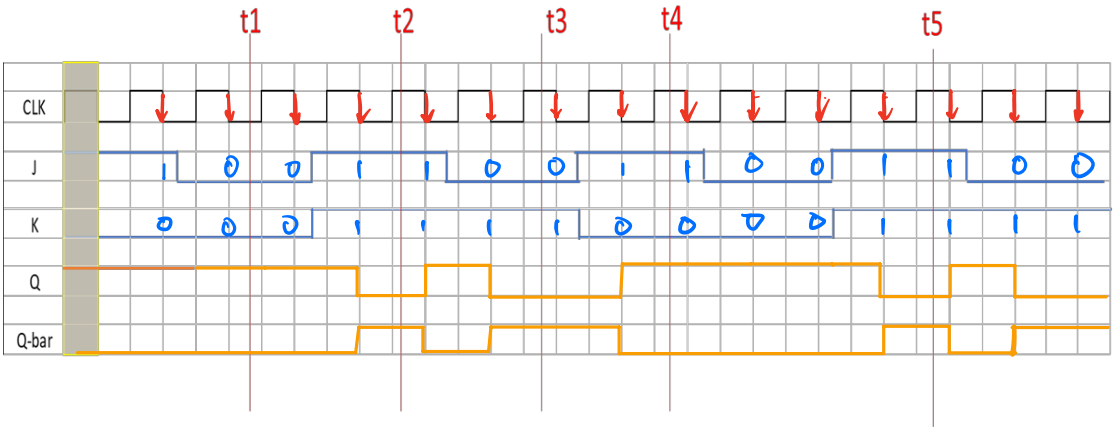


Fig. 5

2. Fill out the table below for J, K, Q and Q-bar at the times t1-t5. [2 pts]

Time	J	K	Q	Q-bar
t1	0	0	1	0
t2	1	1	0	1
t3	0	1	0	1
t4	1	0	1	0
t5	1	1	0	1

C. The following question is about a Transistor-Transistor-Logic (TTL) circuit.

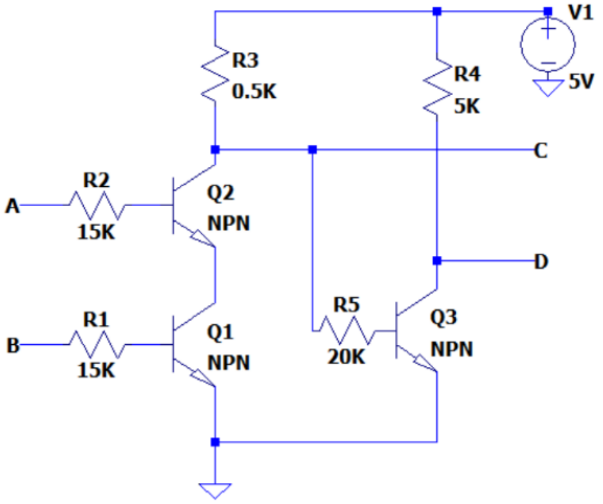


Fig. 6

1. Assume that the circuit above is well tuned such that three transistors (Q1,Q2 and Q3) are turned OFF and ON by the input voltage changes: 0V (LOW) and 2.5V(HIGH). Complete the following table using logic levels of 0 and 1. [2pts]

A	B	C	D
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

$C = \overline{A \cdot B}$, NAND

$D = \overline{C}$. NOT.

or

$= A \cdot B$, AND.

2. Based on the results of the truth table, what type of gate does the output C represent? How about the output D? [2pts]

D. The following circuit is a 5-bit counter.

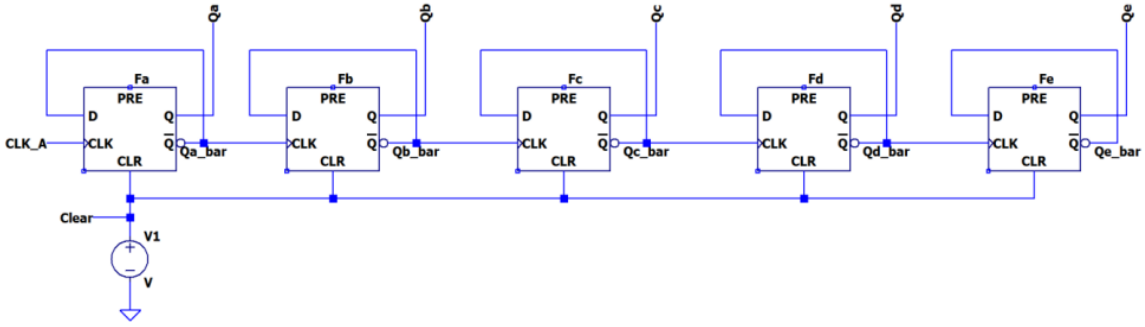


Fig. 7

The table below shows the starting states of the 5-bit counter. Fill the table for each state after running another 6 clock cycles. In decimal notation, what is the number that is being represented by the counter after 6 clock cycles? [5 pts]

	Qe	Qd	Qc	Qb	Qa
Current state	0	1	1	0	0
State after 6 cycles	1	0	0	1	0

Decimal #.

$2^4 + 2^1 = 18$

0 1 1 0 0 → 1
0 1 1 0 1 → 2
0 1 1 1 0 → 3
0 1 1 1 1 → 4
1 0 0 0 0 → 5
1 0 0 0 1 → 6
1 0 0 1 0

3. The 555 Timer Circuit Application and Analysis (20 points)

Fig. 8 shows a 555-Timer configured as an astable multivibrator; i.e. an oscillator. Basically, the frequency, and ON & OFF time of the pulses are controlled by external resisters: R1 and R2, and a capacitor C1.

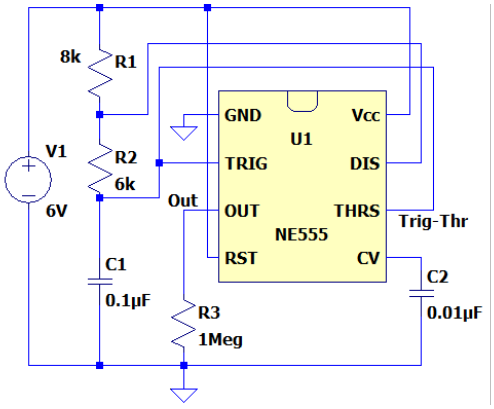


Fig. 8

A. Calculate the time duration for T_high and T_low. Also, calculate the frequency of the output. [3 pts]

T_high : $T_H = 0.693\,(R_1 + R_2)\,C_1 = 0.693\,(14k)\cdot(0.1\mu F)$

$= \boxed{0.97\ ms}$

T_low: $T_L = 0.693\,(R_2)\cdot C_1 = 0.693\,(6K)\cdot(0.1\mu F)$

$= \boxed{0.42\ ms}$

Frequency: $f = \dfrac{1.44}{(R_1 + 2R_2)\cdot C_1} = \dfrac{1.44}{(8K + 2\cdot 6k)(0.1\mu F)}$

$= \boxed{720\ Hz}$

B. Calculate the duty cycle of the output of the 555 timer. [3 pts]

$\text{Duty cycle} = \dfrac{T_H}{T_H + T_L}\cdot 100\,\%$

$= \dfrac{0.97\ ms}{(0.97 + 0.42)\ ms}\cdot 100 = \boxed{69.8\,\%}$

OR. $D = \dfrac{R_1 + R_2}{R_1 + 2R_2}\cdot 100\,\% = \dfrac{8k + 6k}{8k + 12k}\cdot 100 = \boxed{70\,\%}$

C. Fig. 9 below shows the output waveform measured at the pin: 'Trig-Thr' in the timer circuit diagram in Fig.8.

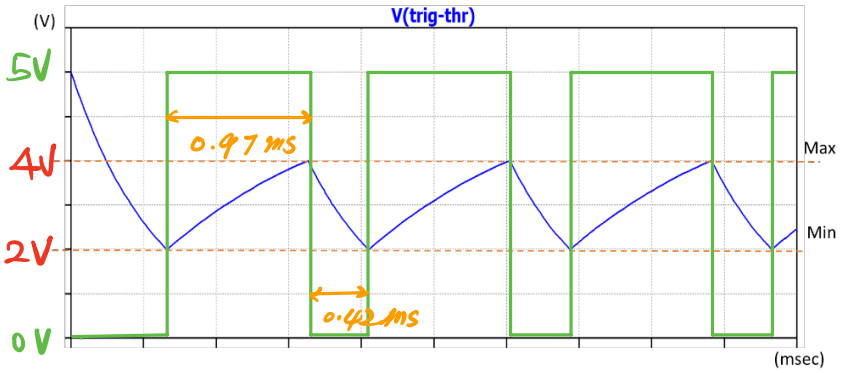


Fig. 9

1. What are the min and max of the waveform indicated on the graph above? Put the number on the Y-axis of voltage. [3 pts]

max: $V_{cc} \cdot \frac{2}{3} = 6 \cdot \frac{2}{3} = 4\,V$

min: $V_{cc} \cdot \frac{1}{3} = 6 \cdot \frac{1}{3} = 2\,V$

2. Using the calculated results from question A and B above, draw the output voltage on the graph in Fig.9. Label all relevant voltages levels, and time duration of 'HIGH" and "LOW" time. [6 pts]

see graph above.

3. For a given C1=0.1uF and R2=6kΩ , calculate the value of R1 to design a timer circuit with a duty cycle of 50%? [5 pts]

$$D = \frac{T_H}{T_H + T_L} = \frac{0.693\,(R_1 + R_2)\cdot C1}{0.693\,(R_1 + 2R_2)\cdot C1}$$

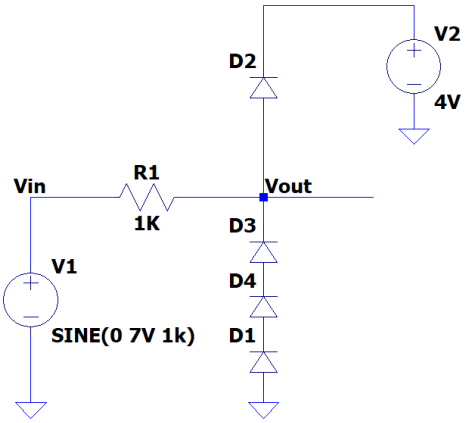
$$= \frac{R_1 + R_2}{R_1 + 2R_2} = 0.5 \quad (50\%)$$

$$2R_1 + 2R_2 = R_1 + 2R_2$$

$$R_1 = 2R_1 \quad . \quad \boxed{R_1 = 0}\ \Omega$$

4. Diode Rectifier, Limiter circuits (20 points)

A. Following diode circuit is a diode limiter for input protection. Given the sinusoidal input with 7V amplitude, and all diodes having 0.7V forward bias voltage, draw the output waveform on the graph in Fig. 11. [5 pts]



V_{in}^{+} limit $= 0.7\,V + 4\,V$
$= 4.7\,V$

V_{in}^{-} limit $= (0.7) \cdot 3 = 2.1\,V$

Fig. 10

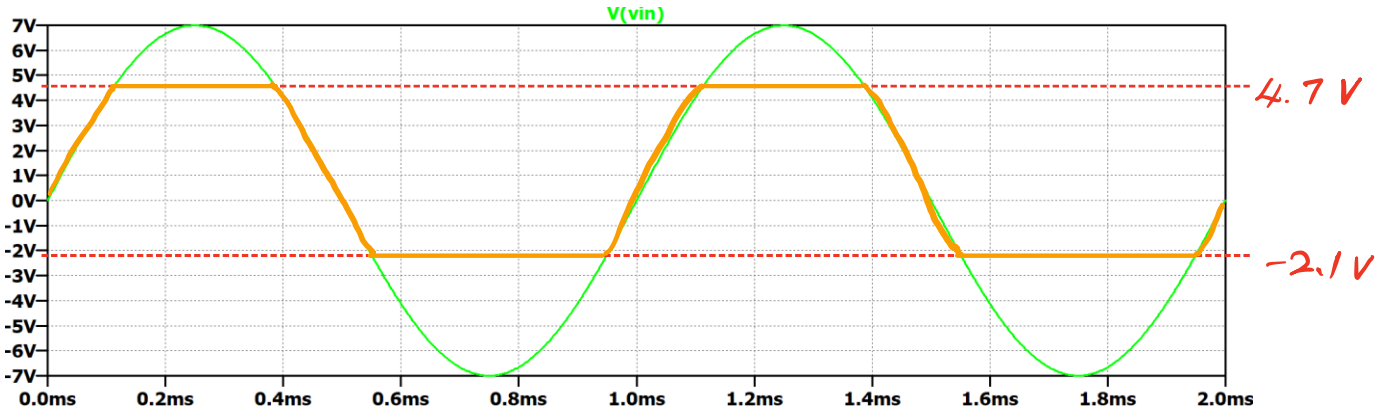


Fig. 11

B. In the following circuit, D1 is a Zener diode with a breakdown voltage of 4.2V. For different cases of V1, fill in the following tables for the current through the diode (ID), through R2 (IR2), and related power consumptions. [7 pts]

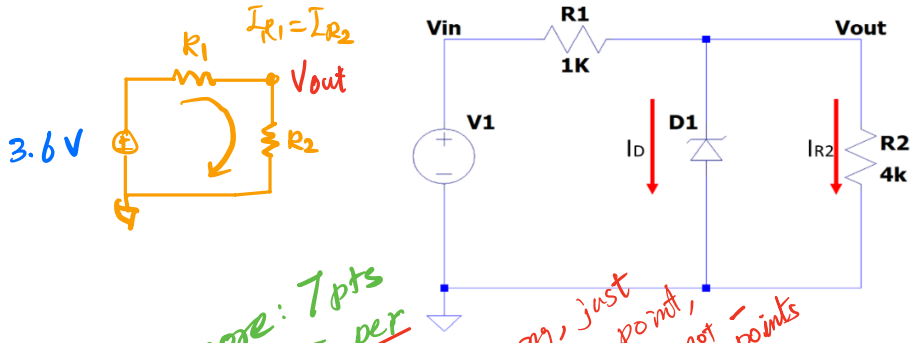


Fig. 12

V1 (V)	Vout (V)	ID (mA)	IR2 (mA)	Power consumption by D1 (mW)	Power consumption by R2 (mW)
3.6 V	2.88	0	0.72	0	2.07
7.0 V	4.2	1.75	1.05	7.35	4.41
10.0 V	4.2	4.75	1.05	19.95	4.41

Fig. 13

C. Fig. 14 shows a full rectifier circuit with a 10V amplitude sinusoidal input and 2kΩ source resistance (Rs). Diodes from D1 to D6 are all Silicon made with Vth=0.7V.

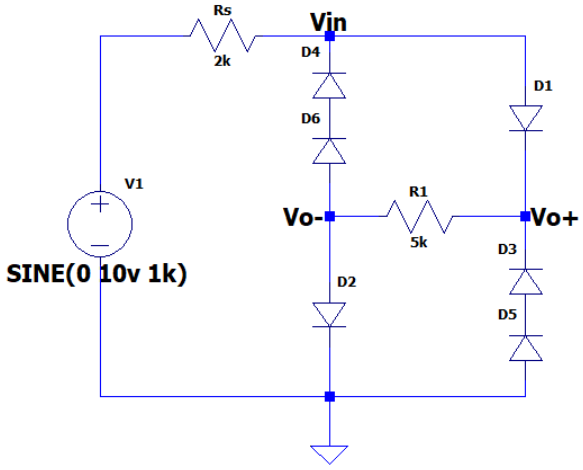


Fig. 14

TAs: just check the gaps from each max. & (1.4V & 2.8V) thanks!

1. Sketch the Vout waveform across R1 in the graph shown in Fig.15. Give clear annotation on the key points illustrating the rectifying function of the circuit. [3 pts]

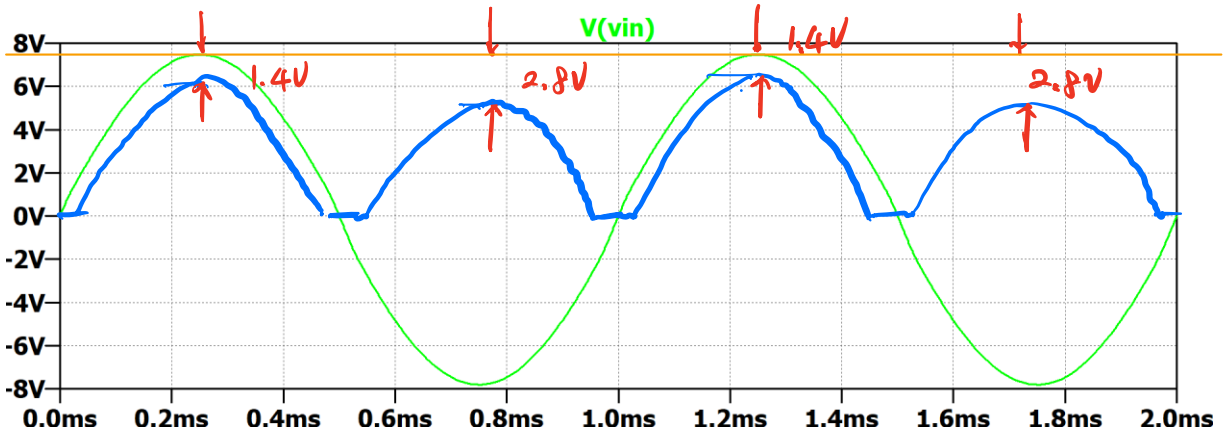


Fig. 15

2. Draw a path of the reverse current (negative part of sinusoidal) on the Fig. 16 with arrows along the diodes and resistors. [2 pts]

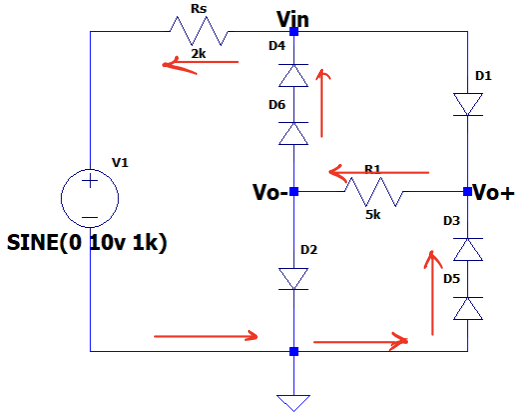


Fig. 16

3. Calculate the peak current through R1 and calculate the power dissipation from that. Peak current means the biggest current flow of the two different paths. [3 pts]

peak current is when forward bias is applied. (only 2 diodes drops)

$$I_{R1} = \frac{10V - 1.4V}{R_s + R_1} = \frac{8.6V}{7k} = 1.228\ mA$$

$$P_{R1} = I^2 \cdot R_1 = (1.228)^2 \cdot 5k = \boxed{7.55\ mW}$$