ENGR-2300

Electronic Instrumentation

Quiz 3

Fall 2019

Name _____

Section ___

Question 1 (20 Points) _____

Question 2 (20 Points) _____

Question 3 (20 Points) _____

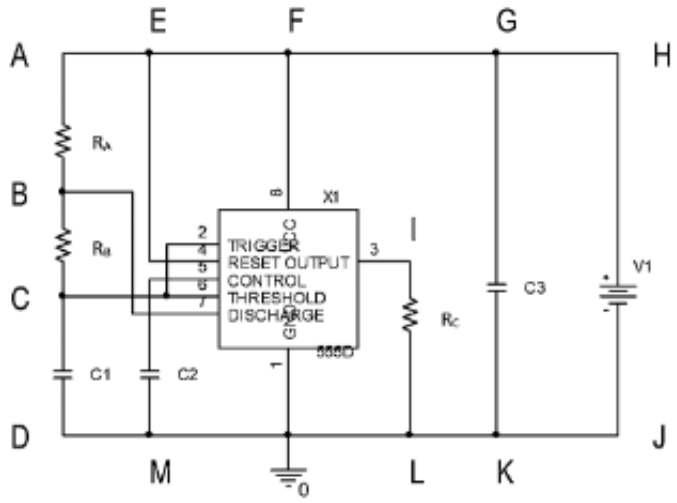
Question 4 (20 Points) _____

LMS Question is worth an additional 20pts

Total (80 points) _____

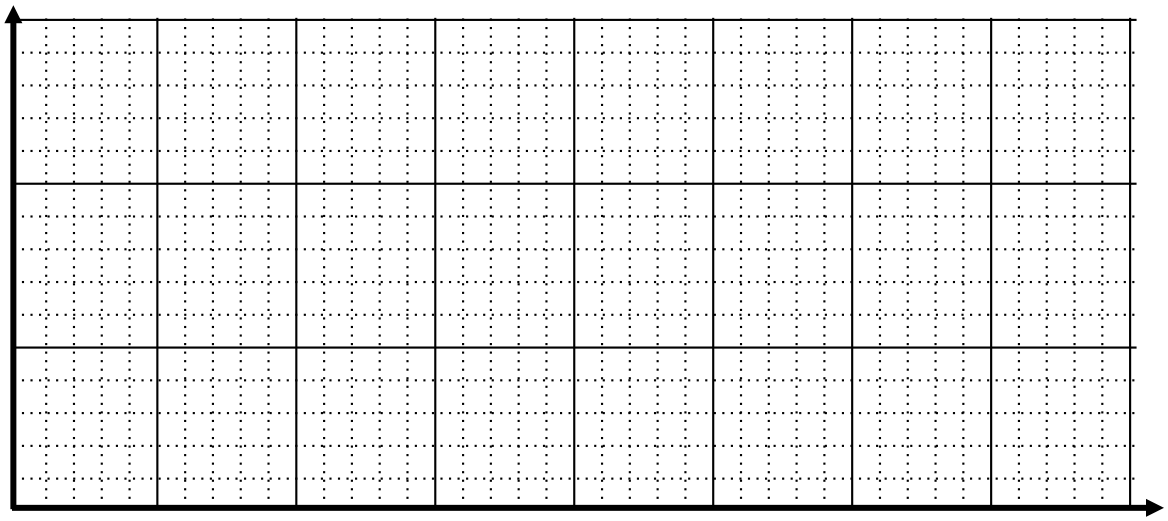
On all questions: **SHOW ALL WORK**. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS. No credit will be given for answers that appear without justification. Read the entire quiz before answering any questions. Also it may be easier to answer parts of questions out of order.

Question 1 (20 Points) Astable Multivibrator (An Iconic 555 Timer Application)



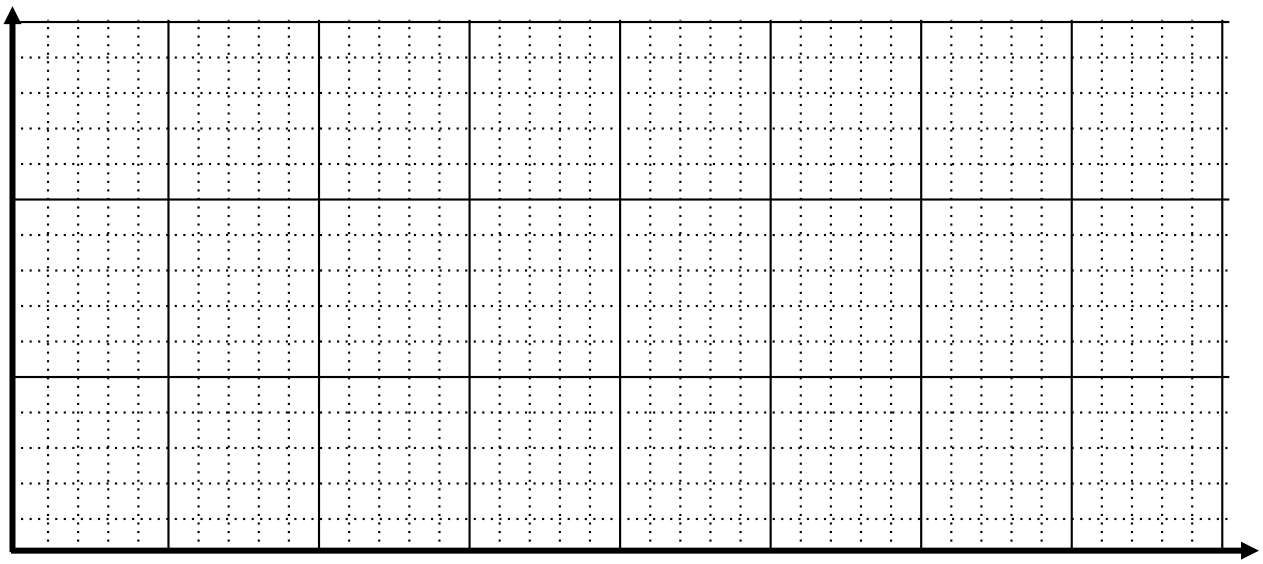
a. A 555 timer, astable multivibrator is built as above with $R_A = 10k\Omega$, $R_B = 9.1k\Omega$, $R_C = 40k\Omega$, C1 = 0.1μF, C2 = 0.01μF, C3 = 330μF, and V1 = 9V. Determine the **on time** (T1) and the **off time** (T2) for this circuit. (4 Pts)

b. Plot the output voltage (**I**) below, showing at least two full cycles, starting with the output voltage at its maximum (assume = 9V). Label the horizontal and vertical scales. (4 Pts)

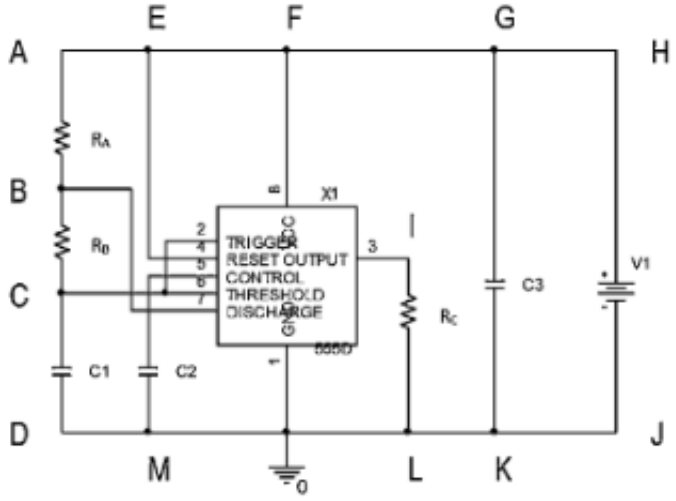


c. Determine the maximum and minimum voltages at pins 6 (C) and 7 (B). Assume that the circuit is in steady state. You may want to look at the background information provided in the crib sheet.(4 Pts)

d. Plot at least two cycles of the voltage at pins 6 & 7. Label the vertical and horizontal scales. (4 Pts)



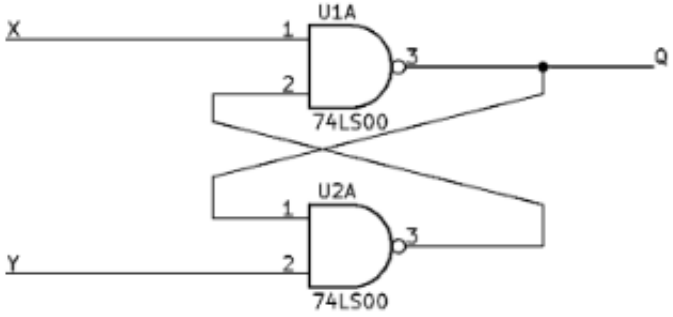
This is the same figure as part a.



e. Modify the circuit to achieve a 90% duty cycle. You are only allowed to change only one resistor and no other components. The frequency is allowed to change. Which resistor do you change and what is the new value? (4 Pts)
Values for Part a. were: $R_A = 10k\Omega$, $R_B = 9.1k\Omega$, $R_C = 40k\Omega$, C1 = 0.1µF, C2 = 0.01µF, C3 = 330µF, and V1 = 9V.

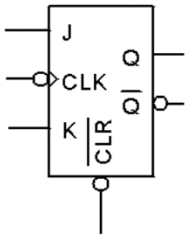
Question 2 (20 Points) Combinational & Sequential Logic Circuits

a. (4 points) Determine the truth table for the following circuit. *Note that you have to do two cases, one where Q begins at 0 and one where it begins at 1.*



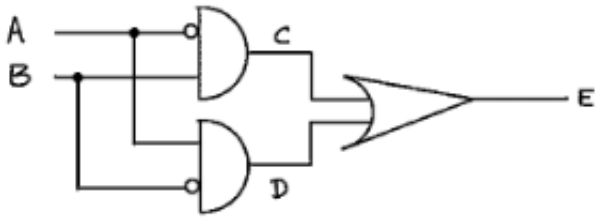
Q Before	X	Y	Work space	Q After
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

b. (4 points) The desired output of a negative edge triggered JK flip flop after the pulse is Q = 0 and Qbar = 1. How can this be achieved? List all possible input conditions for this to happen, i.e. what should be done with J, K, clock, and clear inputs. You are given that the outputs before pulse are Q = 1 and Qbar = 0.



c. (2 points) Given A = Logic '1', E = ?

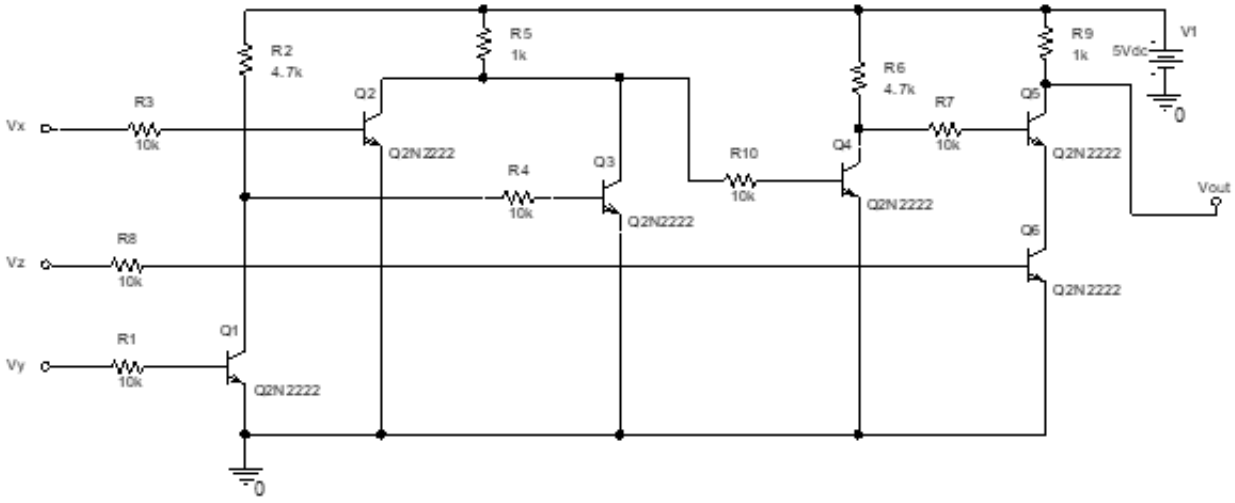
Note: Bubble indicates inversion!



Circle the correct answer.

i) Logic '0'
ii) Logic '1'
iii) C
iv) B
v) D
vi) $\overline{B}$
vii) A.B
viii) A + B

d. (10 points) The circuit below consists of a npn transistor network that implements a logic function between three input variables X, Y, and Z. The binary variables X, Y, and Z are represented using voltages Vx, Vy, and Vz respectively. Vout represents the output voltage of the network for corresponding binary output variable OUT.



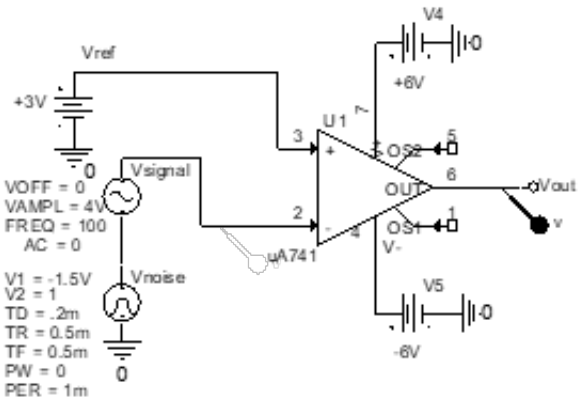
i) (6 points) Draw the logic diagram for the above circuit. Use logic gate symbols and show how the inputs X, Y, Z are related to output OUT. For this you need to identify how transistors, and serial/parallel connections of transistors, can be used to implement logic functions.

ii) (4 points) Fill the truth table below based on the logic diagram derived in previous part, or directly from the given transistor network.

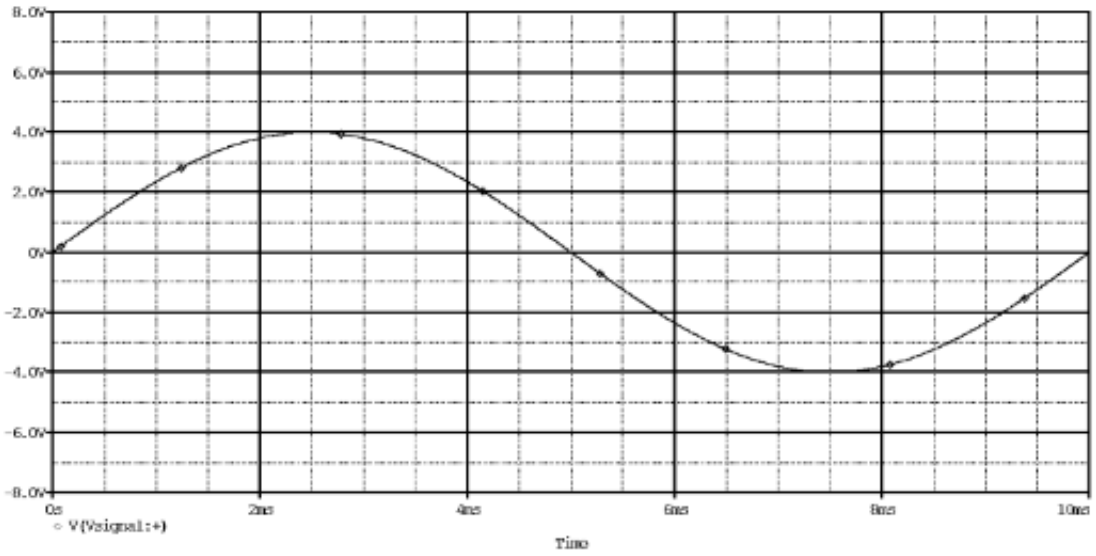
X	Y	Z	OUT
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Question 3 (20 Points) Schmitt Trigger

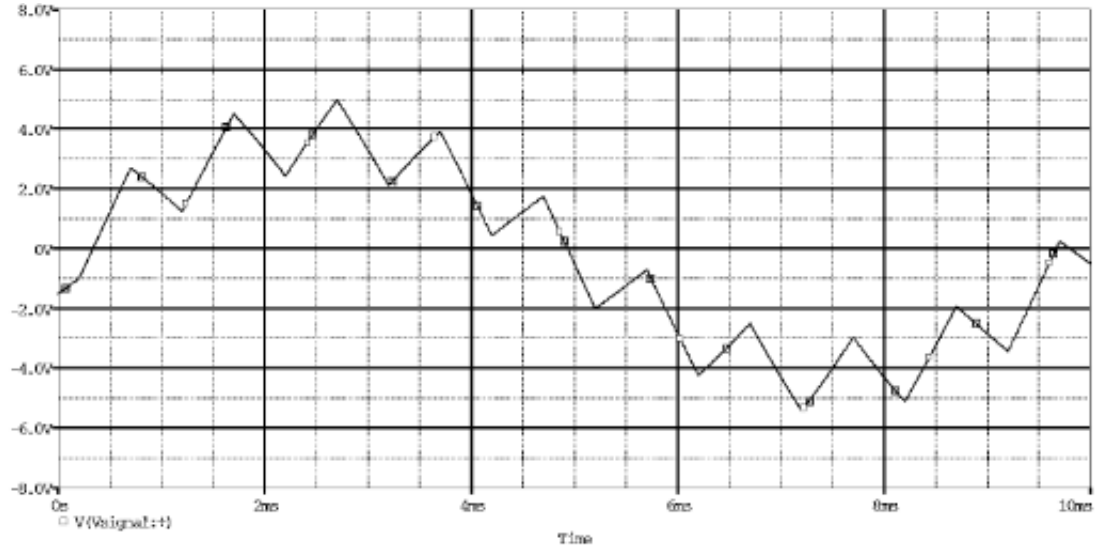
In this problem, we investigate the same properties of Schmitt Triggers we did in Experiment 6. Assume the output of the op-amps is capable of reaching the power supply voltages, +6V and -6V in this example.



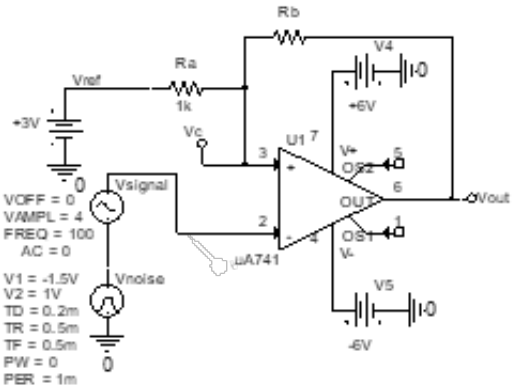
a. For the circuit shown the input signal, Vsignal is compared to Vref. For this part there isn't any noise. Vnoise amplitude is 0V. The plot below has the Vsignal (without noise).
On this plot, draw Vout. Label the plot as you would for an experiment report. (4pts)



b. Same circuit but now a triangle shaped noise has corrupted the signal. Again plot Vout. Label as is done for report. (4pts)



c. This is now the same circuit but configured as a Schmitt Trigger. Vc is the voltage at the non-inverting input of the op amp. Ra=1kΩ. The goal here is to determine values of Rb that will eliminate false output transitions caused by the noise signal.



What is the maximum value of Vout? (1pt) _____

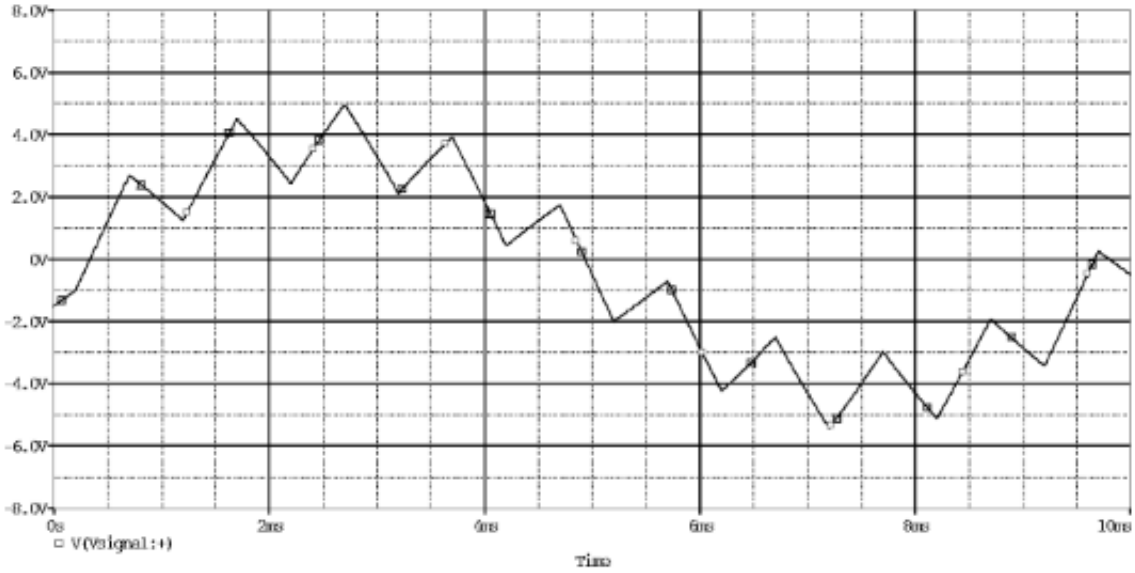
What is the minimum value of Vout? (1pt)_____

Complete the table below, ***use the figure in part d to help fill in the final column:*** **(6pts)**

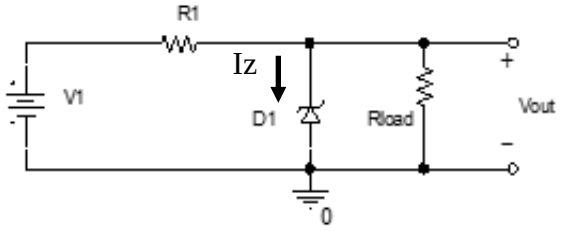
Rb(Ω)	Vc if Vout = max	Vc if Vout = min	Eliminates false pulses (Y on N)
5k			
14k			

d. Below is the same figure as shown in part b. **Now plot Vout and Vc for the Schmitt trigger circuit if Rb =5k.**

Label the plot as is done for the reports. (4pts)



Question 4 (20 Points) Diode Circuits

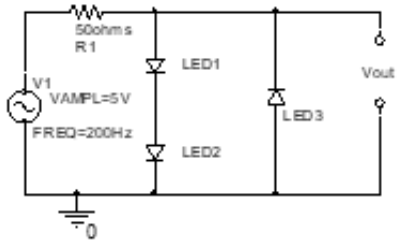


a. (6pts) In the circuit shown:
V1=15V
R1=200Ω
Rload=600Ω

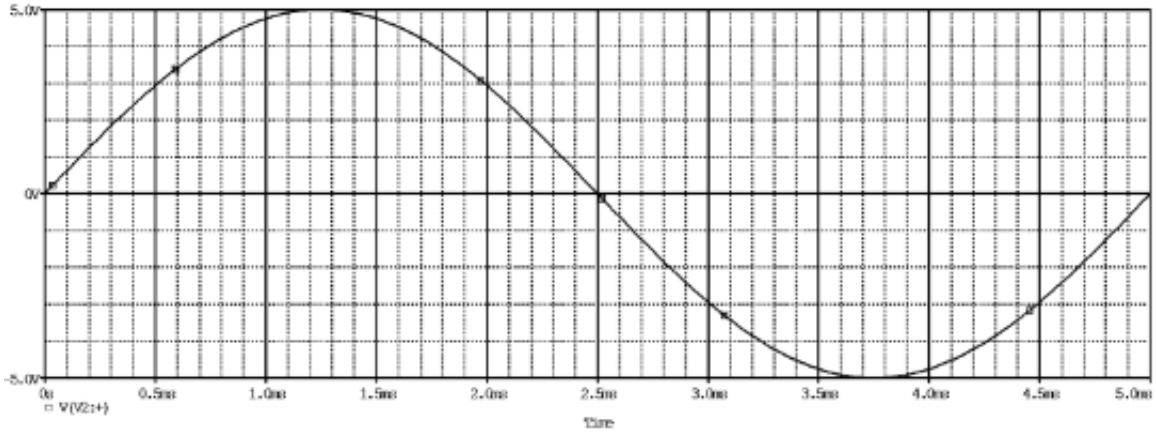
D1 is a Zener. Two different Zener diodes are tried with this circuit. Determine Vout, Iz (the current in the Zener), I_{R1} (the current in R1) and the power loss in the Zener for each case. Use the "Some Additional Background" information provided in the crib sheets. (6pts)

Zener part number	Vout	Iz	I_{R1}	Power loss in Zener
1N749A				
1N759A				

b. The circuit shown is a type of Limiter circuit but it uses LEDs rather than diodes for the limiting. ***Refer to "Additional Background"***



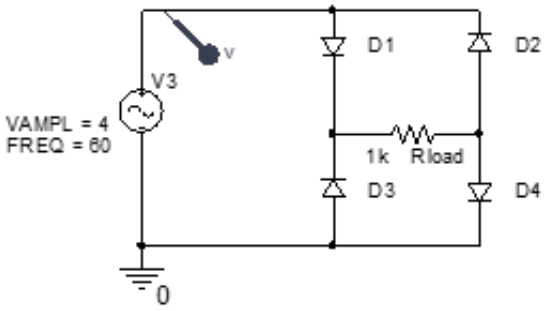
i. (3pts) Sketch and label Vout on the plot. V1 is already plotted.
LED1 is an Pure Green LED (555 nm)
LED2 is a Super Red LED (633 nm)
LED3 is an Ultra Blue LED (430 nm)

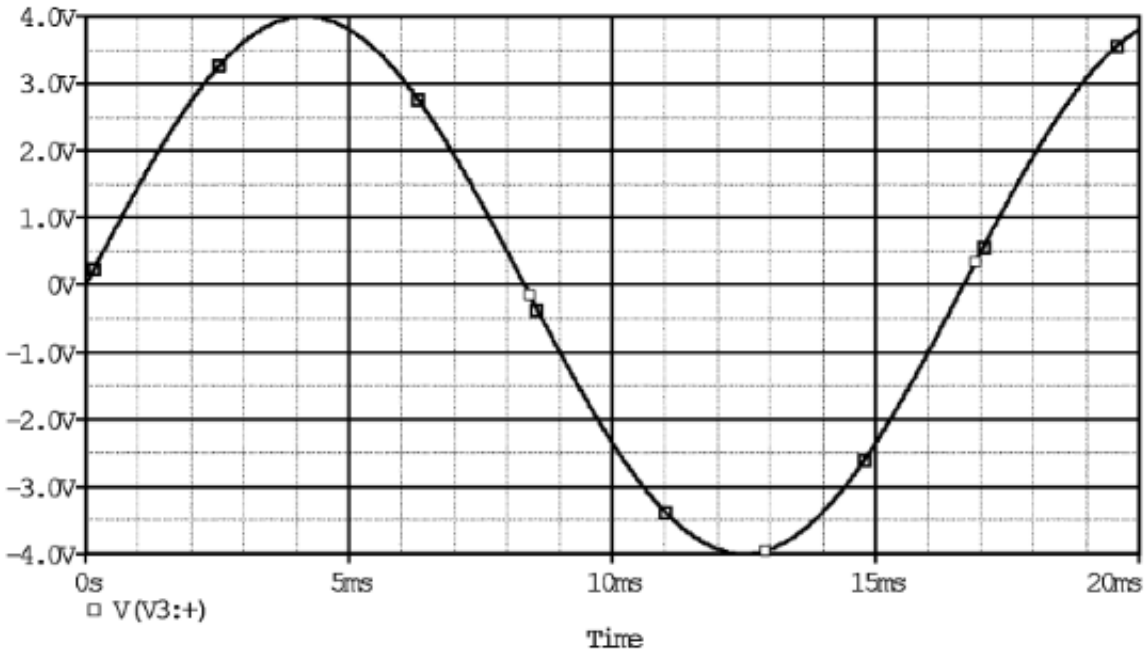


ii. (1pt)What is the peak current through LED1?

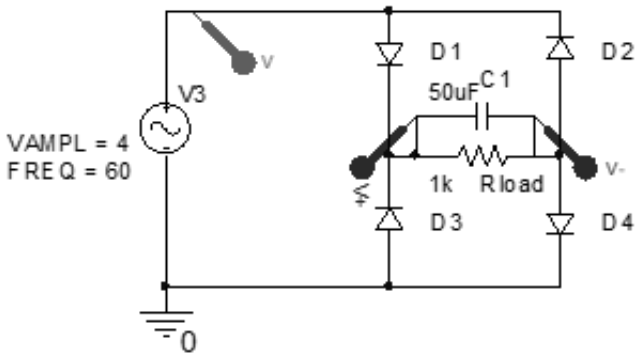
iii. (1pt)What is the peak current through LED2?

c. Rectifier diodes: The voltage across Rload is the output voltage. The plot shows the input voltage. Plot the output voltage using the Von diode model of a 4148 diode. Label important voltages including the peak output voltage. (3pts)





d. A filter capacitor has been added to the circuit in part c. **The plot for part c may be helpful.**



i. What is the time between peaks of the output voltage? (1pts)

ii. At the time of the peak output voltage, **what is the current in Rload**, (the load resistance)? Rload = 1kΩ (1pt)

iii. Immediately after when the voltage peak the diodes will turn off. All of the current in R1 at this time must be supplied by C1. If C1=50uF, what is the dV/dt for the capacitor at this time? The Crib Sheet for Quiz 1 may be useful. (2pts)

iv. Do a crude estimate of the ripple voltage by assuming that the dV/dt (part iii) is constant for a time equal to the time between voltage peaks (part i). (1pts)

e. Do you expect to take the optional final? Your answer here is NON-BINDING. (1pt)

The optional final will:

- cover all topics in the class,
- generally be more difficult than the quizzes
- Not have an LMS portion,
- replace your lowest quiz grade, which includes the LMS portion,

NOT replace your lowest quiz grade, IF the final grade is the lowest. i.e. you cannot hurt you overall grade by attempting the final.

Yes No