ENGR-2300

Electronic Instrumentation

Quiz 3

Spring 2018

Name: _____**Solution**_____

Please write you name on each page

Section: 1 or 2

4 Questions Sets, 20 Points Each
LMS Portion, 20 Points

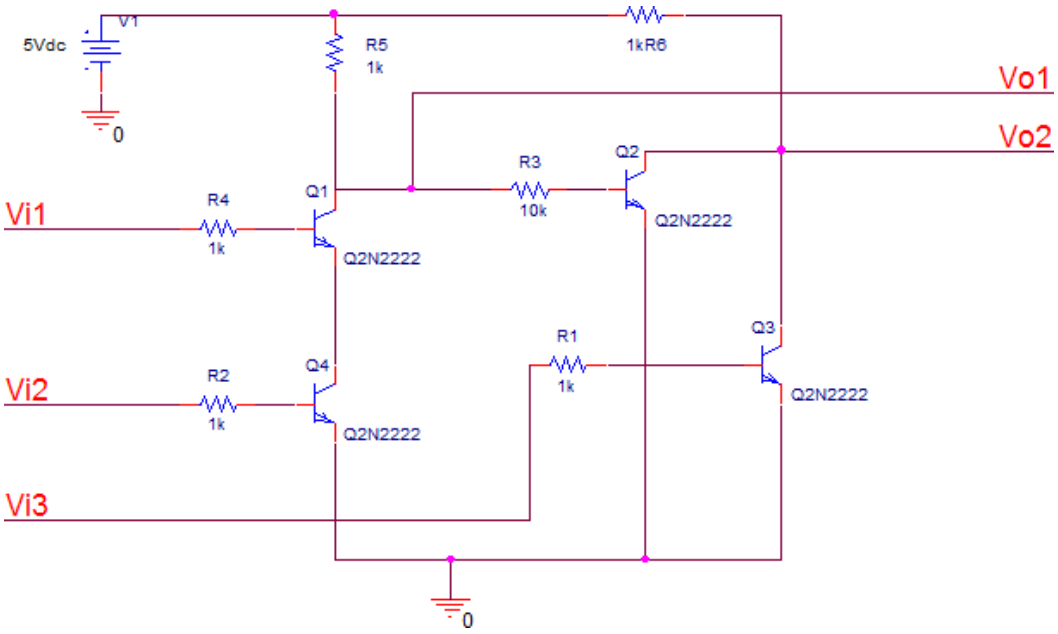
Question Set 1)	Logic Circuits
Question Set 2)	555 Timers
Question Set 3)	Miscellaneous
Question Set 4)	Design Problem

On all questions: **SHOW ALL WORK. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS.** No credit will be given for numbers that appear without justification. Unless otherwise stated in a problem, provide 3 significant digits in answers. It may be easier to answer parts of questions out of order.

DO NOT WRITE ON THE BACK OF PAGES. If you need extra room, make it clear in the main problem statement that work is continuing somewhere else, then use the FRONT SIDE of the additional blank page(s) provided at the end of the exam.

Question Set 1. Logic Circuits

1.1 (8 pnts) The circuit below shows the construction of a custom logic gate using transistors and resistors. There are three inputs: Vi1, Vi2, and Vi3, and two outputs: Vo1 and Vo2. This logic gate follows the standards for TTL circuits, where input voltages of less than 0.8V are considered LOW and greater than 2V are considered HIGH, and for outputs, <0.4 V is LOW and >2.7 V is HIGH. Complete the logic table listed below.



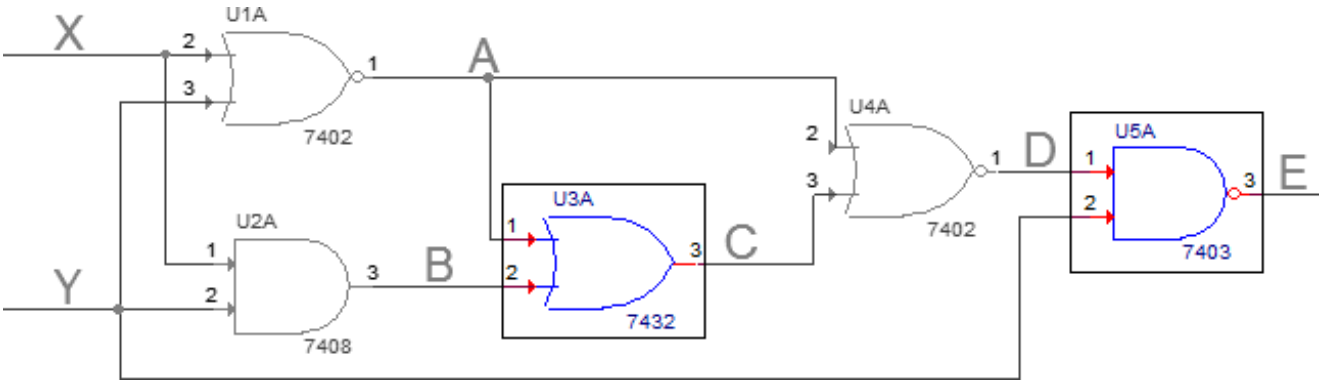
Vi1	Vi2	Vi3	Vo1	Vo2
0	0	0	**1**	**0**
0	0	1	**1**	**0**
0	1	0	**1**	**0**
0	1	1	**1**	**0**
1	0	0	**1**	**0**
1	0	1	**1**	**0**
1	1	0	**0**	**1**
1	1	1	**0**	**0**

1.2 (4 pnts) This is, of course, a 3-input gate with two types of outputs. What effective logic gates are represented by Vo1 and Vo2?

Vo1 Vi1 NAND Vi2

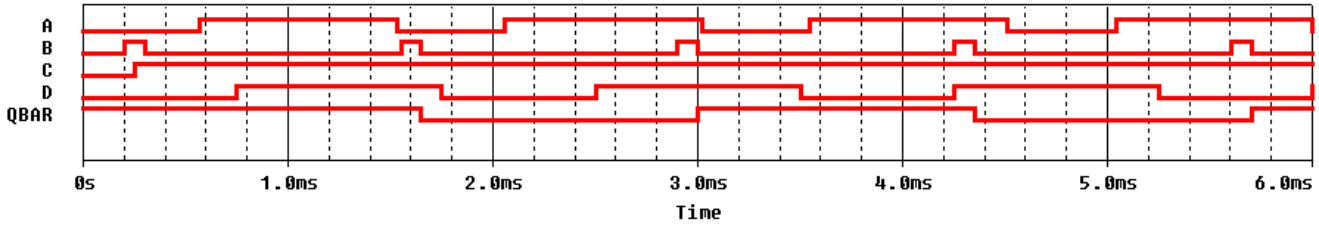
Vo2 Vi3 NOR Vo2

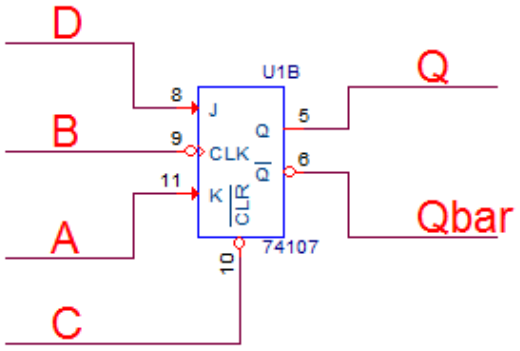
1.3 (4 pnts) Fill in all missing components or blanks in the circuit and truth table below. For the missing components, write in either the type of LOGIC GATE (e.g., AND, NOR, NAND) or draw the symbol for the logic gate; both will be accepted. You do not need to do both.



X	Y	A (X NOR Y)	B (X AND Y)	C (X OR Y)	D (C NOR A)	E (D NAND Y)
0	0	**1**	**0**	1	**0**	1
0	1	**0**	**0**	0	**1**	0
1	0	**0**	**0**	0	**1**	1
1	1	**0**	**1**	1	**0**	1

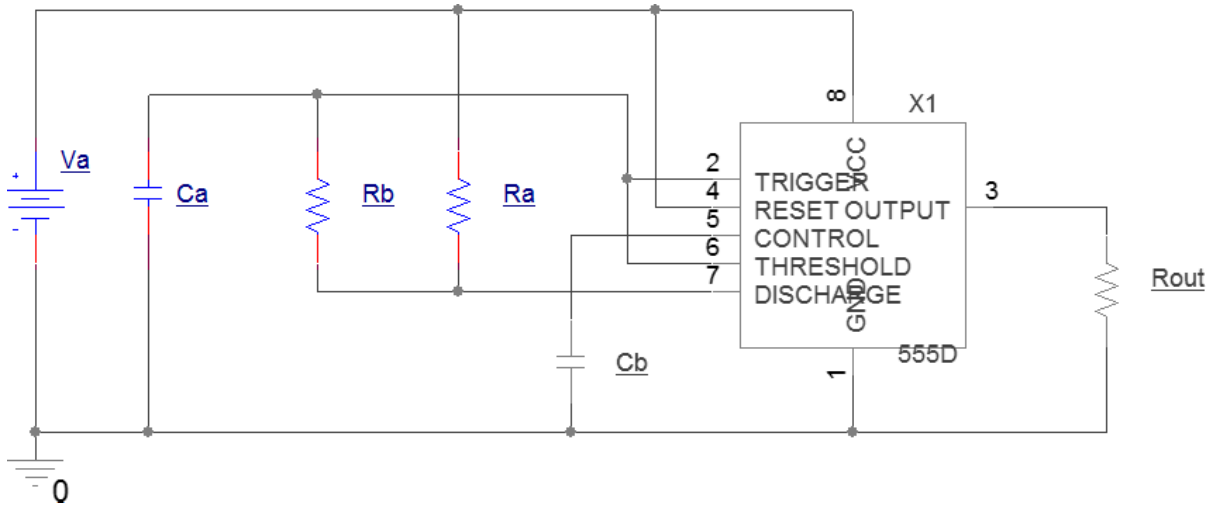
1.4 (4 pnts) The following graph shows the measurements of pins of a JK flip flop. Knowing the output, QBAR (not Q!), label the flip flop device pins below such that the correct signal (A, B, C, and D) is connected to the proper pin.





Question Set 2. 555 Timers

2.1 (4 pnts) Several components are missing from the 555 circuit given below which are needed to configure it as an astable multivibrator. Draw in the missing components and label them using letter subscripts (e.g., R_a, R_b, R_c, C_a, C_b, C_c, etc.)

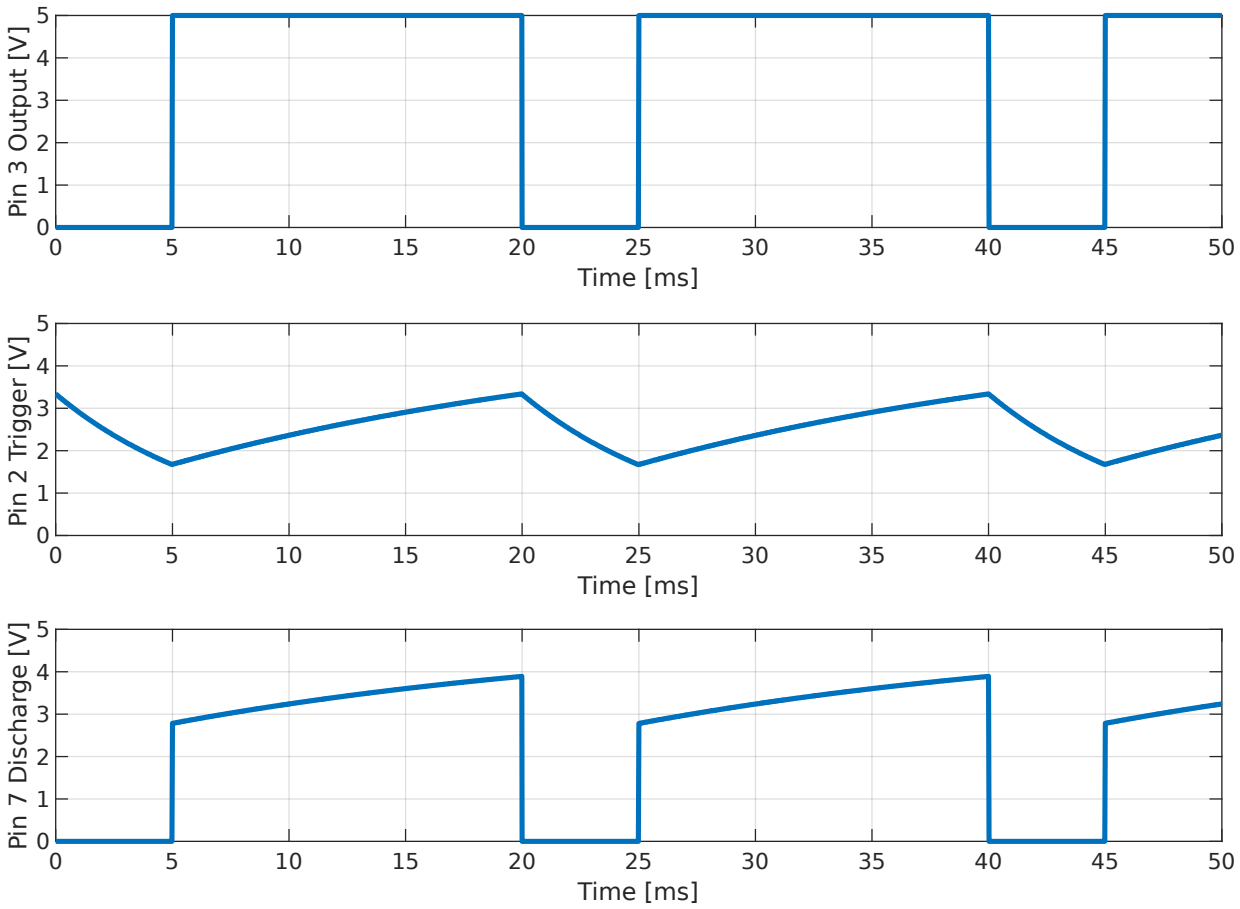


2.2 (4 pnts) Using the labels defined in 2.1, write the equations for the frequency and duty cycle of the output of the circuit above.

$$f = \frac{1.44}{(R_a + 2 * R_b)C_a}$$

$$D = 100\frac{T1}{T1 + T2} \qquad D = 100\frac{R_a + R_b}{R_a + 2R_b}$$

2.3 (6 pnts) The component values are selected such that the DC supply is 5 V, and the output of the circuit is 50 Hz and has a 75 % duty cycle. In the three grids below, draw the output signal (pin 3), trigger signal (pin 2) and discharge signal (pin 7) assuming that the 555 has reached steady state and at time = 0s the output signal just transitioned to LOW. NOTE: For any signal that requires a calculation: a rough approximation is fine (i.e., educated guess of the value).



2.4 (4 pnts) If the capacitor size is doubled, what is the resulting frequency of the output signal?

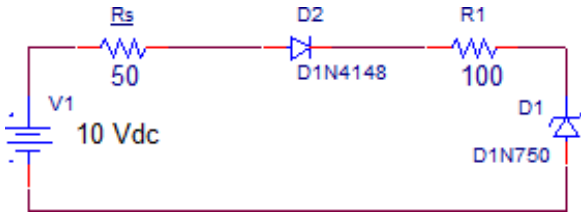
f_orig/2 = 25 Hz

2.5 (2 pnts) Using the configuration in 2.3, if the DC supply was changed from 5 V to 10 V, what output characteristics will change, qualitatively?

The output amplitude will increase (essentially double). Nothing else will change.

Question Set 3. Miscellaneous (Diodes, Rectifiers, Comparators, and Schmitt Triggers)

3.1 (8 pnts) Calculate the Voltage drop across **R1** for each of the circuits given below. Do NOT use the ideal diode model.

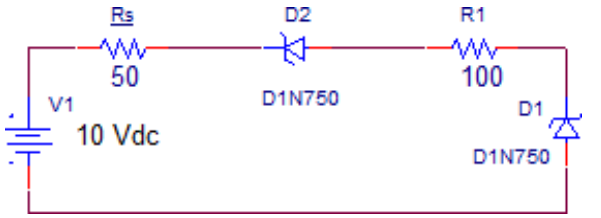


$V_1 = V_{R_s} + V_{D_2} + V_{R_1} + V_{D_1} = 10\text{V}$

$V_{R_s} + V_{R_1} = 10\text{V} - 4.7\text{V} - 0.7\text{V} = 4.6\text{V}$

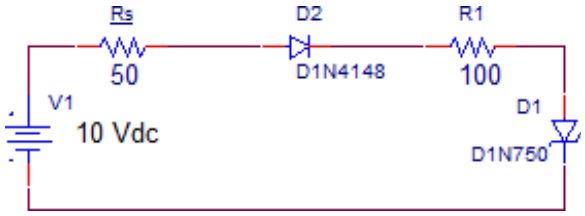
$$V_{R_1} = (V_{R_s} + V_{R_1}) \frac{R_1}{R_s + R_1}$$

V_{R1} **3.07 V**



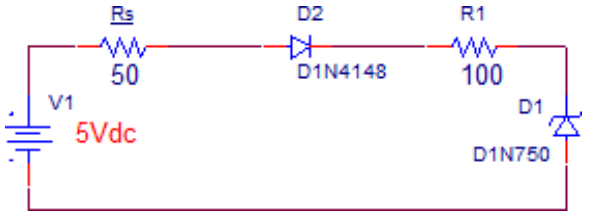
$V_{R_s} + V_{R_1} = 10\text{V} - 4.7\text{V} - 4.7\text{V} = 0.6\text{V}$

V_{R1} **0.40 V**



$V_{R_s} + V_{R_1} = 10\text{V} - 0.7\text{V} - 0.7\text{V} = 8.6\text{V}$

V_{R1} **5.73 V**

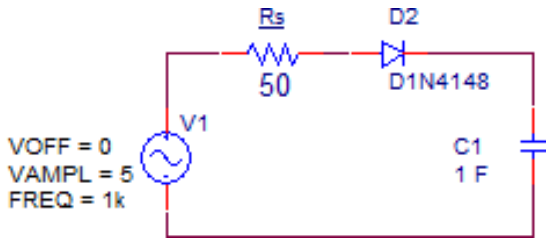


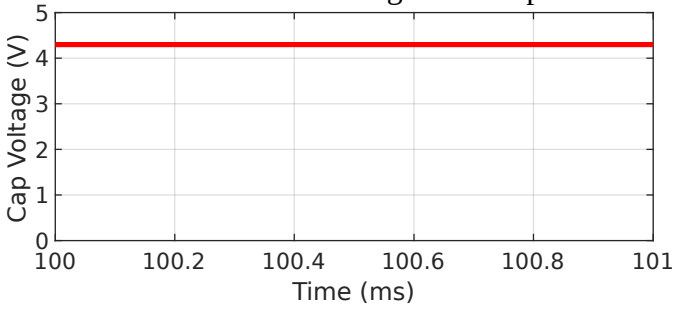
$V_{R_s} + V_{R_1} = 5\text{V} - 4.7\text{V} - 0.7\text{V} = -0.4\text{V}$

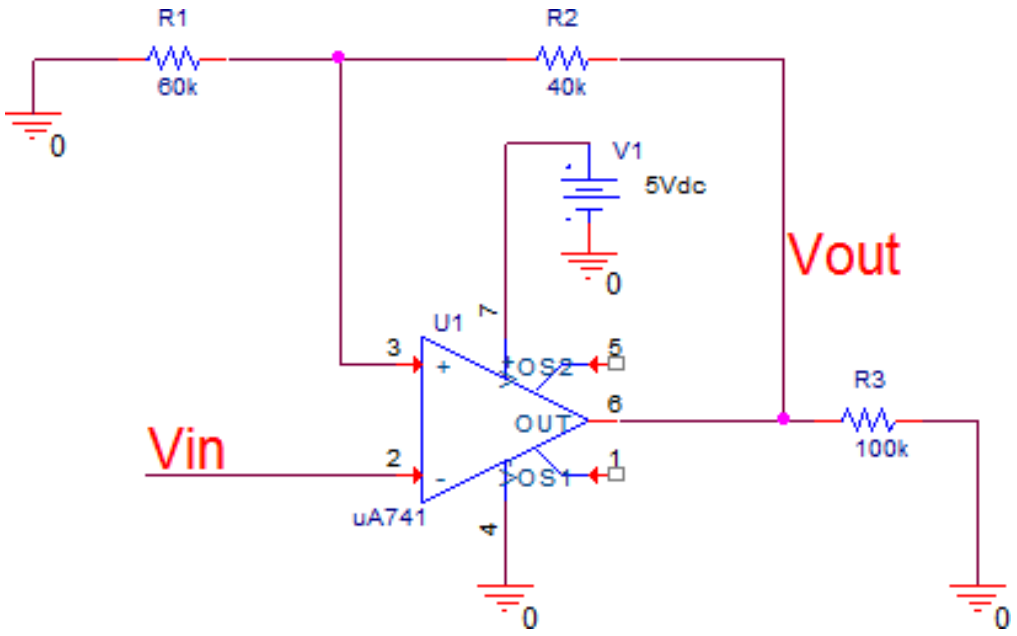
Voltage drop required to allow current flow through diodes greater than DC supply, therefore, no current flow.

V_{R1} **0 V**

3.2 (2 pnts) Sketch the voltage across the capacitor in the below circuit after a long time has passed.







3.3 (4 pnts) Considering the circuit above, what are the threshold(s) for **Vin** to toggle **Vout**? You may assume that the op-amp is ideal.

$$V_3 = V_{\text{out}} \frac{R1}{R1 + R2} = 0.6 V_{\text{out}}$$

$V_{\text{out}} = 0\text{V} \rightarrow$ negative to positive threshold $= 0$

$V_{\text{out}} = 5\text{V} \rightarrow$ positive to negative threshold $= 0.6 \times 5\text{V} = 3\text{V}$

3.4 (6 pnts) If **Vin** is a triangular wave (increases linearly from min to max, then decreases linearly from max to min) with an amplitude of 4 V and a frequency of 5 Hz, how long will **Vout** be HIGH?

Vout transition HIGH when Vout drops below 0V and transition low when Vout rises above 3 V

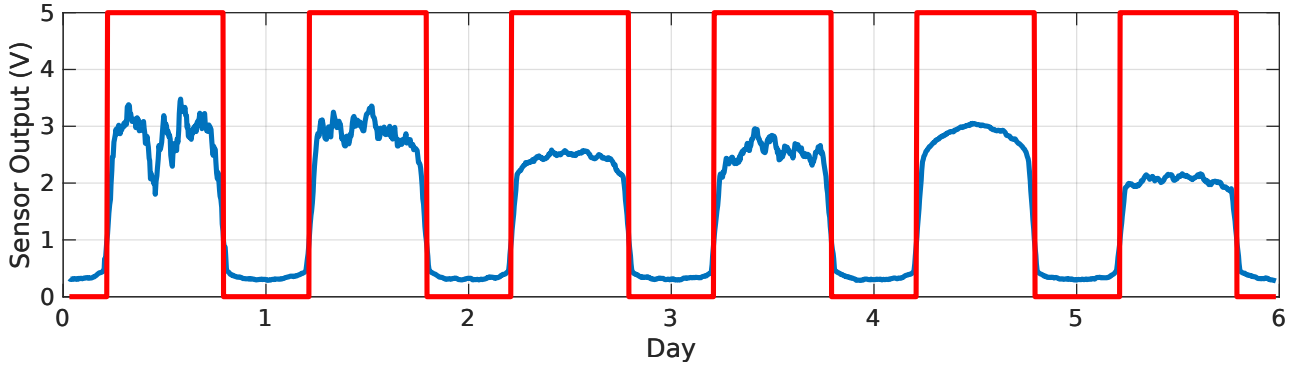
Time for Vin to drop from 0 V to -4 V → $t_{0\text{V}\rightarrow-4\text{V}} = \frac{T}{4} = 50\text{ms}$ $T = \frac{1}{f} = 0.2\text{ms}$

Time for Vin to rise form -4 V to 3 V → $t_{-4\text{V}\rightarrow3\text{V}} = \left(\frac{3-(-4)}{4-(-4)}\right)\frac{T}{2} = 87.5\text{ms}$

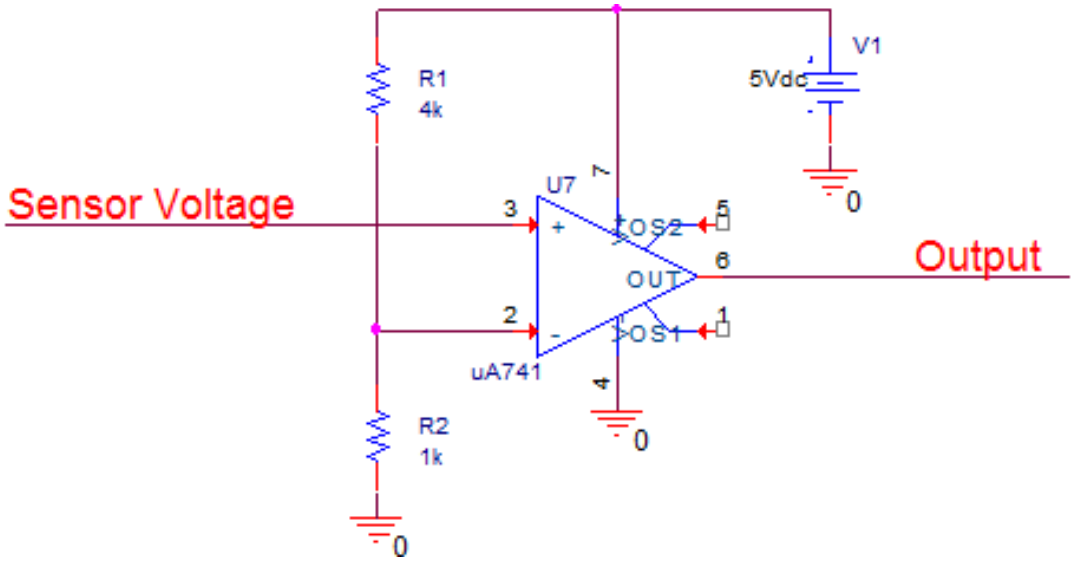
Total: $t_{\text{HIGH}} = t_{0\text{V}\rightarrow-4\text{V}} + t_{-4\text{V}\rightarrow3\text{V}} = 137.5\text{ms}$

Question Set 4. Day Counter (Miscellaneous)

You are tasked with designing a circuit that needs to keep track of how many days it has been active. For some odd reason, you cannot implement this in a way that you use a timer (e.g., 555) or crystal oscillator. As a work around, it is decided to use the sun as a day/night indicator. A sensor is assembled that gives voltage as a function of detected light. A sample sensor output is given below, where higher voltages indicate more light, i.e., daytime.



4.1 (4 pnts) The sensor voltage needs to be converted into a digital logic signal before being used to count the days, with logic HIGH voltage representing daytime. Design and sketch an op-amp circuit, with component values, that will achieve this. Select reasonable sized values for the components.

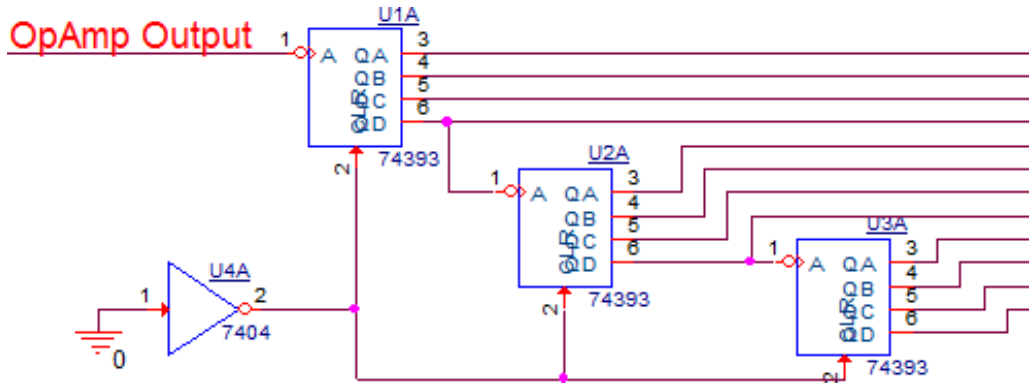


Compare voltage needs to be in the range of 0.75-1.5 V. Using 1 V. Select a reasonable value for R2 and calculate R1. A Schmitt trigger was also be acceptable here. For grading, inverted outputs were also accepted as they were the bulk of the answers.

$$V_2 = 1\text{V} = 5\text{V}\frac{R_2}{R1 + R2} \rightarrow R_1 = 4R_2$$

4.2 (2 pnts) Add a sketch of the output of the op-omp designed in 4.1 to the sensor graph given above.
Solution in plot above, consistent with designed circuit from 4.1 (namely: logic inversion)

4.3 (4 pnts) The output of the op-amp circuit is fed into the circuit below. How many days can this circuit count before it resets?



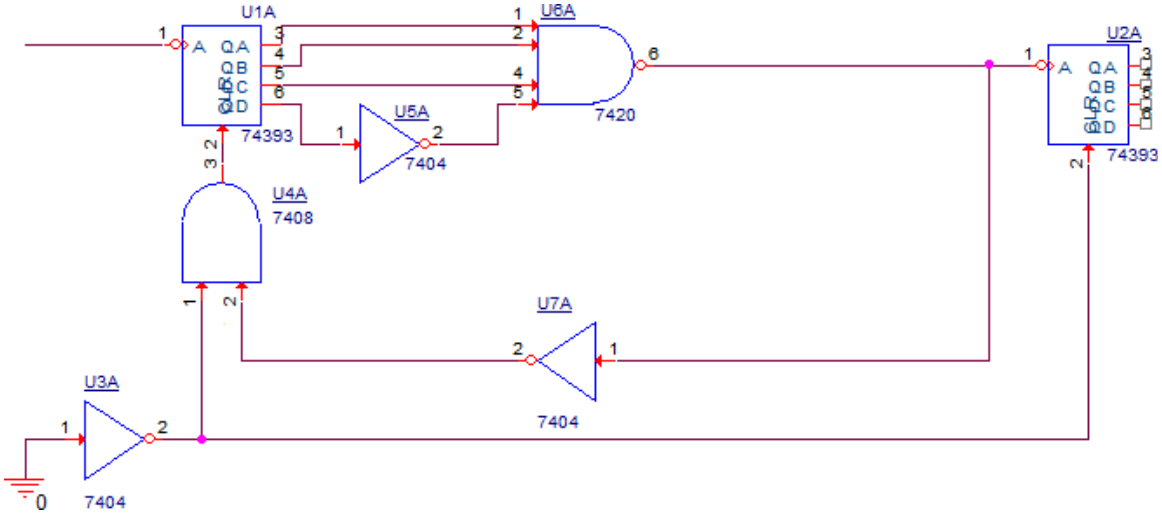
Each counter can count 16 day (includes 0): $16 \times 16 \times 16 = 4096$ Days

OR, 12 binary output lines: $2^{12} = 4096$ Days Note: it's max value is 4095, but 0 is included

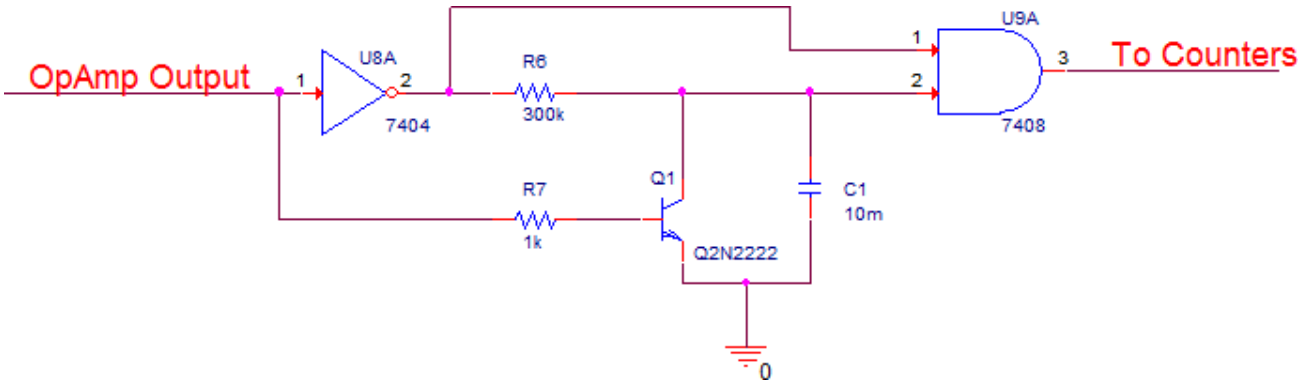
4.4 (2 pnts) The circuit from 4.3 is to be redesigned to count weeks instead of the total number of days. Logic gates need to be inserted between counters U1A and U2A such that the input to U2A is usually a logic HIGH, but transitions to a logic LOW after the last day of the first week counted. What single logic state of U1A's outputs should cause a logic LOW?

$$Q_A = 1, \quad Q_B = 1, \quad Q_C = 1, \quad Q_D = 0$$ binary 0111 = 7

4.5 (4 pnts) Draw in the necessary logic gates to produce the conditions required in 4.4. You must use all of U1A's outputs. Additionally, after a week has been counted, U1A needs to be reset to start counting a new week. Draw in the necessary logic gates to achieve this as well.



4.6 (2 pnts) The below circuitry was inserted between the op-amp subcircuit and the counter subcircuit. What is it's purpose and how does it work? Hint: the sensor may be placed were it is generally dark at night, but cars may drive by frequently.



Not: that this circuit should have had another inverter on the opAmp input. Iit was designed assuming that nighttime produced an OpAmp output of HIGH instead of the requested solution shown in pt 1&2. Due to this, LOW represents daylight. Any answer that was obviously confused because of this was accepted.

It will prevent triggering of the day counter by passing lights by requiring that the op-amp output stay LOW for a long time. This is tested by using the charge time of the given RC circuit. If both the inverse of the op-amp output and the RC circuit are HIGH (e.g., greater than TTL HIGH threshold), then the signal to the counter will be HIGH, otherwise it will stay LOW. The RC is reset to LOW (0V) any time the op-amp output is HIGH.

Any reasonable answer giving both PURPOSE and HOW was accepted.

4.7 (2 pnts) Do you expect to take the optional final? Your answer here is NON-BINDING.

The optional final will:

- cover all topics in the class,
- generally be more difficult than the quizzes (excluding quiz 1...maybe),
- Not have an LMS portion,
- replace your lowest quiz grade, which includes the LMS portion,
- **NOT** replace your lowest quiz grade, **IF** the final grade is the lowest.
  - i.e. you cannot hurt you overall grade by attempting the final.

YES NO

Extra work pages. Note the problem number work belongs to.

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