ENGR-2300

Electronic Instrumentation

Quiz 3

Fall 2018

Name SOLUTIONS

Section ___

Question 1 (20 Points) _____

Question 2 (20 Points) _____

Question 3 (20 Points) _____

Question 4 (20 Points) _____

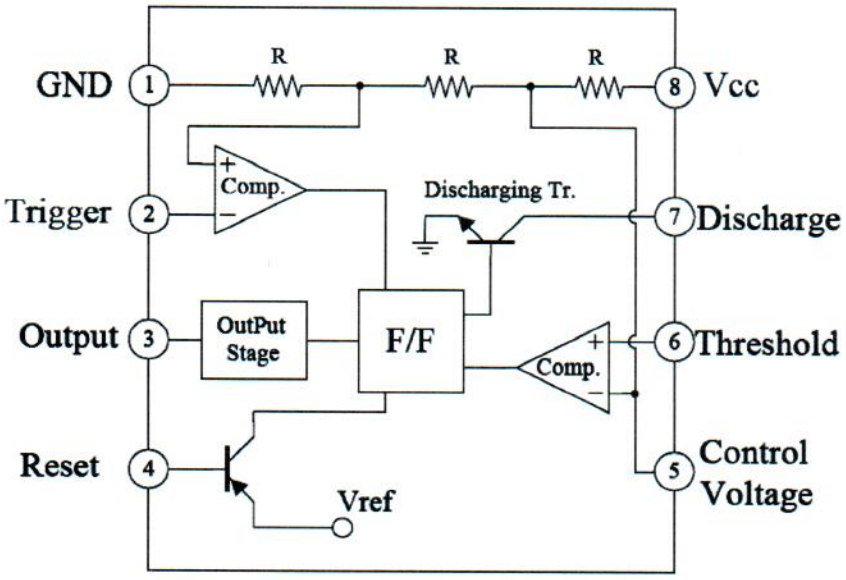
LMS Question is worth an additional 20pts

Total (80 points) _____

On all questions: **SHOW ALL WORK**. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS. No credit will be given for answers that appear without justification. Read the entire quiz before answering any questions. Also it may be easier to answer parts of questions out of order.

Some Additional Background plus

555 Timer Block Diagram

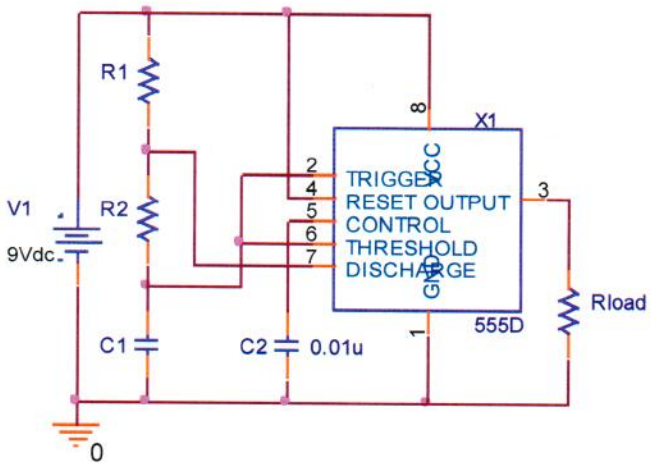


Zener Diodes: From Wikipedia: A **Zener diode** is a diode which allows current to flow in the forward direction in the same manner as an ideal diode, but also permits it to flow in the reverse direction when the voltage is above a certain value known as the breakdown voltage, "zener knee voltage", "zener voltage", "avalanche point", or "peak inverse voltage".
The device was named after Clarence Zener, who discovered this electrical property. Many diodes described as "zener" diodes rely instead on avalanche breakdown as the mechanism. Both types are used. Common applications include providing a reference voltage for voltage regulators, or to protect other semiconductor devices from momentary voltage pulses.

Type Number	Nominal Zener Voltage V_Z @ I_{ZT}[2] (Volts)	Test Current I_{ZT} (mA)	Maximum Zener Impedance Z_{ZT} @ I_{ZT}[1] (Ω)	Maximum Regulator Current I_{ZM}[2] (mA)	Maximum Reverse Leakage Current	
					T_A = 25°C I_R @ V_R = 1V (μA)	T_A = 150°C I_R @ V_R = 1V (μA)
1N746A	3.3	20	28	110	10	30
1N747A	3.6	20	24	100	10	30
1N748A	3.9	20	23	95	10	30
1N749A	4.3	20	22	85	2	30
1N750A	4.7	20	19	75	2	30
1N751A	5.1	20	17	70	1	20
1N752A	5.6	20	11	65	1	20
1N753A	6.2	20	7	60	0.1	20
1N754A	6.8	20	5	55	0.1	20
1N755A	7.5	20	6	50	0.1	20
1N756A	8.2	20	8	45	0.1	20
1N757A	9.1	20	10	40	0.1	20
1N758A	10	20	17	35	0.1	20
1N759A	12	20	30	30	0.1	20

Question 1 (20 Points) Astable Multivibrator (An Iconic 555 Timer Application)

a. (4pt) The 555 timer circuit shown is to have a duty cycle of 80%. For a given C1, what ratio of resistors R1/R2 will produce this duty cycle.



$$T1 = 0.693(R1 + R2)C1$$

$$T = 0.693(R1 + 2R2)C1$$

$$\frac{T1}{T} = \frac{0.693(R1+R2)C1}{0.693(R1*2R2)C1} = \frac{R1+R2}{R1+2R2} = .8$$

$$\frac{R1}{R2} = 3$$

b. (4pt) Using this ratio of R1/R2 and C1 = 10μF, calculate the values for R1 and R2 needed to yield a frequency of 20Hz.

$$f = \frac{1.44}{(R1+2R2)C1} = 20 = \frac{1.44}{(3R2+2R2)10^{-5}}$$

$$R2 = 1.44k \text{ and } R1 = 4.32k$$

c. (2pt) For an ideal 555, what are the maximum and minimum voltages on pin 2 above during normal operation?

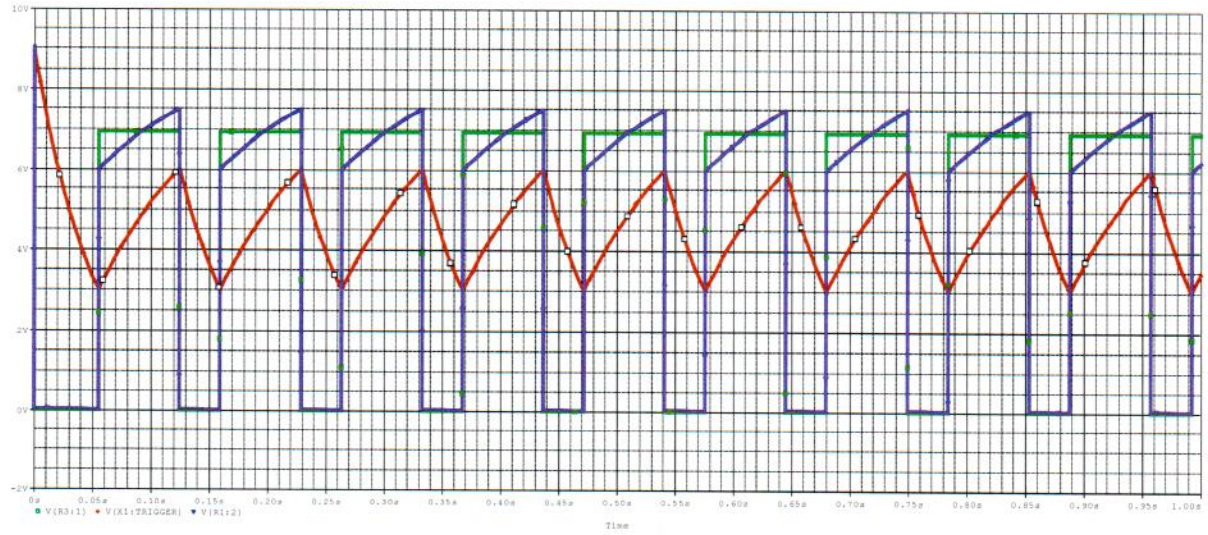
Max = 6V, Min = 3 because of the internal divider of the 555

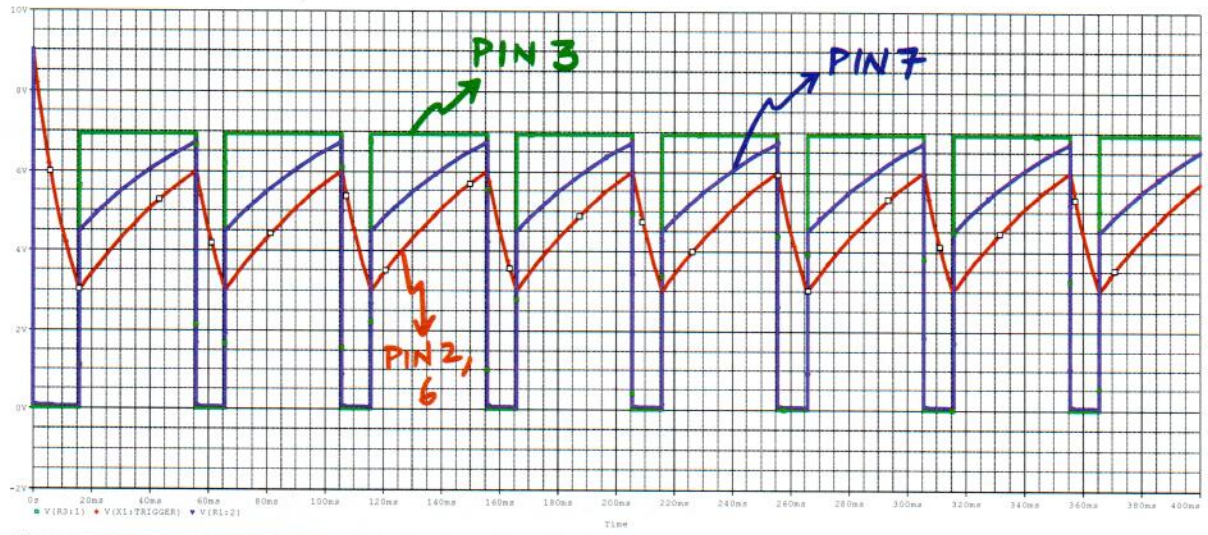
d. (4pt) For an ideal 555, what are the maximum and minimum voltages on pin 7 above during normal operation?

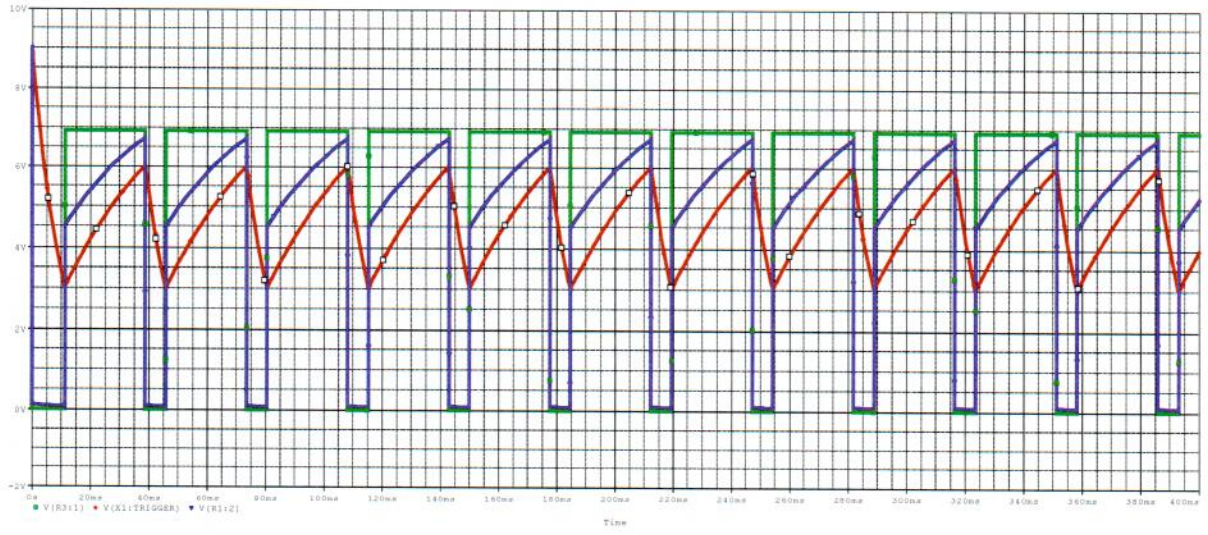
Min = 0 since on pin 7 the transistor connects to zero
Max = 6V plus the voltage across R2 or 6 + (0.25)3=6.75V

On the next page, the freq must be 20 Hz so the period must be 1/20=50ms so the 3rd plot is out. The 2nd plot has the correct frequency. The first plot does not have an 80% duty cycle, so it has to be the middle plot. The individual curves must satisfy the voltages listed above so they are as labeled.

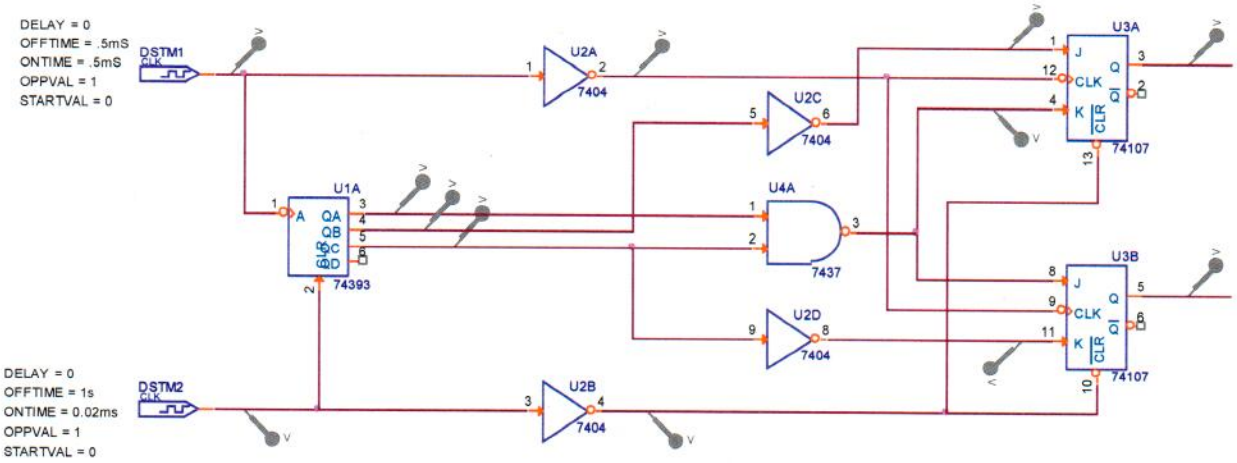
e. (6pts) Which of the sets of plots below shows the voltages on pins 2, 3, 6 and 7 for the case considered here? Label which plot is which in the correct figure.





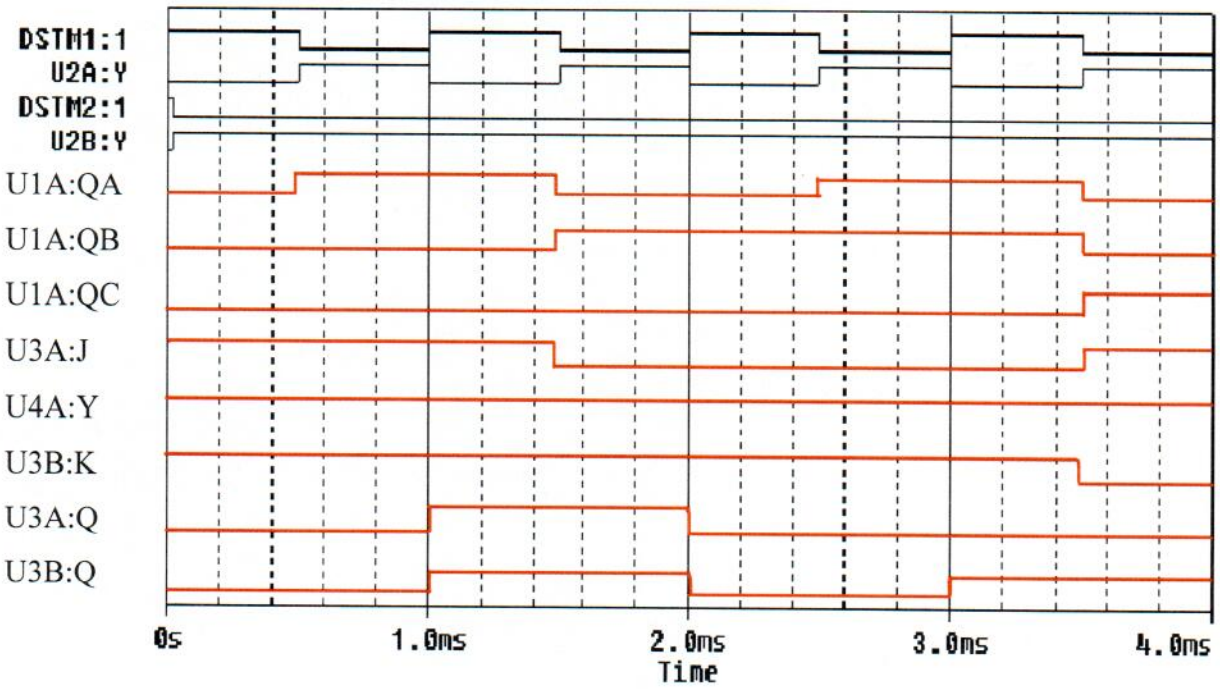


Question 2 (20 Points) Combinational & Sequential Logic Circuits



In the circuit pictured above, clock DSTM1 provides a clock signal to a counter and two flip flops. The flip flops are clocked one half cycle after the counter to allow for propagation of the signals through the gates. (The counter changes on the negative edge of DSMT1 and the flop flops change on the negative edge of U2A:Y.) DSTM2 provides an initial reset pulse to both chips. This is required by PSpice to ensure that all sequential devices start in a known state.

a. The timing diagram below shows the reset pulses and the clock signals. Sketch the following signals in the space provided: the output from the counter (U1A:QA, U1A:QB, & U1A:QC); the output from the combinational logic (U2C:Y=U3A:J, U4A:Y=U3A:K=U3B:J, & U2D:Y=U3B:K); and the output from the flip flops (U3A:Q & U4A:Q). (2pt per trace = ***16pt***)

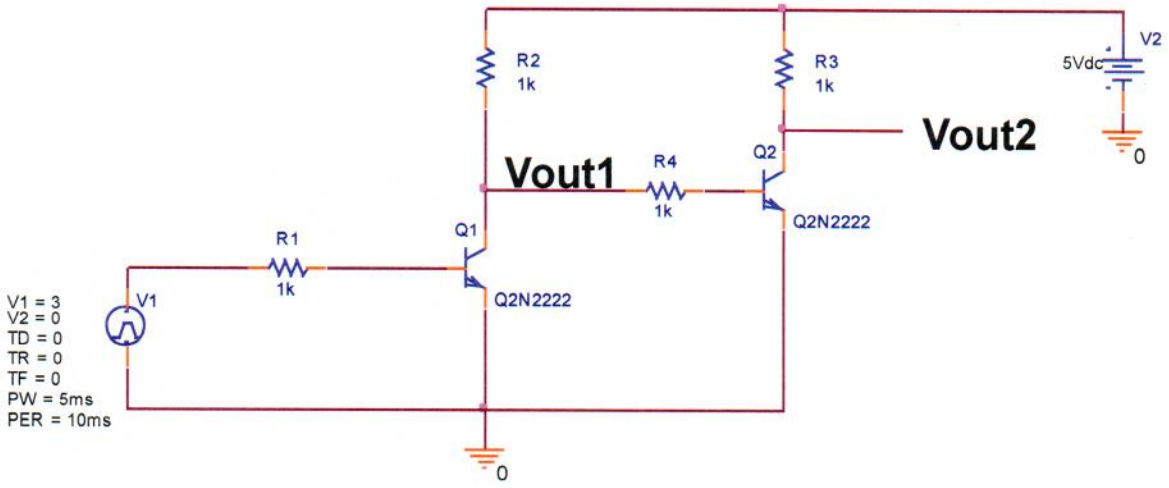


b. (2 pts) A 4-bit counter is cleared and then receives a string of clock pulses. What are QA, QB, QC and QD after 16 clock pulses? Clearly indicate the state of each signal.

15 → 1111
16 → 10000
4-bit counter output

QD	QC	QB	QA
0	0	0	0

c. (2 pts) Consider the circuit below consisting of two NPN transistors Q1 and Q2. Vout1 is the collector terminal of Q1 and Vout2 is the collector terminal of Q2. For a given voltage V1, fill the table below indicating the status of Q1, Q2 (open/closed) and voltage level of Vout1 and Vout2 (High/low). *Note*: Transistor Q1 is open means Q1 is off and no current flows through it.



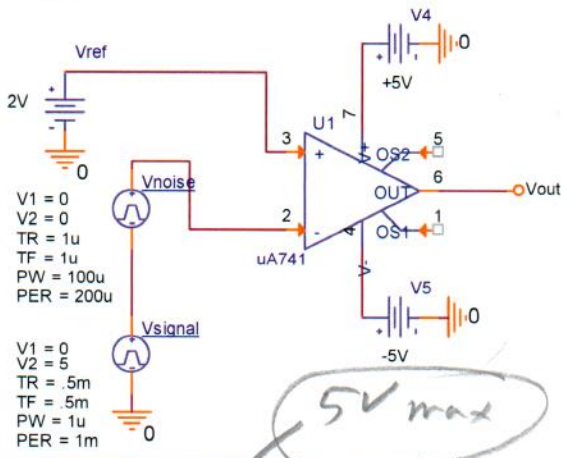
V1	Q1 (open/closed)	Vout1 (High/Low)	Q2 (open/closed)	Vout2 (High/Low)
0V	Open	High	closed	Low
3V	closed	Low	open	High

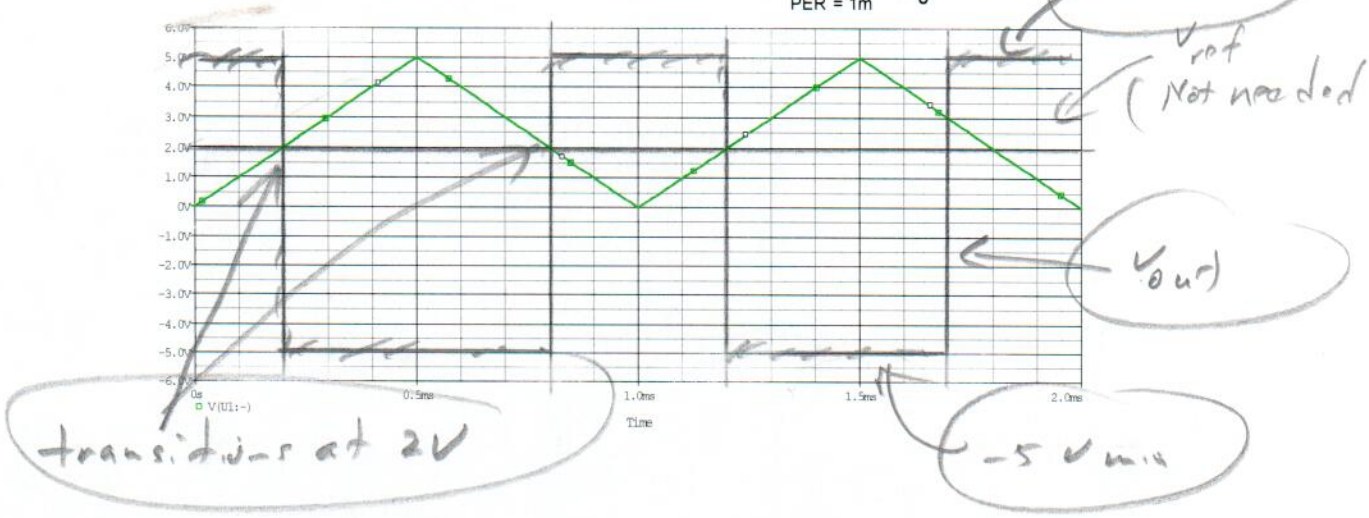
Vout2 = V1 → BUFFER!

Question 3 (20 Points) Comparator and Schmitt Trigger

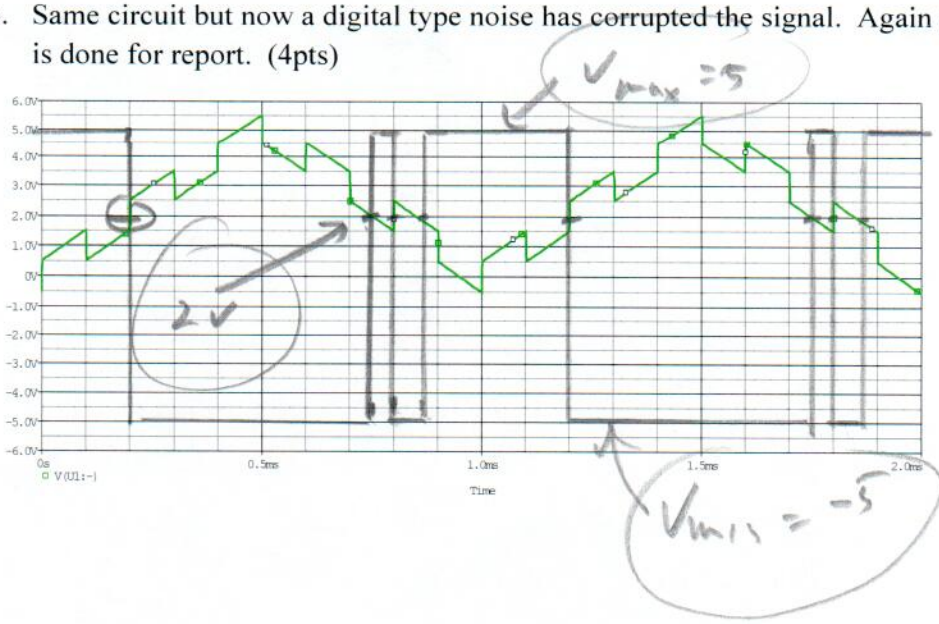
In this problem, we investigate the same properties of Schmitt Triggers we did in Experiment 6. Assume the output of the op-amps is capable of reaching the power supply voltages.

a. For the circuit shown the input signal, Vsignal is compared to Vref. For this part there isn't any noise. Vnoise amplitude is 0V. The plot below has the Vsignal (without noise). On this plot, draw Vout. Label the plot as you would for an experiment report. (4pts)





b. Same circuit but now a digital type noise has corrupted the signal. Again plot Vout. Label as is done for report. (4pts)

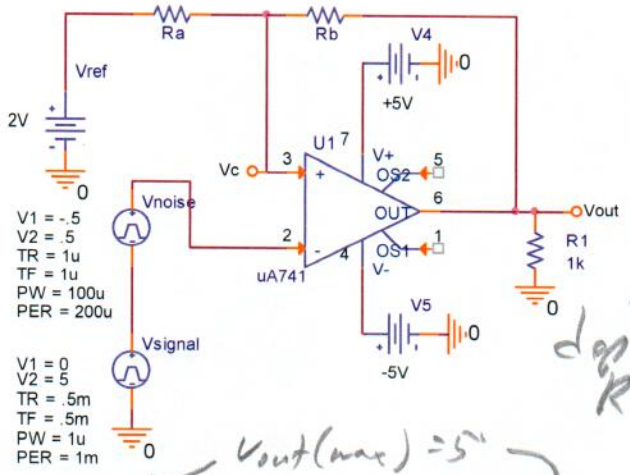


c. It is desired to remove transitions of the output due to the noise. The output should look similar to part a. but the timing will be changed. In other words, there should only be one output pulse per cycle of the signal. Use the schematic below. This can be done using trial and error.

i. Ra is set at 1kΩ. Determine a value for Rb which will have the desired effect. There is a range of possible value. (2pts)

ii. For your value of Rb, determine the possible values for the voltage at the point labeled as Vc. (2pts)

iii. Plot Vout and Vc on the plot below for your values of Rb. (4pts)



Rb=

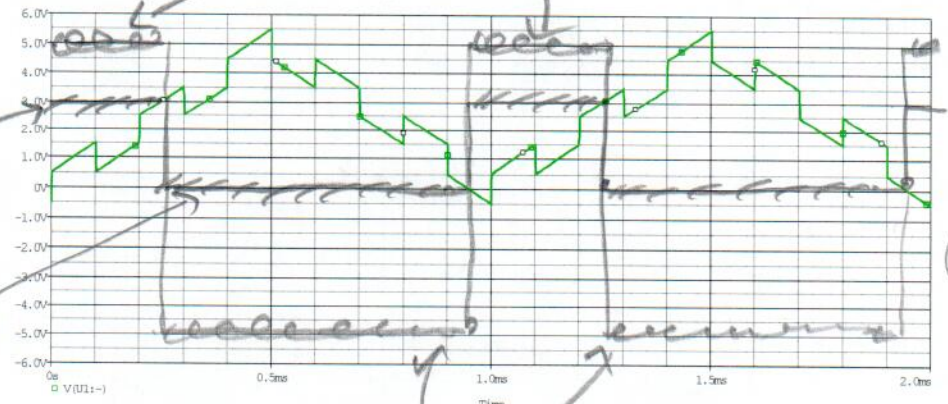
Vc(max) =

Vc(min) =

any value if $2k \leq R_b \leq 15k\Omega$

depends on R_b

$R_b(k\Omega)$	$V_c(max)$	$V_c(min)$
2.5	2.86	0
3	2.75	0.25
5	2.50	0.83
7	2.38	1.13
10	2.27	1.36
15	2.19	1.56



$V_{out(max)} = 5$

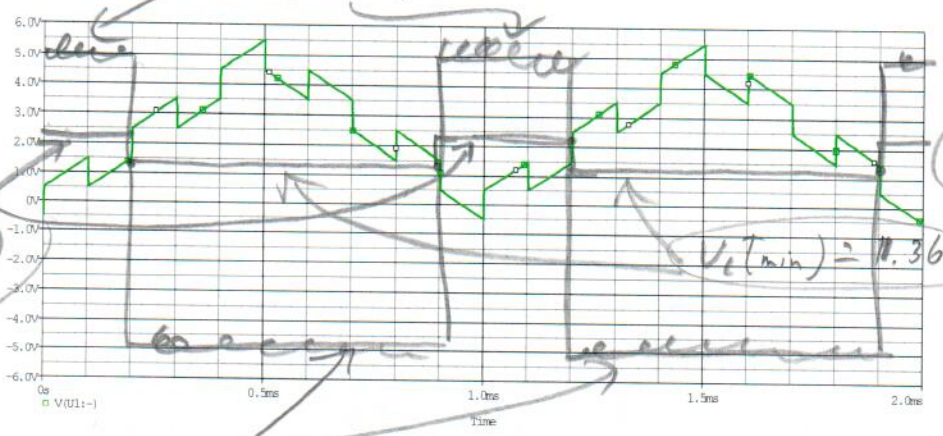
$V_{c\,max} = 2.86V$

$V_{c(min)} = 0$

$V_{out(min)} = -5$

Plot Vc and Vout. Be sure to label significant voltages.

2.5 ± Ω R_b



Spare plot for part c. Use if needed.

$R_b = 10k\Omega$

Transitions slightly different for different values of R_b

d. Now consider real op-amps but continue to use your values for Rb. The output voltage of the real op-amp won't match the power supply voltage. If Vout can only reach to 1V away from the power supply (Vout max is 4V and Vout min is -4V) what will now be your values for Vc (use the same analysis as you used for part c.ii.) (2pts)

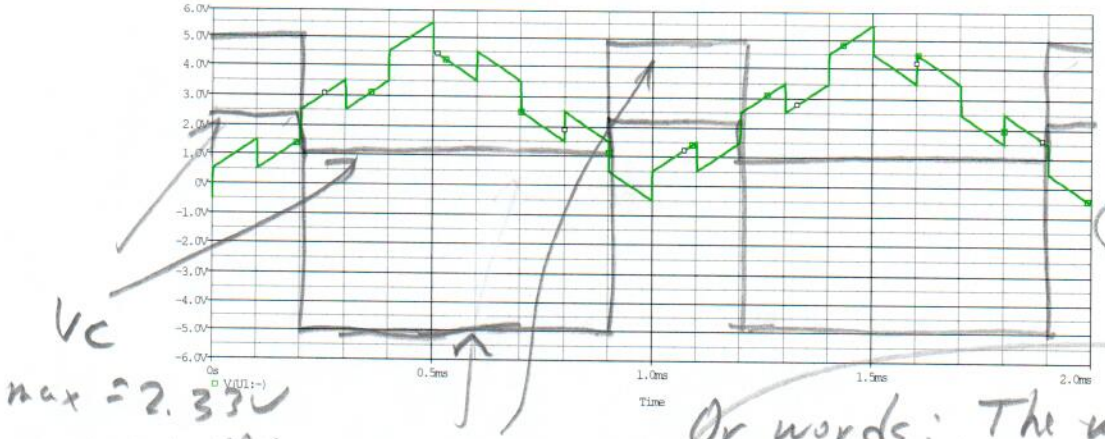
Depends on R_b

R_b	Vc(max)	Vc(min)
2.5k	2.52V	0.29V
5k	2.33V	1.00V
10k	2.15V	1.45V
15k	2.13V	1.63V

e. Will your design still work to eliminate the false transitions caused by the noise? Support your answer by giving your analysis. You don't need to plot the results. (2pts)

Yes if $2k < R_b < 13k\Omega$

No if $R_b > 13k\Omega$



Use plot if it helps answer part e.

2nd plot with $R_b = 5k\Omega$

Or words: The values of Vc are sufficiently different to avoid false transitions due to the noise.

$V_o \approx -12V$

Question 4 (20 Points) Diode Circuits

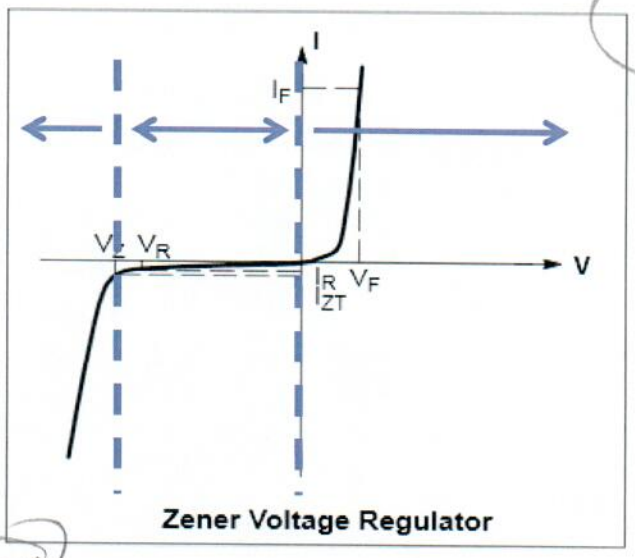
a. (4 Pts) We wish to regulate a 12V DC power supply using a Zener Diode from the table at the beginning of this quiz. Like all Zeners, this diode has three voltage ranges shown in its I-V curve below: the Off Region, The Forward Bias Region and the Reverse Bias Region. Assuming ideal conditions for this diode, complete the following

i. The voltage across the diode is $V_D \approx 0.7V$ in the Forward Region

ii. The voltage across the diode is $V_D \approx 12V$ in the Reverse Region

iii. The current through the diode is $I_D \approx 0A$ in the OFF Region

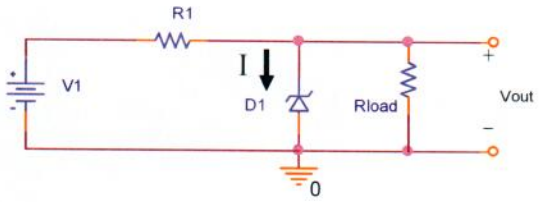
iv. What Zener part number would be used for this application? 1N759A or 1N759



Zener Voltage Regulator

6.2V

b. For the circuit shown, the Zener is a 1N753A. Use the "Some Additional Background" information at the beginning of this exam. (3pts)



i. What is the Zener voltage for this diode? 6.2V

ii. What is maximum Zener current recommended by the manufacturer? This is also referred to as the Maximum Regulator Current.

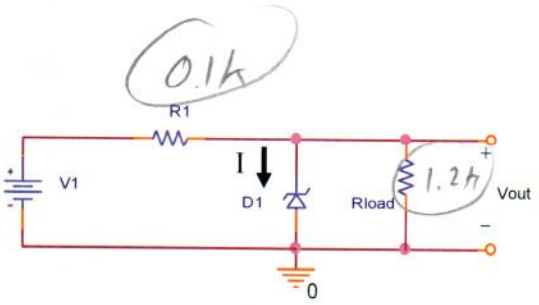
I(max) = 60mA

iii. If operated at the maximum Zener current, how much power will be dissipated by the Zener.

Power = $V \cdot I$ = 372mW OR 0.372W

0.1k

This is the same circuit as part b and is still using the 1N753A Zener.



The circuit shown

V1 has various values

Complete the table for different values of V1 and fill in the following table:

V1	Vout	I (Zener current)
4V	3.69V	0
8V	6.2V	12.8mA
12V	6.2V	52.8mA

$V_1 = 4V$ Zener is off — no current

4V, 0.1k, 1.2k $V_{out} = \left(4 \times \frac{1.2}{1.2+0.1}\right) = 3.69$ to $3.7V$

$V_1 = 8V$ Zener on $V_{out} = V_{zener} = 6.2V$ $I_{Rload} = 6.2/1.2 = 5.17mA$

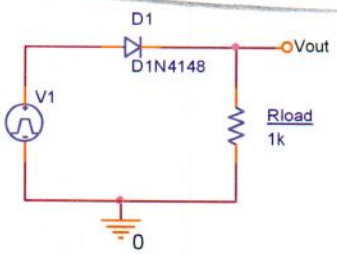
$I_{R_1} = (8-6.2)/0.1 = 18mA$

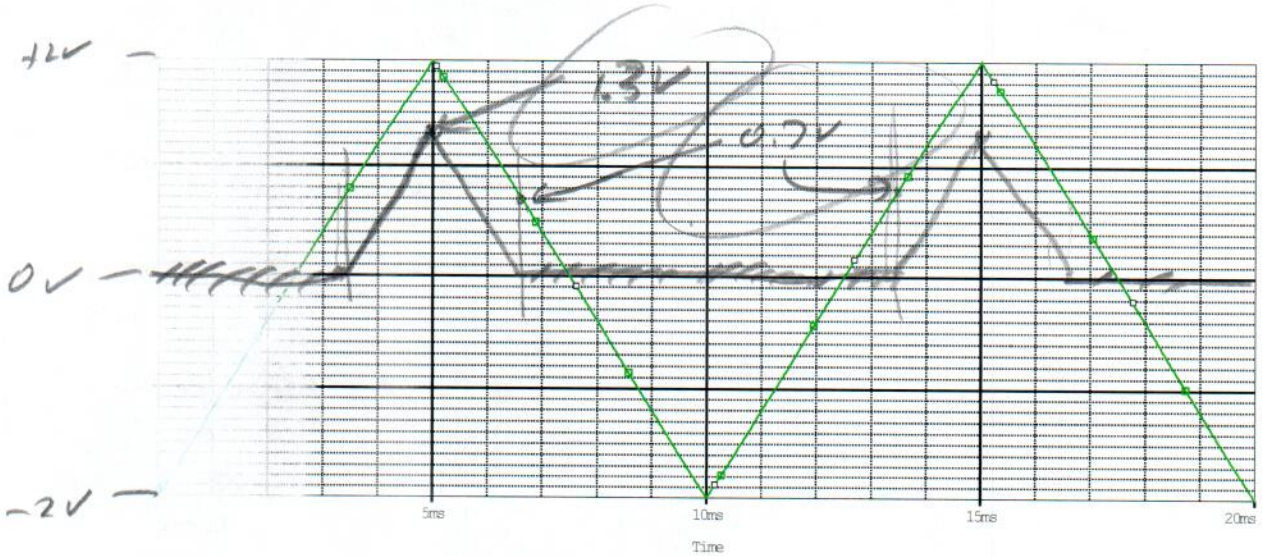
$I_z = 18 - 5.17 = 12.8mA$

$V_1 = 12V$ $V_{out} = 6.2$ $I_{R_1} = (12-6.2)/0.1 = 58mA$

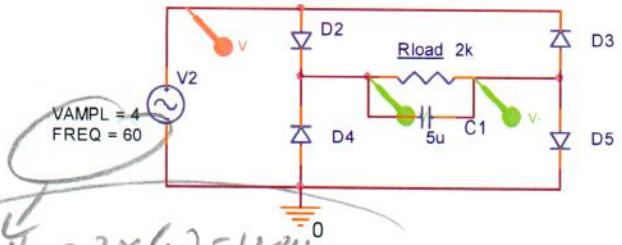
$I_z = I_{R_1} - I_{Rload} = 58 - 5.17 = 52.8mA$

For the circuit shown, plot Vout relative to ground on the plot below. V1 is displayed on the plot. Use the V_{on} diode model with V_{on}=0.7V. Label as you would for a report. (3pts)





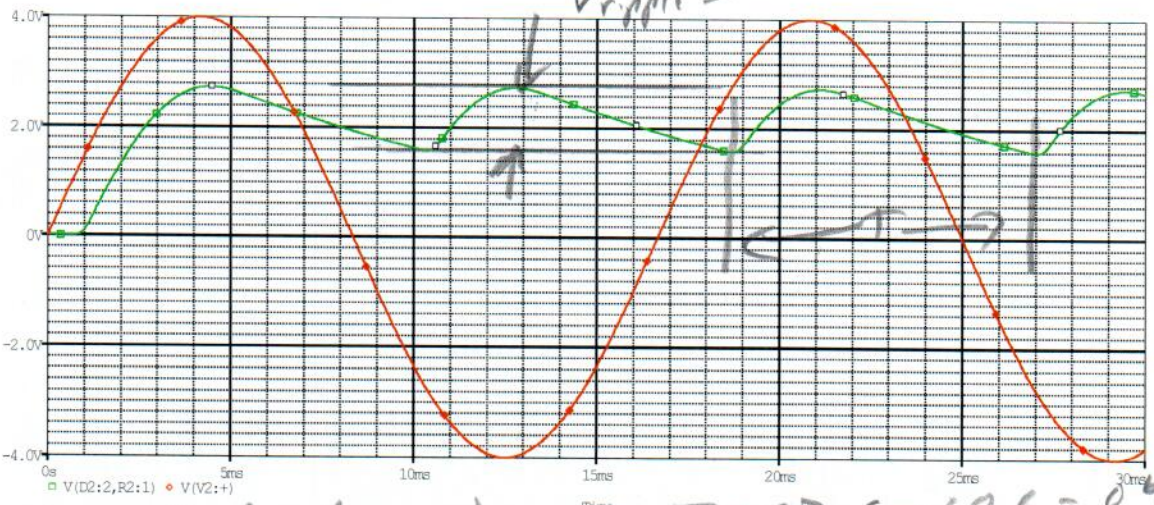
e. For the circuit shown, the input and the output voltages are shown in the plot below. Ignore the 1st ½ cycle. (3pts)



i. Determine the values of:

V_{ripple} 1.2V_pp The peak to peak value of the ripple on the output. Ignore the 1st ½ cycle.

f_{ripple} 120Hz The frequency of the ripple.



It is desired to reduce the magnitude of the ripple by a factor of **approximately** 2. List something that can be changed for this circuit to achieve this, and list how much it would need to be changed (and if it would need to be increased or decreased.)

1) Double C1 ⇒ C1 = 10uF

2) Double Rload ⇒ Rload = 4kΩ

3) Double the drive freq. f = 120Hz

Real world – the load and drive will be fixed and can't be change.

f. Do you expect to take the optional final? Your answer here is NON-BINDING. (1pt)
The optional final will:

- cover all topics in the class,
- generally be more difficult than the quizzes
- Not have an LMS portion,
- replace your lowest quiz grade, which includes the LMS portion,
- NOT replace your lowest quiz grade, IF the final grade is the lowest. i.e. you cannot hurt you overall grade by attempting the final.

Yes No

with also allow decreasing $|V_2|$ but needs not by 1/2 because of diode drop, rather drop to ~2.8V peak to 0 - 5.6V_pp