# ENGR-2300

Electronic Instrumentation

Quiz 3

Spring 2014

On all questions: **SHOW ALL WORK**. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES <u>AND UNITS</u>. No credit will be given for answers that appear without justification. Also, if there is a small flaw in your reasoning, we will not know and not be able to give you credit for what you have correct if you do not provide information on how you solved the problem. Read the entire quiz before answering any questions. Also it may be easier to answer parts of questions out of order.

K. A. Connor

Some Additional Background
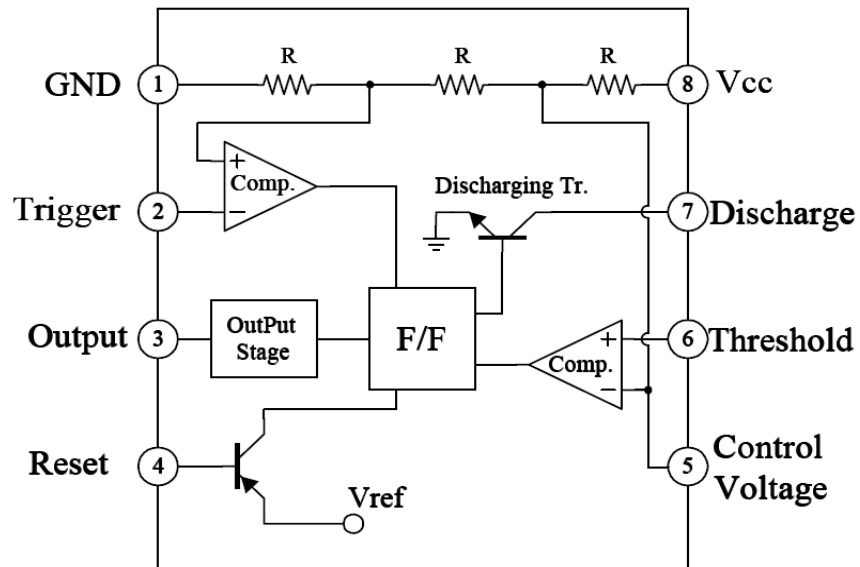
Electrical Signals (Cell Phone Disco) at the Franklin Institute
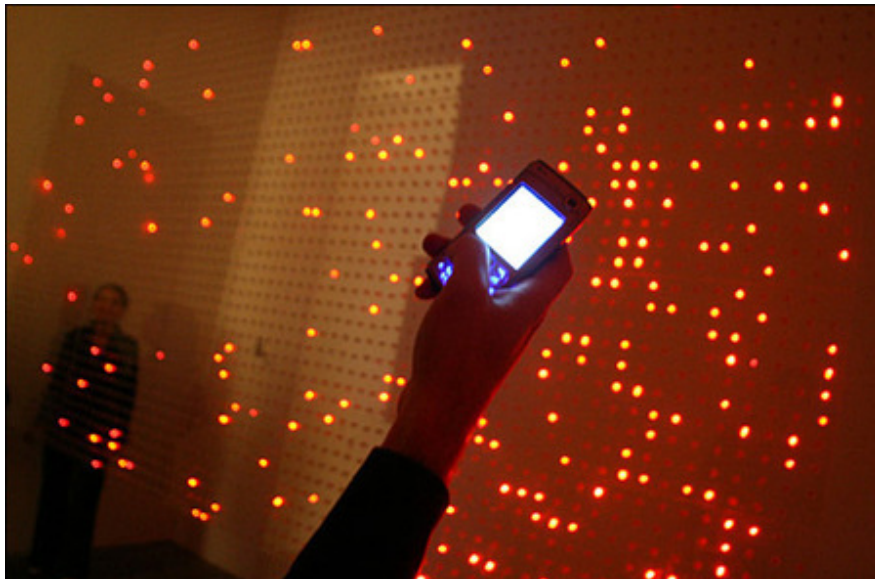
An art installation at Philadelphia's Franklin Institute, "Electrical Signals," is an array of light-emitting diodes (LEDs) that respond to electrical signals imperceptible to the human eye. As visitors make a call or send a text message from their own cell phones, the transmitted signals cause the LEDs to light up. Any idea how this works?

Check out http://www.cellphonedisco.org/ for more information about this and similar installations in Pittsburgh and elsewhere.

K. A. Connor

Question 1 (25 Points) Astable Multivibrator (An Iconic 555 Timer Application)
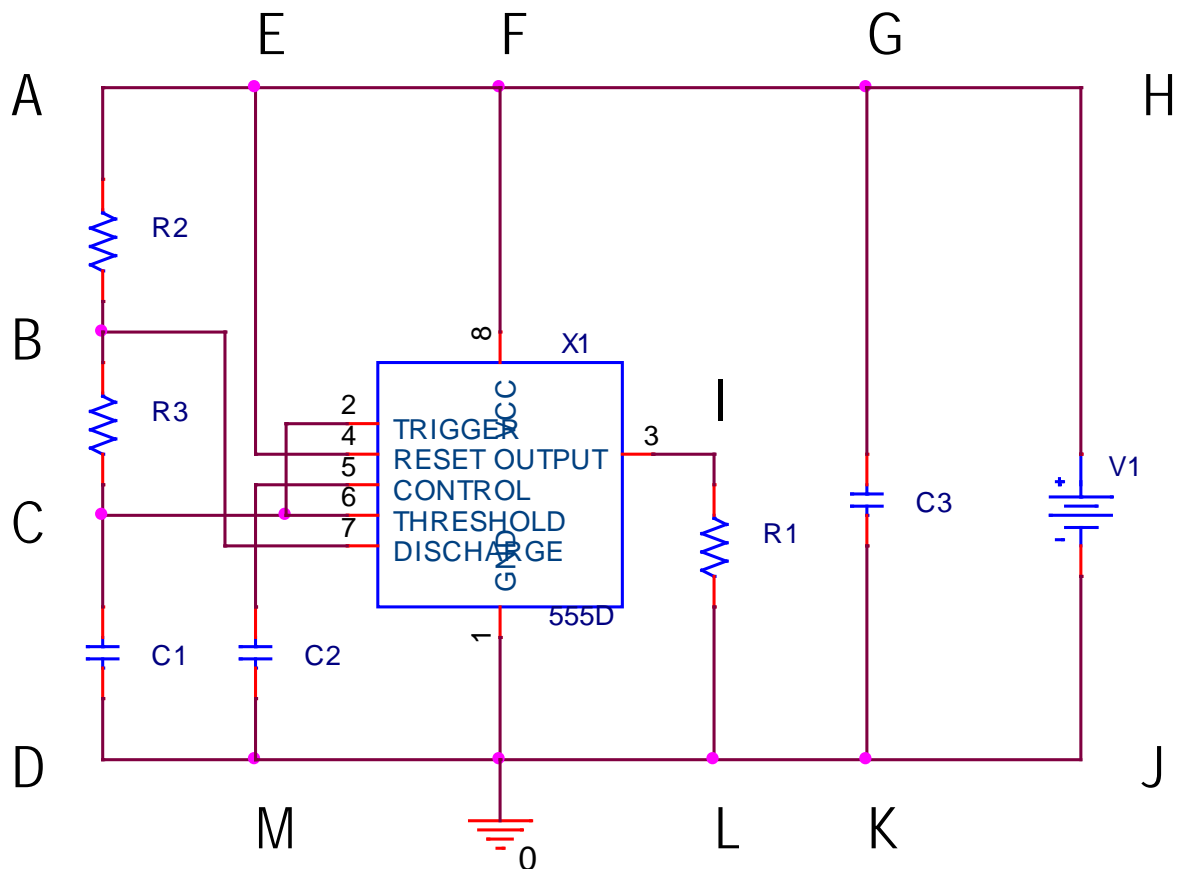
a. Consider first the circuit consisting only of the resistors R2 & R3, the capacitor C1 and the voltage source V1. Which of the following expressions is the mathematical representation of the voltage across the capacitor V_C vs. time after the switch is closed? (4 Points) *Hint: What is the voltage V_C at $t = 0$ and $t = \infty$?*

i) $V_C = V1 + V1\exp(-t/\tau)$

ii) $V_C = V1\exp(-t/\tau)$

iii) $V_C = V1 - V1\exp(-t/\tau)$

iv) $V_C = -V1 + V1\exp(-t/\tau)$

Which is the correct expression for the time constant τ?

i) $\tau = \dfrac{(R2 + R3)}{C1}$

ii) $\tau = (R2 + R3)C1$

iii) $\tau = \dfrac{C1}{(R2 + R3)}$

iv) $\tau = \dfrac{1}{[(R2 + R3)C1]}$
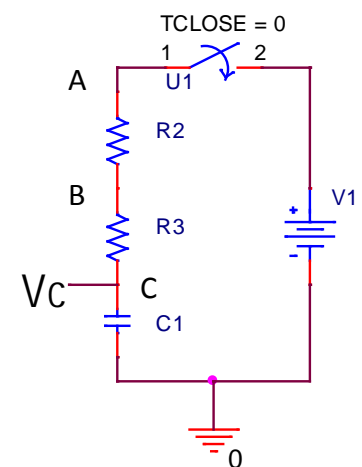
b. Using the same circuit parameters listed in part c, this circuit is simulated using PSpice, and the following voltages observed at points A, B and C. Label the three voltage traces with the corresponding letter from the circuit diagram. (3 points)
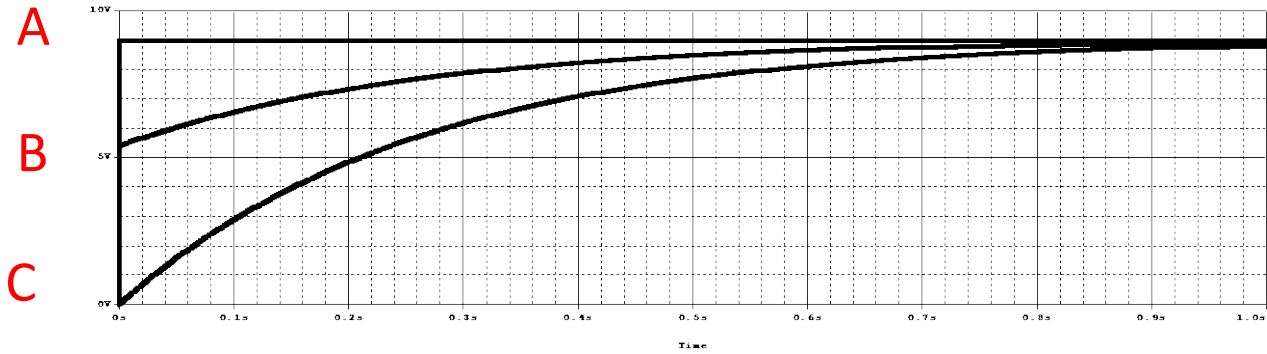

Simulation Results for Astable Circuit:
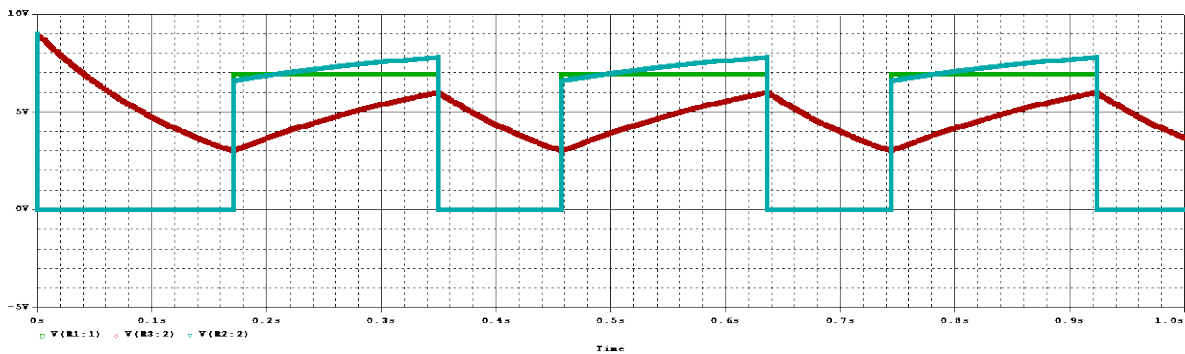
c. A 555 timer, astable multivibrator is built as above with R1 = 1kΩ, R2 = 22kΩ, R3 = 33kΩ, C1 = 4.7μF, C2 = 0.01μF, C3 = 470μF, and V1 = 9V. Determine the **on time** (T1) and the **off time** (T2) for this circuit. (4 Points)

T1=.179s   T2=.107s   in agreement with the PSpice results on the previous page.

d. Plot the output voltage below, showing two full cycles, starting with the output voltage at its maximum. Label the horizontal and vertical scales. (5 Points)
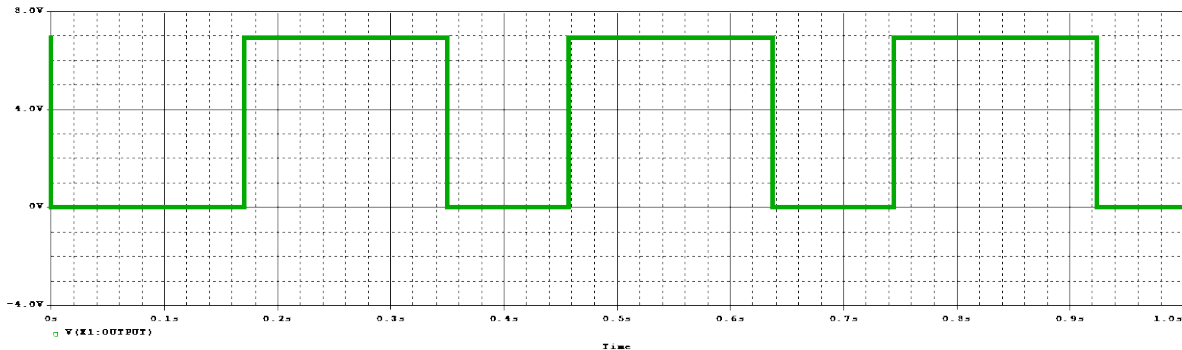

Answers for the peak output value in the range of 5-9V are OK. Generally, the output should be a little less than the power voltage, but this also depends on the load resistance.

e. Determine the maximum and minimum voltages at pins 6 and 7. Assume that the circuit is in steady state. (4 Points)

Ans: Pin 6 is trivial. The max is 6V and the min is 3V. For pin 7, it is necessary to use the voltage divider made with R2 and R3. For the max value, V7$_{MAX}$ = 6V + (0.6)3V = 7.8V. For the min value, V7$_{MIN}$ = 3 + (0.6)6V = 6.6V. Note that V7$_{MIN}$ is ambiguous, so zero is also acceptable.

f. Plot two cycles of the voltage at pin 6. Label the vertical and horizontal scales. (5 Points)

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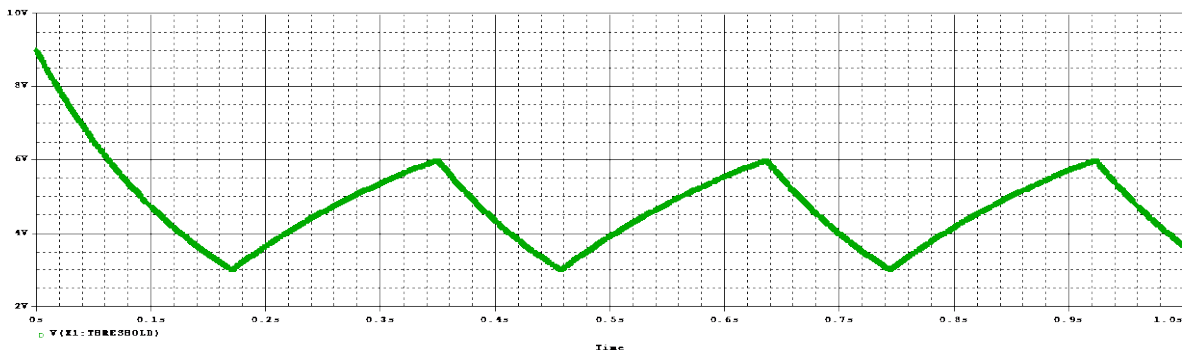
Question 2 (25 Points) Combinational Logic Circuits

It is possible to configure any standard logic gate out of either just NOR gates or NAND gates.
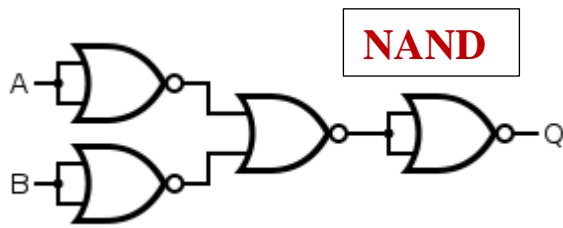*Hint: Determine the states of the other points in each circuit as you fill out the tables.*

a. The following circuit is configured using only NAND gates. Fill in the truth table for this
    circuit and identify the standard logic gate that behaves in the same manner. (6 points)

OR
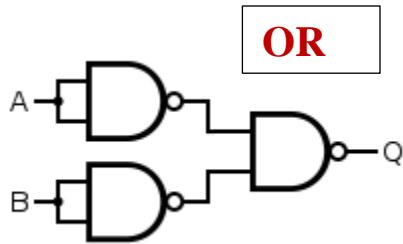
Input A	Input B	C	D	Output Q
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

b. The following circuit is configured using only NOR gates. Fill in the truth table for this
    circuit and identify the standard logic gate that behaves in the same manner. (6 points)

NAND

Input A	Input B	C	D	E	Output Q
0	0	1	1	0	1
0	1	1	0	0	1
1	0	0	1	0	1
1	1	0	0	1	0

c. The following circuit is configured using only NAND gates. Fill in the truth table for this
    circuit and identify the standard logic gate that behaves in the same manner. (6 points)
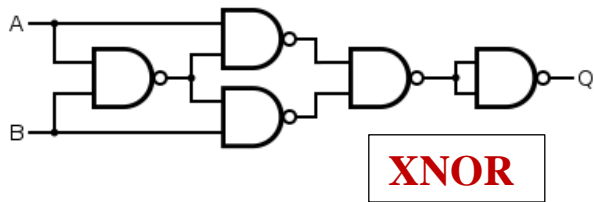
XNOR

Input A	Input B	C	D	E	F	Output Q
0	0	1	1	1	0	1
0	1	1	1	0	1	0
1	0	1	0	1	1	0
1	1	0	1	1	0	1

d. The following circuit is configured using only NOR gates. Fill in the truth table for this
    circuit and identify the standard logic gate that behaves in the same manner. (6 points)
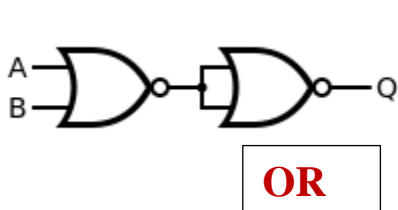
OR

Input A	Input B	C	Output Q
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

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e. What logic gate can be realized with either the NAND or NOR configuration shown below? (1 point)
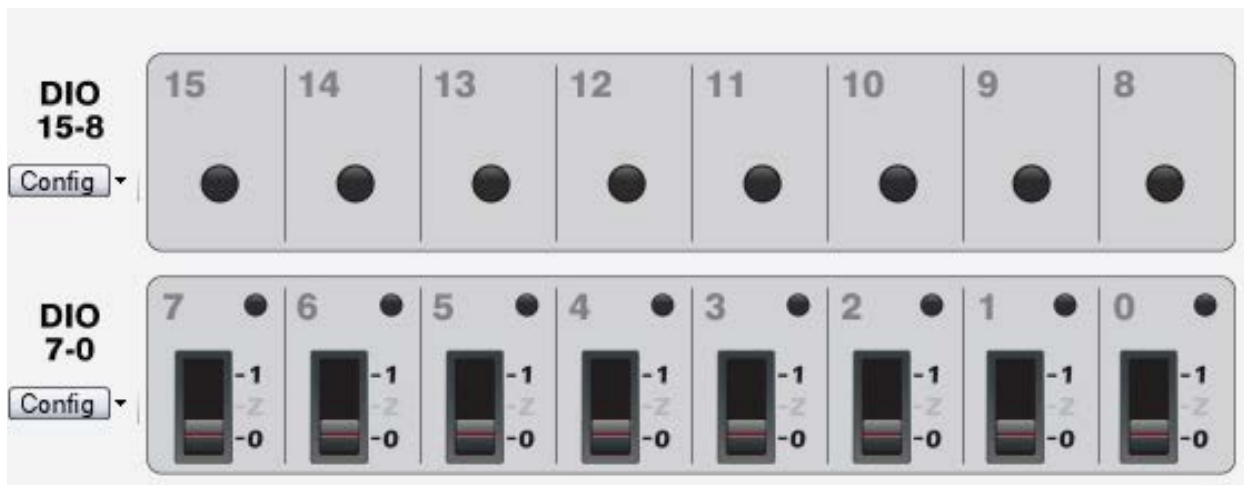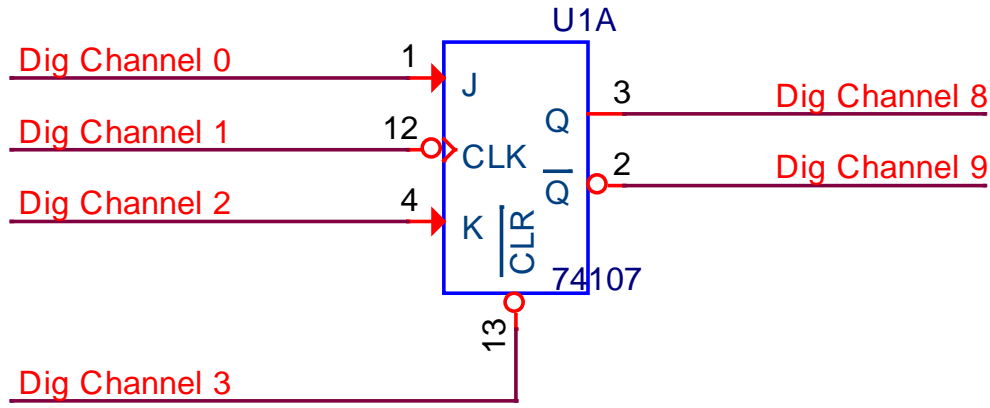
Both are NOT gates or inverters

A ─□D○─ Q

NOT

A ─□D○─ Q

Question 3 (25 Points) Sequential Logic & Switching

The following circuit shows a JK Flip-Flop being driven by 4 digital signals (channels 0-3) and monitored by two digital channels (8 & 9).

a. First assume that the signal on $\overline{CLR}$ has been cycled so that the output is in a known state with Q low. What position should the Channel 3 switch be in after $\overline{CLR}$ has been cycled? (2 points)

High. This info is included in the last part of problem 4.

b. Next, Channels 0 & 2 are both set low (zero) and Channel 1 is switched high and low. Fill in the table below for this sequence. This process is repeated for each of the four possible combinations of Channels 0 & 2. Fill in the other three tables. (8 points)

0 = J   2 = K   1 = CLK   8 = Q   9 = Qbar

Answers below can be written as 0 or low, 1 or high

Channel 0 = low; Channel 2 = low	Channel 8	Channel 9
Channel 1 = high	low	high
Channel 1 = low	low	high
Channel 1 = high	low	high
Channel 1 = low	low	high
Channel 1 = high	low	high
Channel 1 = low	low	high
Channel 1 = high	low	high
Channel 1 = low	low	high

J = 0, K = 1 then Q stays low

| Channel 0 = low; Channel 2 = high	Channel 8	Channel 9
Channel 1 = high	low	high
Channel 1 = low	low	high
Channel 1 = high	low	high
Channel 1 = low	low	high
Channel 1 = high	low	high
Channel 1 = low	low	high
Channel 1 = high	low	high
Channel 1 = low	low	high

J = 1, K = 0 then Q goes high at the falling edge of the clock pulse

Channel 0 = high; Channel 2 = low	Channel 8	Channel 9
Channel 1 = high	low	high
Channel 1 = low	high	low
Channel 1 = high	high	low
Channel 1 = low	high	low
Channel 1 = high	high	low
Channel 1 = low	high	low
Channel 1 = high	high	low
Channel 1 = low	high	low

J = 1, K = 1 then Q toggles at the falling edge of the clock pulse

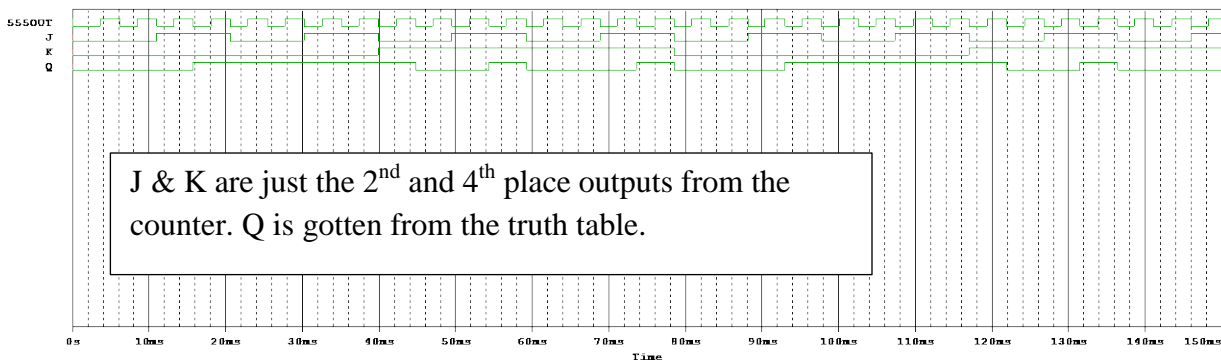| Channel 0 = high; Channel 2 = high	Channel 8	Channel 9
Channel 1 = high	low	high
Channel 1 = low	high	low
Channel 1 = high	high	low
Channel 1 = low	low	high
Channel 1 = high	low	high
Channel 1 = low	high	low
Channel 1 = high	high	low
Channel 1 = low	low	high

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c. The circuit below is configured to drive the JK Flip Flop. The output signal from the 555 (at A) is shown. Complete the timing diagram by carefully sketching the 3 additional signals at B, C and D. (6 Points) *The counter also responds to the trailing edge of the pulses it counts. The horizontal scale goes from 0 to 150ms.*
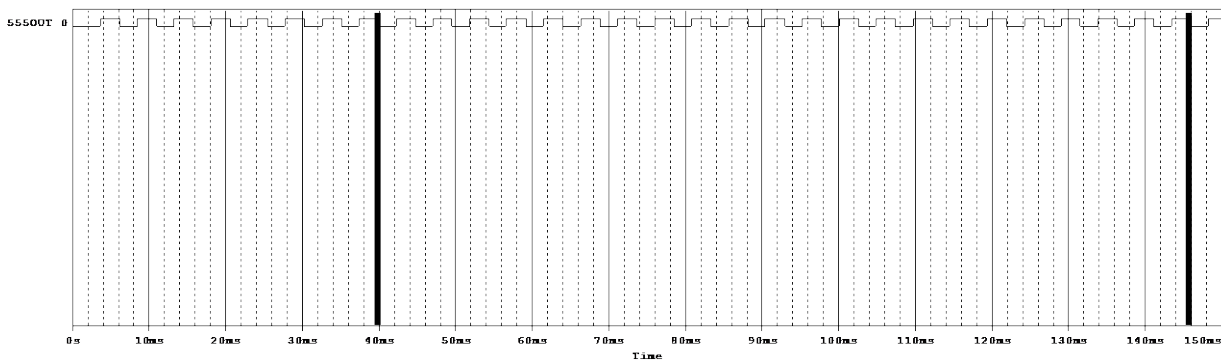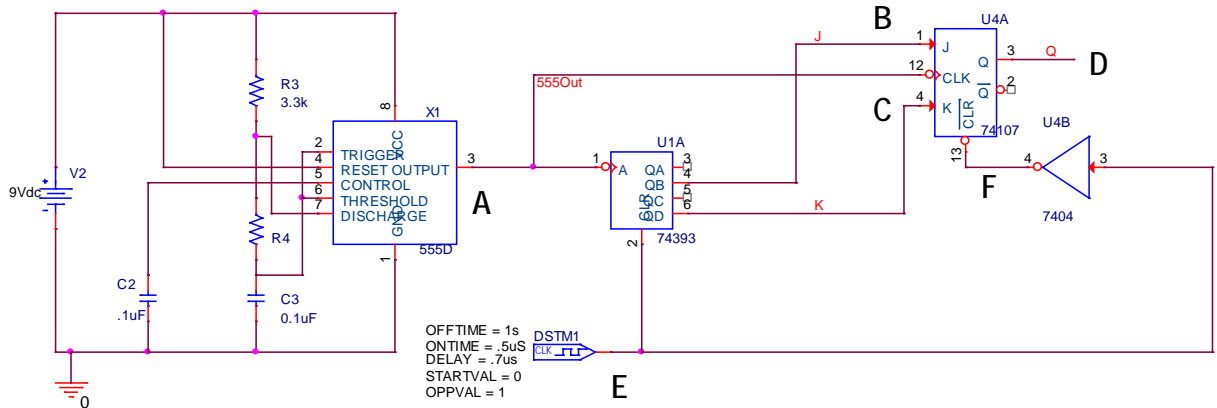
Also notice that the value of R4 is not given. Determine its value from the frequency of the clock signal produced by the 555 timer chip. To assist your calculation, two dark vertical lines have been added at t = 40ms and t = 146ms. (2 points)

22 cycles in 146-40 = 106ms gives us f = 22/106 kHz = .2075 kHz = 208Hz (anything close is OK)

J & K are just the 2nd and 4th place outputs from the counter. Q is gotten from the truth table.

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d. Finally, the output of the Flip Flop (D) is used to control a transistor switch. Note that the transistor power supply is 5V to be consistent with the usual voltage sources for the gates. On the timing diagram below, add the voltages at S1, S2, and S3. Be sure to indicate the values of the voltages. (4 Points) *Hint: The voltage at S1 will look like the final output of the previous circuit, but now the voltage level matters, not just whether or not the signal is high or low. A range of answers is acceptable for the voltage level at S1. However, be sure you explain your choice.*
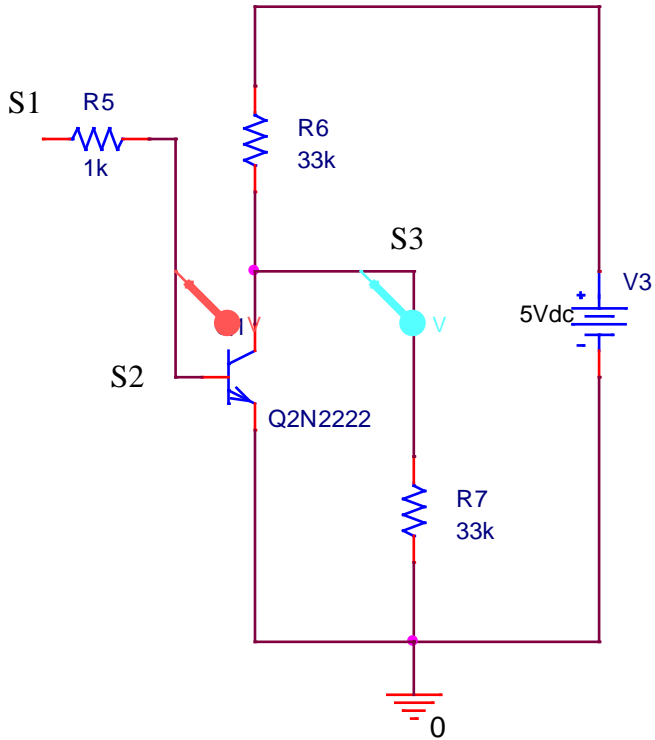
The voltage S1 is typically around 3.1 or so for Vcc = 5V. However, any value from 3-5V is fine. Ideal logic devices should go to 5V but most logic levels are around 3.3V.
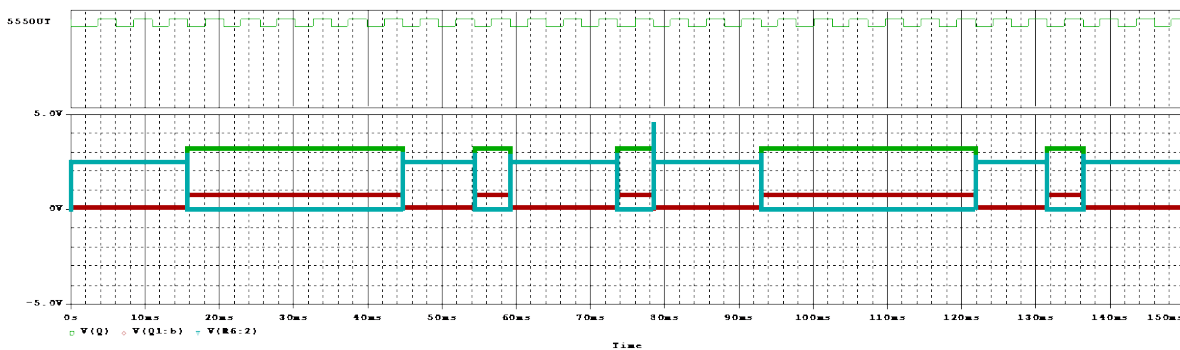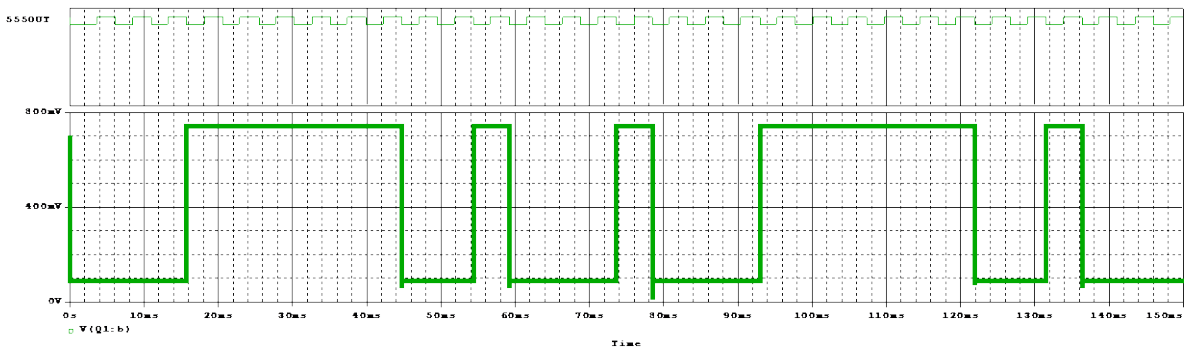

See next page for more detail.

e. In what city is the Franklin Institute located? What circuit component studied in this course is used in large numbers in an exhibit there? (5 Points) Philadelphia, LEDs.
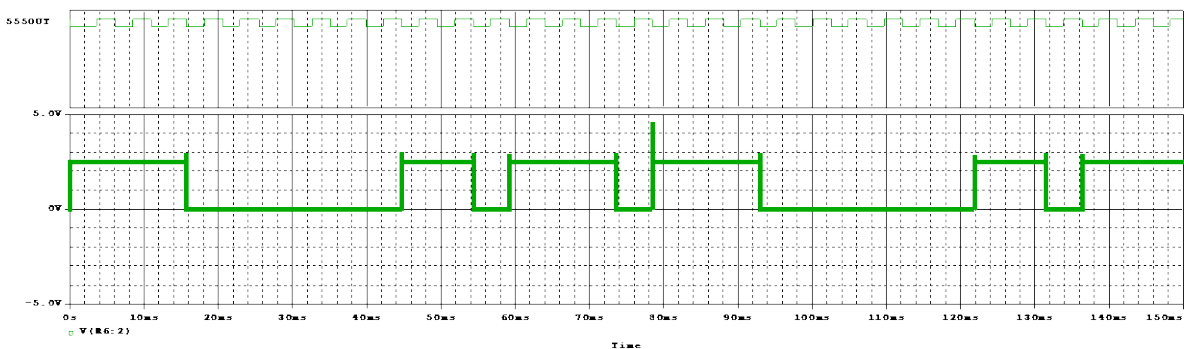
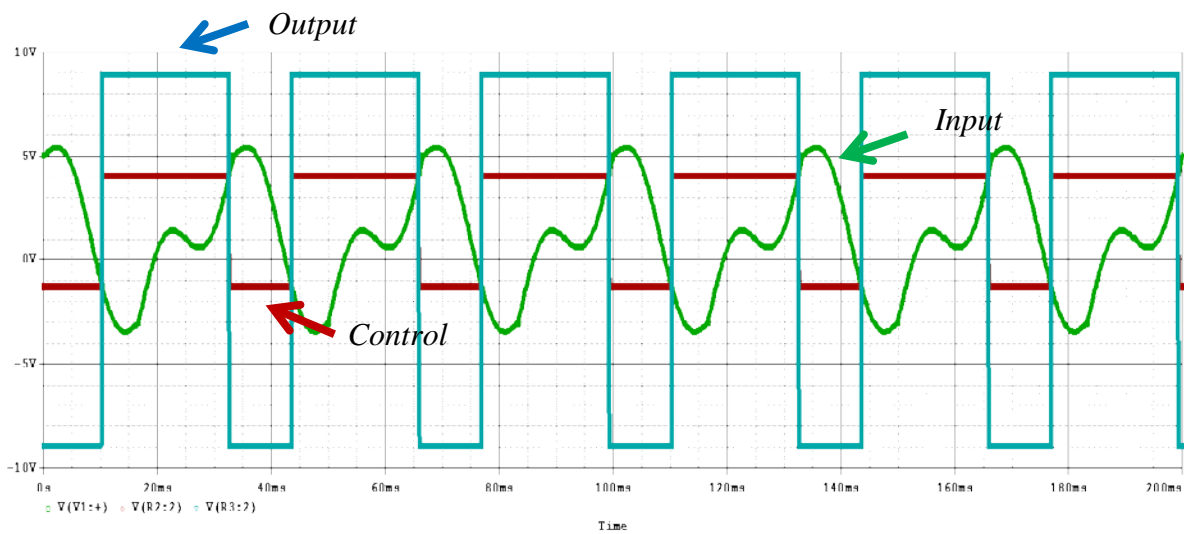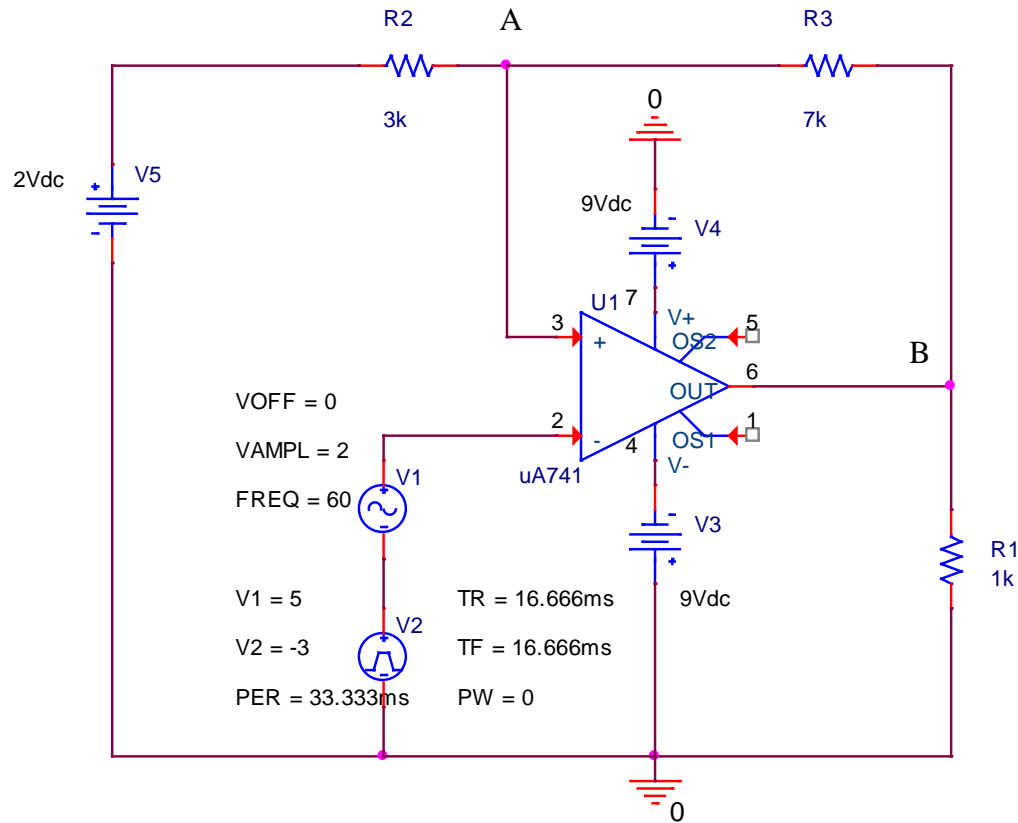*K. A. Connor*

At S1
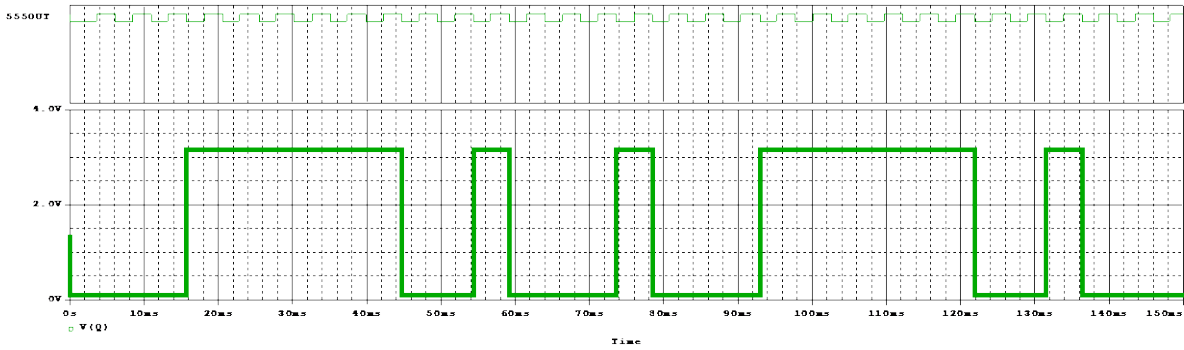
At S2

At S3

Notice that all are shaped like the output from the Flip Flop. Just the voltage amplitudes are different.
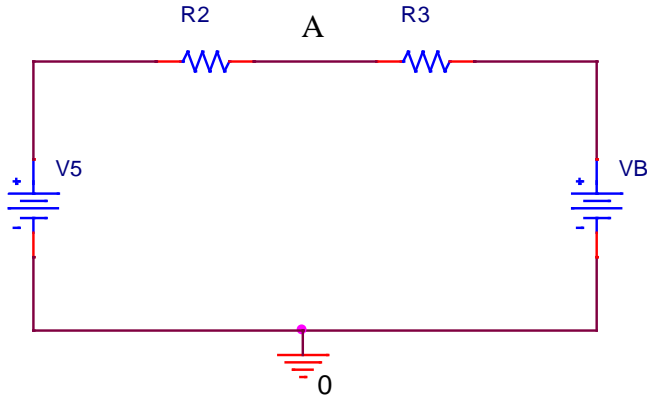
Question 4 (25 Points) Schmitt Trigger

A combination of a low frequency sine wave and a low frequency triangular wave is passed through a homemade Schmitt Trigger, as shown below along with a plot of the resulting input signal vs. time.

Blue: Output, Green: Input, Red: control voltage at point A

a. Before beginning this problem, consider the circuit below which includes only the voltage source V5 = 2V, resistors R2 = 3kΩ & R3 = 7kΩ, and an unspecified voltage source VB. Determine the voltage at node A (between the two resistors) in terms of VB and the given values of V5, R2 & R3. (4 Points)

R2   A   R3

V5   VB

Ans: this is a voltage divider, so that

$$V_A = 2Volts + \frac{R2}{R2+R3}(VB-2)Volts$$

0

The remaining questions pertain to the full Schmitt Trigger circuit.

b. Assume ideal conditions, what are the two threshold voltages for the Schmitt Trigger? (6 Points)

Ans: using the answer from part a,

$$V_{Max} = 2Volts + \frac{3}{3+7}(9-2)Volts = 2 + 2.1 = 4.1Volts$$

$$V_{Max} = 2Volts + \frac{3}{3+7}(-9-2)Volts = 2 - 3.3 = -1.3Volts$$

c. Plot the voltages at points A and B vs. time on the plot above. (8 Points) Be sure to clearly label the two voltages.

See previous page.

d. If you are using this as the input to a counter, how many positive pulses does it count per second? (5 Points)

6 per 200ms or about 30 per second.

e. What is the input impedance of the Analog Discovery oscilloscope? (2 Points) For logic devices, why do you start with $\overline{CLR}$ low and then keep it high or *CLR* high and then keep it low? (1 point) From a recent question of the day (1MΩ)

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