

ENGR-2300

Electronic Instrumentation

Quiz 3

Fall 2022

Print Name _____ **RIN** _____**Section** _____

I have read, understood, and abided by the Collaboration and Academic Dishonesty statement in the course syllabus. The work presented here was solely performed by me.

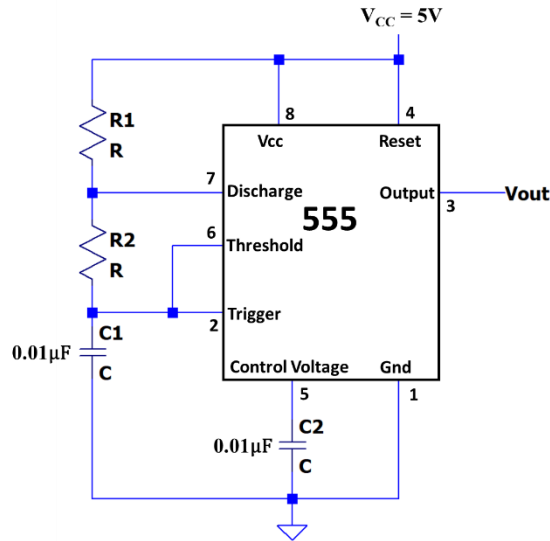
Signature: _____

Date: _____

On all questions: SHOW ALL WORK. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS. No credit will be given for numbers that appear without justification. Unless otherwise stated in a problem, provide 3 significant digits in answers. Read the entire quiz before answering any questions. Also it may be easier to answer parts of questions out of order.

I. The 555 Timer in Astable Multivibrator Configuration (20 points)

Shown below is a 555-Timer configured as an astable multivibrator, which generates a train of voltage pulses.

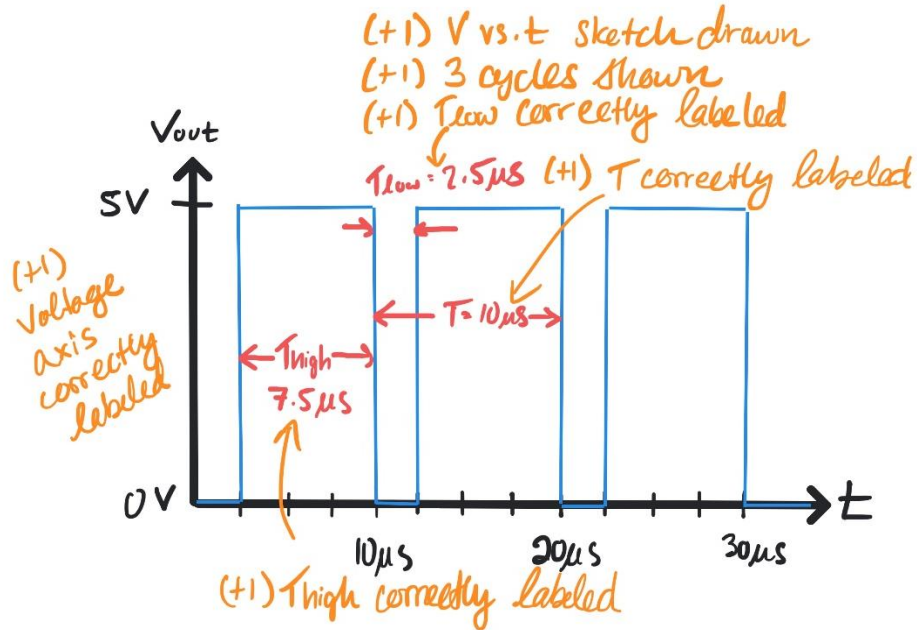


- (4 pts) You are tasked with using the 555 timer to generate a train of voltage pulses with a frequency of $f = 100 \text{ kHz}$ and a duty cycle of 75%. Calculate the total period of one cycle of pulses (T), the amount of time per cycle that the voltage output is high (T_{high}) and the amount of time per cycle that the voltage output is low (T_{low}).

- Calculation of T : $T = \frac{1}{f} = \frac{1}{100 \text{ kHz}} = 10 \mu\text{s}$ (+1) Correct formula
(+1) No math mistake

- Calculation of T_{high} : a duty cycle of 75% means that V_{out} is high for 75% of the period of the pulse, so $T_{high} = 0.75T = 0.75 \times 10 \mu\text{s} = 7.5 \mu\text{s}$ (+1) Correct formula
- Calculation of T_{low} : a duty cycle of 75% means that V_{out} is low for 25% of the period of the pulse, so $T_{low} = 0.25T = 0.25 \times 10 \mu\text{s} = 2.5 \mu\text{s}$ (+1) Correct formula

2. (6 pts) Sketch at least 3 cycles of the output voltage from the 555 timer vs. time. Label all relevant voltages, the total period (T), the time per cycle that the output voltage is high (T_{high}) and the time per cycle that the output voltage is low (T_{low}).c)



3. (4 pts) Calculate values for R_1 and R_2 to the nearest Ohm that will generate the output voltage you sketched in Q1.b.

- Calculating R_2 : $T_{low} = 0.693R_2C_1 \rightarrow R_2 = \frac{T_{low}}{0.693C_1} = \frac{2.5\mu s}{0.693 \cdot 0.01\mu F} = 361\Omega$

(+) Correct formula; (+) No math error

- Calculating R_1 : $T_{high} = 0.693(R_1 + R_2)C_1 \rightarrow R_1 = \frac{7.5\mu s}{0.693 \cdot 0.01\mu F} - 361\Omega = 721\Omega$

(+) Correct formula; (+) No math error

4. (4 pts) If you were to use this output signal to drive an LED via pulse-width modulation (PWM), what is the average voltage that is delivered to the LED over time?

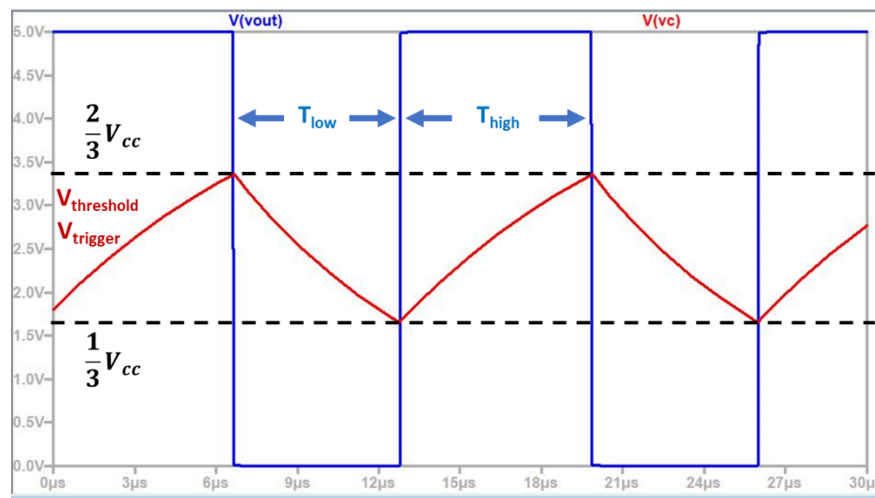
- V_{avg} for a square wave can be calculated as follows:

$$V_{avg} = \frac{V_{low}T_{low} + V_{high}T_{high}}{T} = \frac{0V \cdot 2.5\mu s + 5V \cdot 7.5\mu s}{10\mu s} = \frac{15}{4}V = 3.75V$$

(+2) A correct approach to calculating V_{avg}

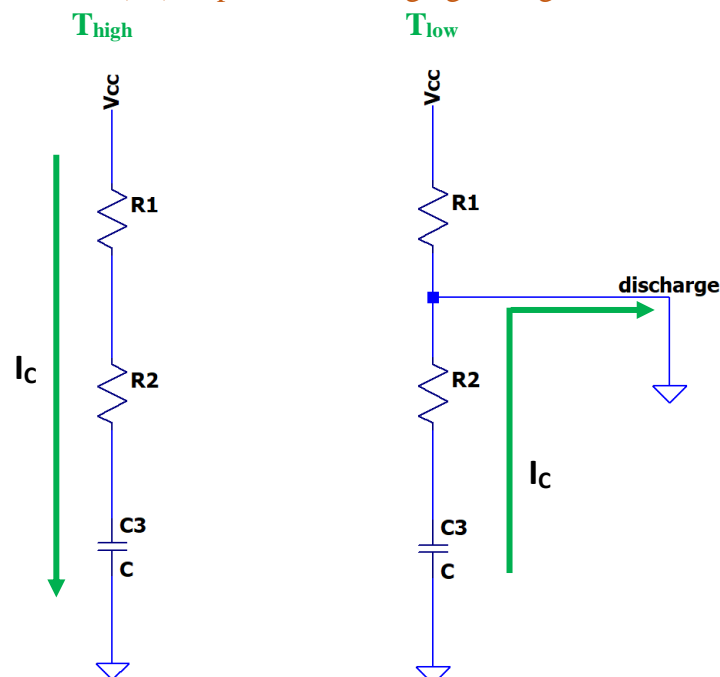
(+2) No math error

5. (2 pts) The astable multivibrator configuration of the 555 timer switches its output from high to low when $V_{\text{threshold}}$ crosses $2/3V_{cc}$ and from low to high when V_{trigger} crosses $1/3V_{cc}$, as shown below:



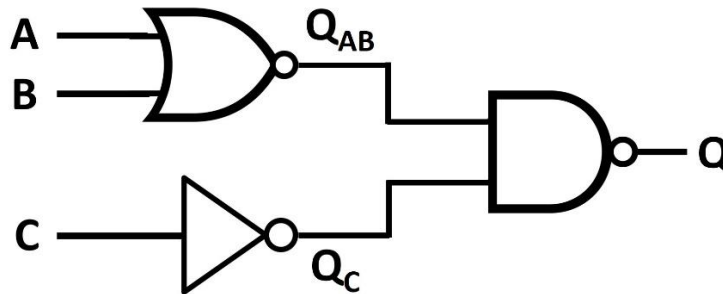
Why is T_{high} determined by $(R_1+R_2)C_1$, but T_{low} is determined by R_2C_1 ?

- T_{high} is set by the time it takes for $V_c = V_{\text{trigger}} = V_{\text{threshold}}$ to charge from $1/3 * V_{cc}$ to $2/3 * V_{cc}$, which is proportional to $(R_1+R_2)C_1$ because the capacitor is being charged via V_{cc} through R_1 and R_2 . (+) Capacitor charging through R_1 and R_2
- T_{low} is set by the time it takes for $V_c = V_{\text{trigger}} = V_{\text{threshold}}$ to discharge from $2/3 * V_{cc}$ to $1/3 * V_{cc}$, which is proportional to R_2C_1 because the capacitor is being discharged to ground via the discharge pin of the 555 timer through R_2 . (+) Capacitor discharging through R_1



II. Combinational and Sequential Digital Logic (20 points)

1. (6 pts) Write the truth table for the following logic circuit, including entries for Q_{AB} , Q_C and Q .



A	B	C	Q_{AB}	Q_C	Q
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	0	1	1
0	1	1	0	0	1
1	0	0	0	1	1
1	0	1	0	0	1
1	1	0	0	1	1
1	1	1	0	0	1

(+2) Correct table of inputs (A, B, C)

(+1) Correct Q_{AB} (NOR gate truth table)

(+1) Correct Q_C (NOT gate truth table)

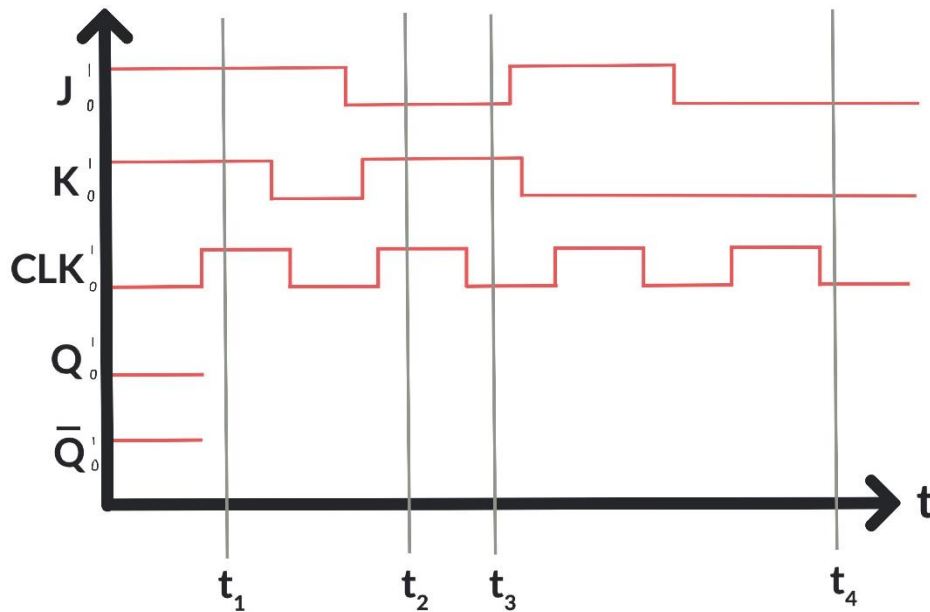
(+2) Correct Q

2. (2 pts) Which fundamental 3-input logic gate is the circuit in Q2.1 equivalent to? Explain your reasoning in one sentence.

The circuit in Q2.1 is equivalent to a **3-input OR gate**, since its output (Q) is 1 when any of the inputs (A , B or C) are 1; and the output is 0 only when all inputs are 0.

(+2) Some appropriate reasoning for determining what the gate is equivalent to, even if Q2.1 is incorrect

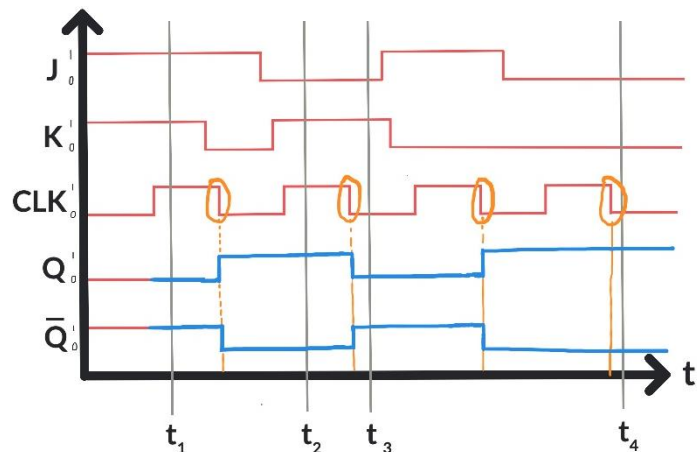
3. (6 pts) JK Flip Flop: below is the timing diagram for a JK flip-flop with the inputs **CLK**, **J** and **K** already given. Sketch **Q** and \bar{Q} vs. time and fill out the table for **Q** and \bar{Q} at the given times.



Time	J	K	Q	\bar{Q}
t ₁				
t ₂				
t ₃				
t ₄				

Solution

J	K	C	Q	\bar{Q}
0	0	p	no change	
0	1	p	0	1
1	0	p	1	0
1	1	p	toggle	



According to the truth table for the JK flip-flop:

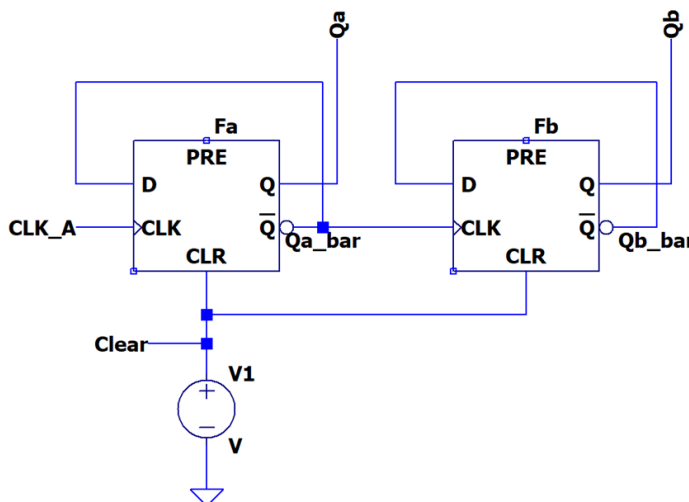
- At falling clock edge #1: $J = 1, K = 0 \rightarrow Q = 1, Qbar = 0$
- At falling clock edge #2: $J = 0, K = 1 \rightarrow Q = 0, Qbar = 1$
- At falling clock edge #3: $J = 1, K = 0 \rightarrow Q = 1, Qbar = 0$
- At falling clock edge #4: $J = 0, K = 0 \rightarrow Q = \text{No Change}, Qbar = \text{No Change}$

(+1) Q and Qbar only change on a falling clock edge
 (+1) Q and Qbar are always complements of each other

Time	J	K	Q	\bar{Q}
t ₁	1	1	0	1
t ₂	0	1	1	0
t ₃	0	1	0	1
t ₄	0	0	1	0

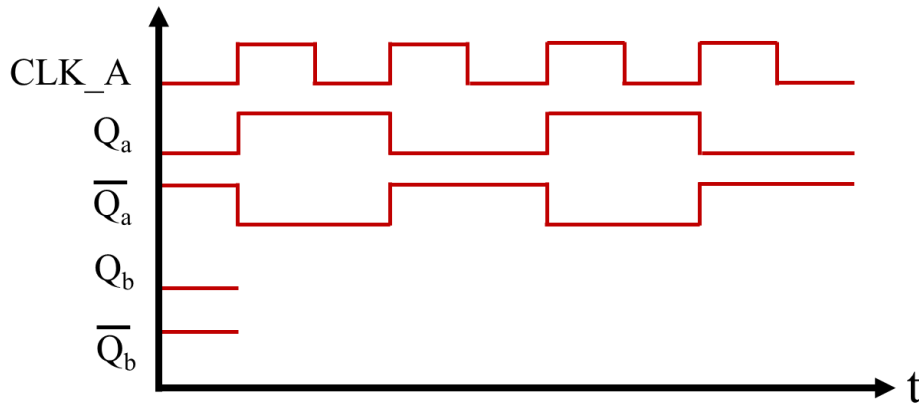
(+1) All entries for time t₁ are correct
 (+1) All entries for time t₂ are correct
 (+1) All entries for time t₃ are correct
 (+1) All entries for time t₄ are correct

4. (4 pts) The counter circuit below consists of two D flip-flops (**Fa** and **Fb**), with a clock input **CLK_A** and two outputs **Qa** and **Qb**. The D flip-flop is a *rising edge device* with the following truth table:

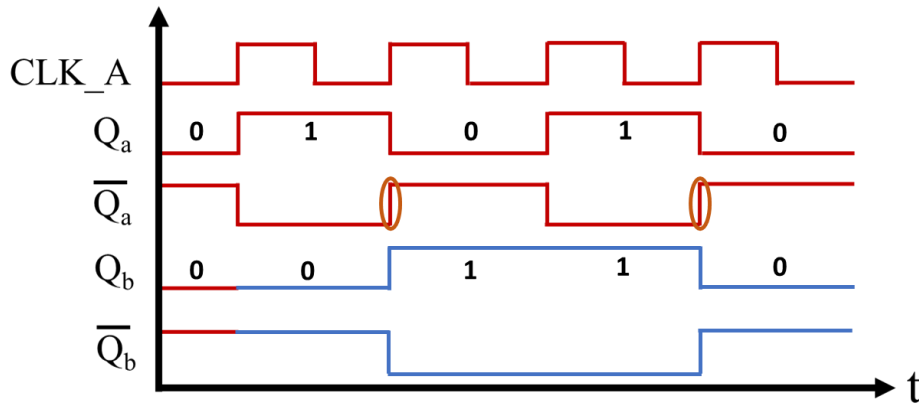


D	CLK	Q	\bar{Q}
0	Rising edge	0	1
1	Rising edge	1	0

Complete the timing diagram below by sketching the outputs Q_b and $\overline{Q_b}$ (Qb_bar).



Solution: Qa_bar acts as the CLK input to flip-flop Fb and Qb_bar is the D input to Fb, so when Qa_bar goes from low to high, Fb looks at its D input (Qb_bar), then sets Qb to whatever D is (Qb_bar). The way the circuit is configured, Qb will toggle on every rising edge of Qa_bar . This is a 2 bit counter.

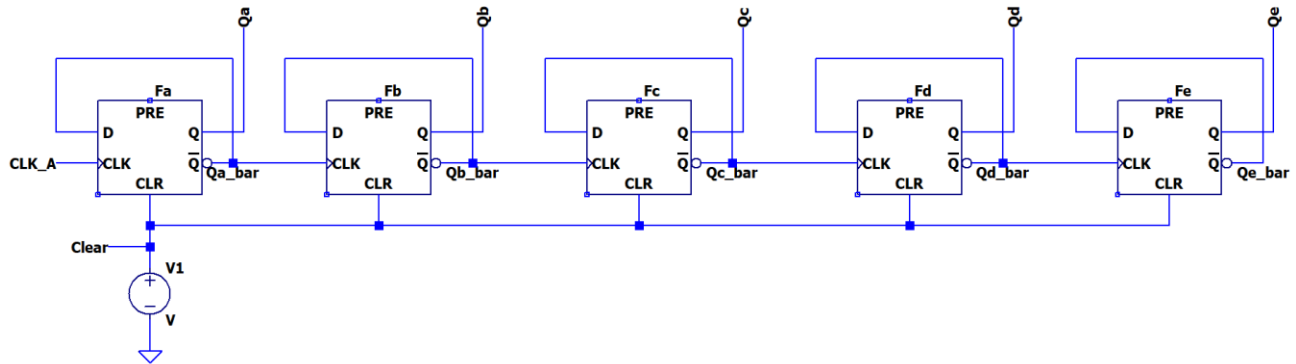


(+1) Qb and Qb_bar change only on rising edge of Qa_bar

(+1) Qb and Qb_bar are complements of each other

(+2) Correct Qb and Qb_bar

5. (2 pts) If a 3rd, 4th, and 5th D flip-flop (**Fc**, **Fd** and **Fe**) were to be added to the counter circuit in Q2.5 beyond **Fb** to provide additional outputs **Qc**, **Qd** and **Qe** to the circuit as shown below, what is the highest number this counter could represent? Give your answer in both binary (base 2) and decimal (base 10) representations.



This circuit is a 5-bit counter, which could represent a largest number (in binary) of **11111**. The decimal representation of 11111 is $1*2^0 + 1*2^1 + 1*2^2 + 1*2^3 + 1*2^4 = 1 + 2 + 4 + 8 + 16 = 31$

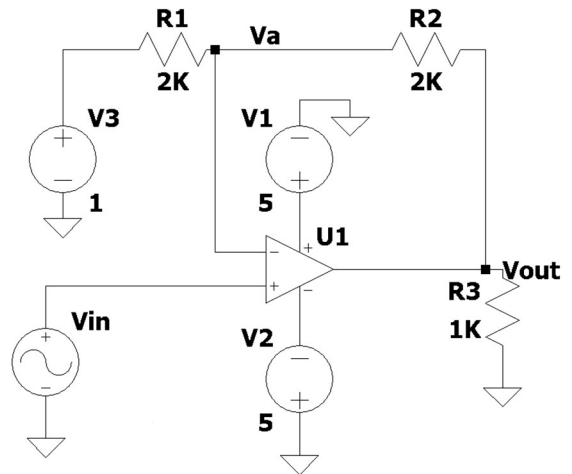
(+1) Correct binary form

(+1) Correct decimal form

III. Comparators and Schmitt Triggers (20 points)

The circuit shown is used for this problem. V1, V2 and V3 are DC voltage sources with the values shown.

V1=5V, V2=5V (resulting in -5V at the V- input) and V3=1V. Assume the output of the op-amp is capable of reaching the power supply voltages; hence it is called a **rail-to-rail op amp**.



a. (2pts) What are the two possible values of Vout?

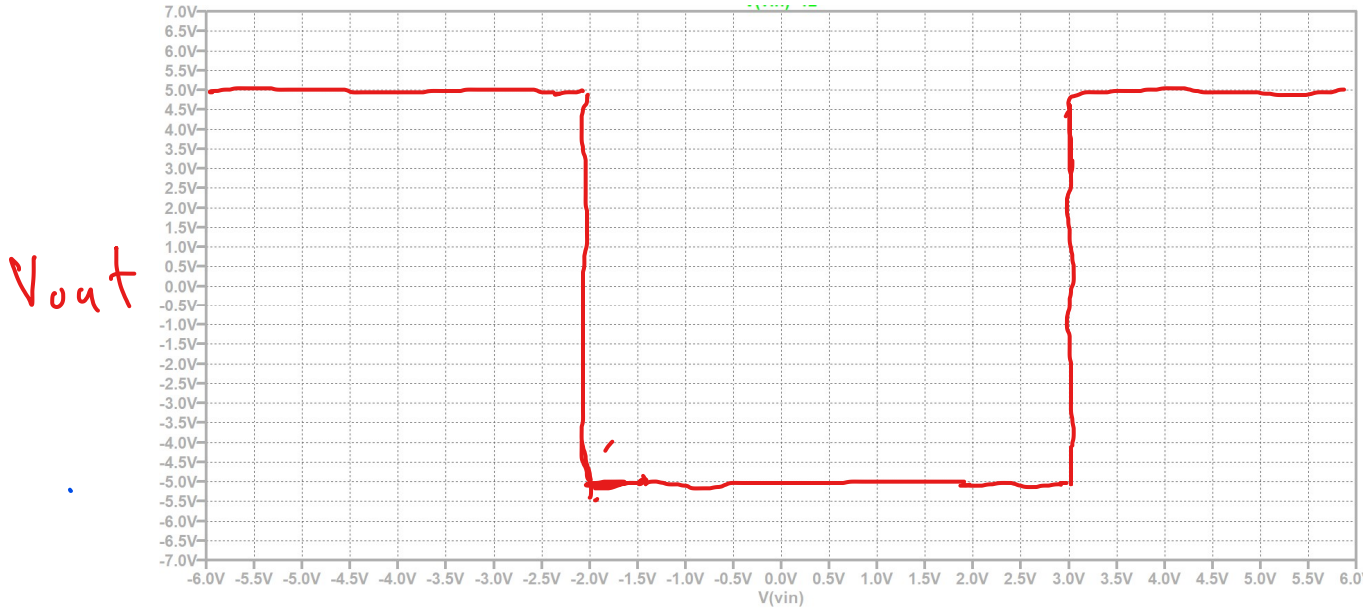
+5V, -5V

b. (4pts) What are the two possible values of Va, the voltage at the inverting node of the op amp?

$V_a = 1 + (V_{out} - 1) \frac{R_2}{R_1 + R_2}$ $V_a = 3V, -2V$

$V_a = 1 + (5 - 1) \frac{1}{2} = 3$ or $V_a = 1 + (-5 - 1) \frac{1}{2} = -2$

c. (8pts) Plot Vin vs Vout on the graph shown. Label critical voltages.



- d. (2pts) Explain how a Schmitt trigger circuit is different from a comparator circuit. (This should be a structural description, not a description of the inputs/outputs (2pts))

a comparator will switch between a high and low output at a specific voltage reference threshold. When a Schmitt trigger toggles between high and low outputs it also toggles between low and high reference thresholds, leading to hysteresis behavior.

- e. (2pts) Describe in your own words exactly how a Schmitt trigger circuit eliminates noise from an input signal.

Because a Schmitt trigger has a moving reference threshold, noise cannot repeatedly trigger a change between output high and output low unless the noise amplitude is very high.

- f. (2pts) Can you increase the noise reduction capability of the circuit shown on the previous page by changing the value of one or more of the resistors? If so, state which resistor or resistors you would change and whether you would increase or decrease their resistance.

Yes. Suppose we increased R_2 to 3k.

$$V_a = 1 + (V_{out} - 1) \frac{R_1}{R_1 + R_2}$$

$$= 1 + (V_{out} - 1) \frac{3}{5}$$

$$V_{a+} = 1 + 4 \cdot \frac{3}{5} = 3.4$$

$$V_{a-} = 1 - 6 \cdot \frac{3}{5} = -2.6$$

difference in thresholds has increased from

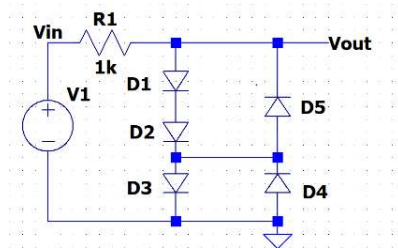
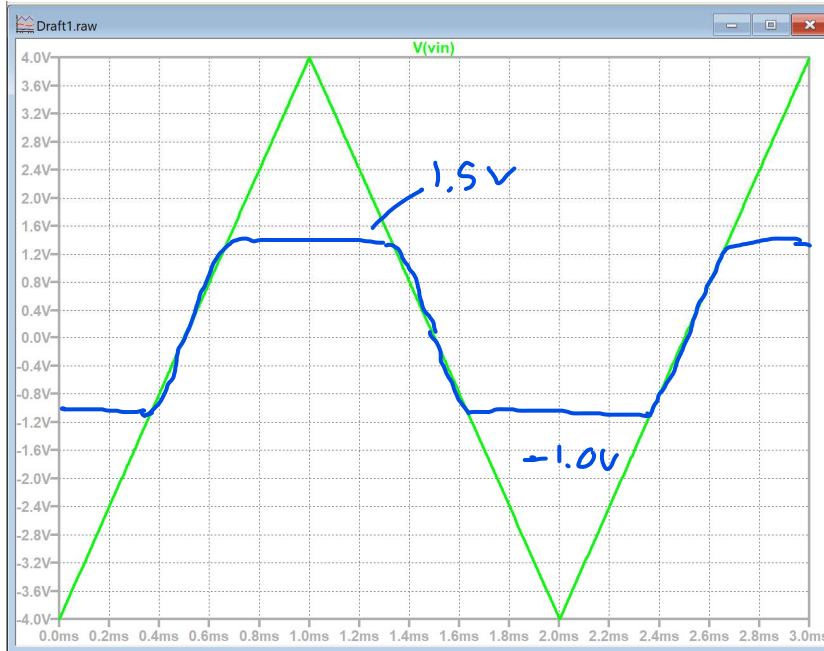
$$3 - (-2) = 5$$

to

$$3.4 - (-2.6) = 6$$

IV – Diodes (20 points)

- a. (4pts) The graph shows $V_1(t)$ for the circuit shown. Draw $V_{out}(t)$ on the graph using the V_{on} Model with $V_{on}=0.5V$. Label important voltages.



$$V_{D1} + V_{D2} + V_{D3} = 1.5V$$

$$V_{D4} + V_{D5} = 1.0V$$

- b. (2pt) A diode is found to have $I_S=4 \times 10^{-11}A$. Find V_D , the diode voltage when $I_D=200mA$ at room temperature and if $n=1$. Use the diode equation. Hint: assume that the -1 term is insignificant when solving for V_D but then go back and show if it was appropriate to make that assumption about the “-1” term.

$$I_D = I_S \left(e^{\frac{V_D}{nV_T}} - 1 \right)$$

$$0.2A = (4 \times 10^{-11}) \left(e^{\frac{V_D}{V_T}} \right)$$

$$V_T = 25.9 \times 10^{-3}$$

$$e^{\frac{V_D}{V_T}} = e^{\frac{0.57}{25.9 \times 10^{-3}}} \gg 1$$

$$\rightarrow V_D = 0.578V$$

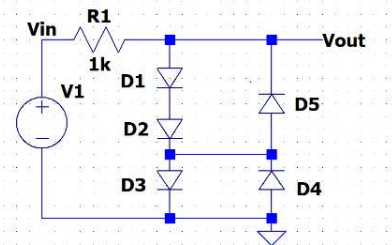
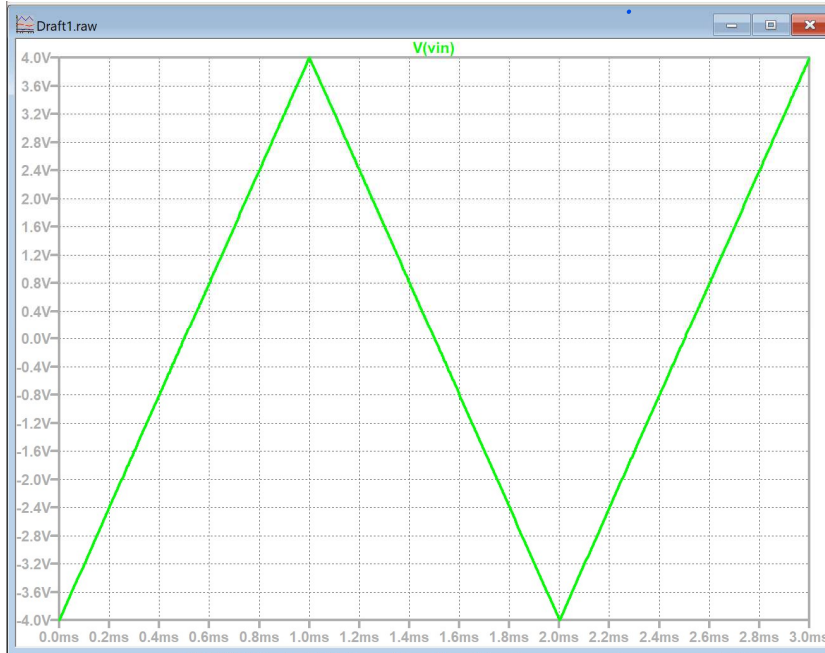
- c. (2pt) Calculate the power flowing through the diode in part b.

$$P = IV \quad I = 200mA$$

$$V_D = 0.578$$

$$P = 0.11W$$

- d. (3pts) Rectifier diodes: For the circuit shown, R1 is the load and the voltage across R1 is V_{out} . Use the Von diode model with $V_d=0.5V$. Sketch V_{out} . V_1 is already plotted.



repeat from part a

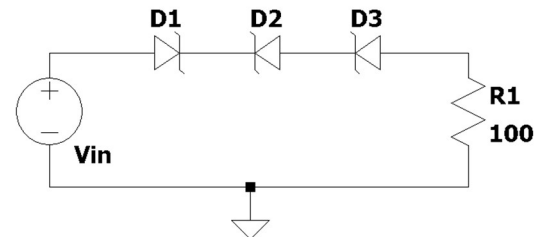
- e. (2 pts) Describe in your own words how the behavior of Zener diodes is different from that of other diodes.

Zener diodes have a relatively low reverse breakdown voltage.

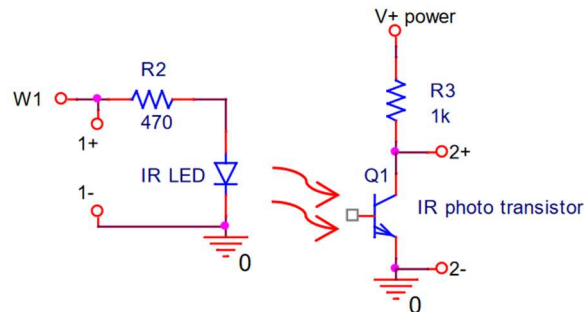
- f. (3 pts)

In the diagram at right, is there some voltage V_{in} that will cause current to flow in R1? Explain why or why not.

Yes. $V_{in} \geq V_d$ of D1 + V_z of D2 + V_z of D3.



- g. (2 pts) Suppose that another student has built the following circuit from Experiment 8.



The student shows you an input and output waveform and claims that the output waveform represents the phototransistor responding to the IR LED. Describe one way you can verify that this is true without modifying the circuit.

place an optical block between the IR LED and phototransistor.

- h. (2 pts) In addition to being used to generate light, can light-emitting diodes also be used to build rectifier circuits? Explain why or why not?

Yes. In their IV characteristics they behave the same as LEDs that don't emit light.