ENGR-2300

Electronic Instrumentation

Quiz 3

Spring 2017

Name ____Solution____________

Section ___

Question 1 (20 Points) ___________

Question 2 (20 Points) ___________

Question 3 (20 Points) ___________

Question 4 (20 Points) ___________

LMS Question is worth an additional 20pts

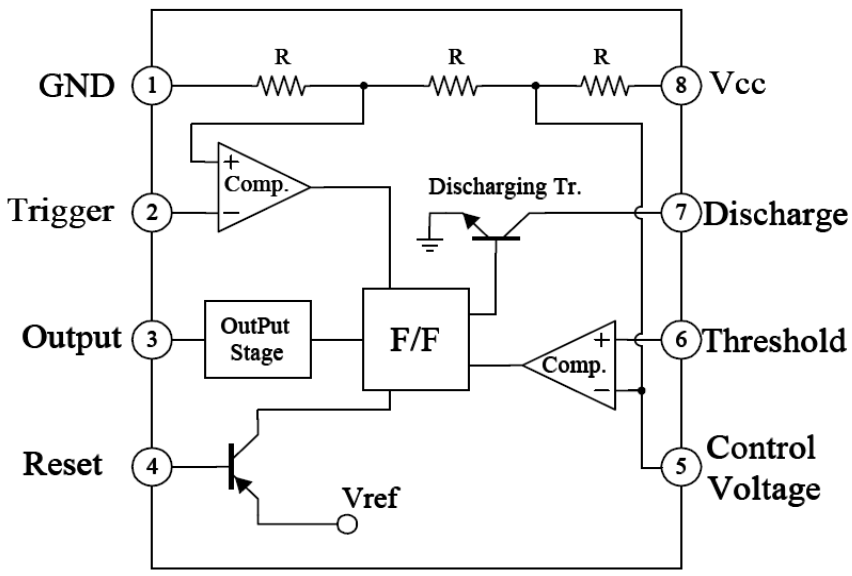
Total (80 points) ______________

On all questions: **SHOW ALL WORK**. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS. No credit will be given for answers that appear without justification. Read the entire quiz before answering any questions. Also it may be easier to answer parts of questions out of order.

Some Additional Background plus

Standard Resistor Values (±5%)						
1.0	10	100	1.0K	10K	100K	1.0M
1.1	11	110	1.1K	11K	110K	1.1M
1.2	12	120	1.2K	12K	120K	1.2M
1.3	13	130	1.3K	13K	130K	1.3M
1.5	15	150	1.5K	15K	150K	1.5M
1.6	16	160	1.6K	16K	160K	1.6M
1.8	18	180	1.8K	18K	180K	1.8M
2.0	20	200	2.0K	20K	200K	2.0M
2.2	22	220	2.2K	22K	220K	2.2M
2.4	24	240	2.4K	24K	240K	2.4M
2.7	27	270	2.7K	27K	270K	2.7M
3.0	30	300	3.0K	30K	300K	3.0M
3.3	33	330	3.3K	33K	330K	3.3M
3.6	36	360	3.6K	36K	360K	3.6M
3.9	39	390	3.9K	39K	390K	3.9M
4.3	43	430	4.3K	43K	430K	4.3M
4.7	47	470	4.7K	47K	470K	4.7M
5.1	51	510	5.1K	51K	510K	5.1M
5.6	56	560	5.6K	56K	560K	5.6M
6.2	62	620	6.2K	62K	620K	6.2M
6.8	68	680	6.8K	68K	680K	6.8M
7.5	75	750	7.5K	75K	750K	7.5M
8.2	82	820	8.2K	82K	820K	8.2M
9.1	91	910	9.1K	91K	910K	9.1M

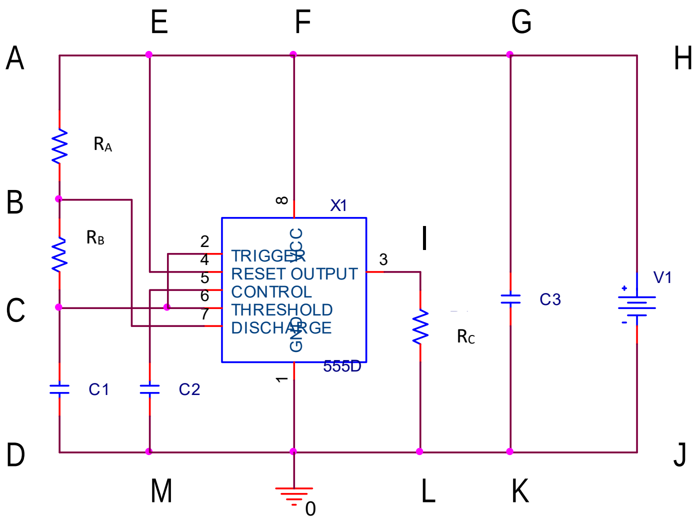
555 Timer Block Diagram



Zener Diodes: From Wikipedia: A **Zener diode** is a diode which allows current to flow in the forward direction in the same manner as an ideal diode, but also permits it to flow in the reverse direction when the voltage is above a certain value known as the breakdown voltage, "zener knee voltage", "zener voltage", "avalanche point", or "peak inverse voltage".
The device was named after Clarence Zener, who discovered this electrical property. Many diodes described as "zener" diodes rely instead on avalanche breakdown as the mechanism. Both types are used. Common applications include providing a reference voltage for voltage regulators, or to protect other semiconductor devices from momentary voltage pulses.

Type Number	Nominal Zener Voltage V_Z @ I_{ZT}[3] (Volts)	Test Current I_{ZT} (mA)	Maximum Zener Impedance Z_{ZT} @ I_{ZT}[1] (Ω)	Maximum Regulator Current I_{ZM}[2] (mA)	Maximum Reverse Leakage Current	
					$T_A = 25°C$ I_R @ $V_R = 1V$ (μA)	$T_A = 150°C$ I_R @ $V_R = 1V$ (μA)
1N746A	3.3	20	28	110	10	30
1N747A	3.6	20	24	100	10	30
1N748A	3.9	20	23	95	10	30
1N749A	4.3	20	22	85	2	30
1N750A	4.7	20	19	75	2	30
1N751A	5.1	20	17	70	1	20
1N752A	5.6	20	11	65	1	20
1N753A	6.2	20	7	60	0.1	20
1N754A	6.8	20	5	55	0.1	20
1N755A	7.5	20	6	50	0.1	20
1N756A	8.2	20	8	45	0.1	20
1N757A	9.1	20	10	40	0.1	20
1N758A	10	20	17	35	0.1	20
1N759A	12	20	30	30	0.1	20

Question 1 (20 Points) Astable Multivibrator (An Iconic 555 Timer Application)



a. (4pts) A 555 timer, astable multivibrator is built as shown with R_A = unknown, R_B = unknown, $R_C = 33k\Omega$, $C1 = 10\mu F$, $C2 = 0.01\mu F$, $C3 = 330\mu F$, and V1 = 9V. Determine the ratio of resistors R_A/R_B that will produce a duty cycle of 60%.

Duty Cycle = T1/T

$(R_A+R_B)/(R_A+2R_B) = 0.6$

$R_A+R_B = 0.6R_A + 1.2R_B$

$0.4R_A=0.2R_B$

$\mathbf{R_A/R_B = 1/2}$

b. (4pts) Using this ratio of R_A/R_B, calculate the values for R_A and R_B needed to yield a frequency of 20Hz.

$R_B = 2R_A$

$f = 1.44/(R_A + 2R_B)C1$

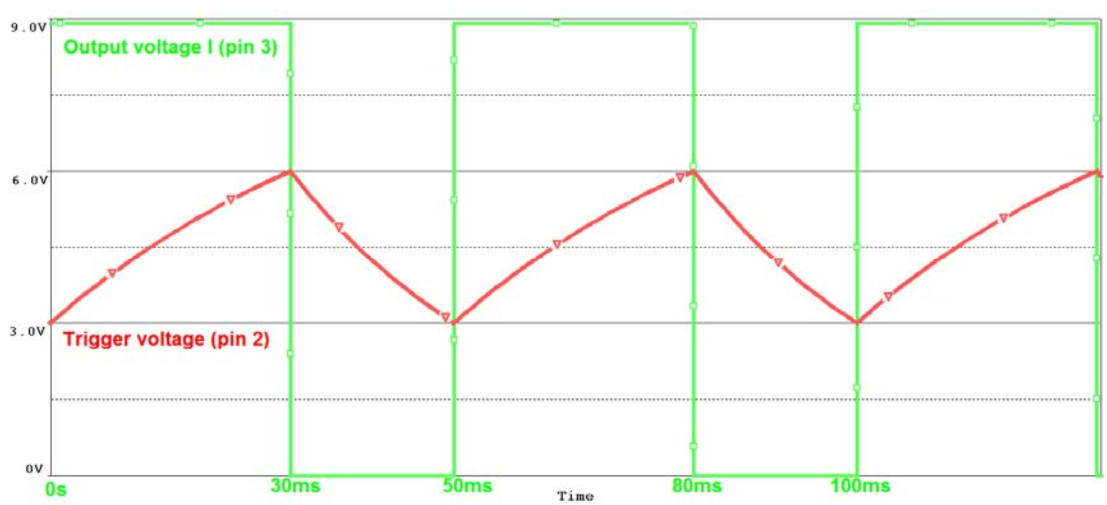
$f = 1.44/(R_A + 2(2R_B))C1$

$20 = 1.44/(5R_A)(10\mu)$

$\mathbf{R_A = 1.44k\Omega}$

$\mathbf{R_B = 2.88k\Omega}$

c. (3pts) Plot the output voltage (**I**) below, showing at least two full cycles, starting with the output voltage at its maximum (assume = 9V). Label the horizontal and vertical scales.



d. (3pts) Determine the maximum and minimum voltages at pins 6 (C). List the values and add a trace to the plot for part c. above for this voltage. Assume that the circuit is in steady state. You may want to look at the background information at the beginning of this exam.

Trigger at 1/3rd and 2/3rd of V1 (9V)
Vmin = 3V and Vmax = 6V

e. (2pts) The capacitors used for this project are inexpensive and have a large tolerance band of +10% and -5%. This means the actual capacitance can be 10% greater than the labeled value or 5% less than that value. Determine the maximum and the minimum period that this circuit might have given this tolerance band.

T = 1/f = 1/20 = 50 ms
When C1 is 10% greater than labeled value, **Tmax = 1.1 x 50 ms = 55 ms**
When C1 is 5% less than labeled value, **Tmin = 0.95 x 50 ms = 47.5 ms**

f. (1pt) List the answer you found for R_A and R_B in part b. on the previous page. The background information provided list standard 5% resistor values. Now list the values you would use for R_A and R_B to build the actual circuit, trying to stay as close to the design timing. Use only one resistor for each of R_A and R_B .

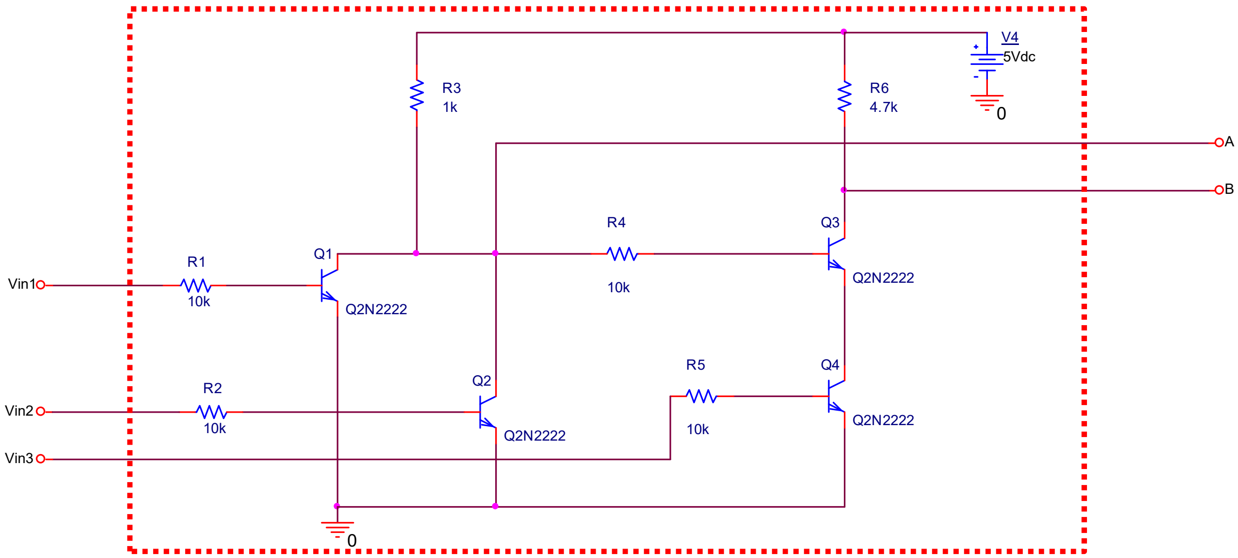
R_A = 1.44 kΩ → use **R_A = 1.5 kΩ**
R_B = 2.88 kΩ → use **R_B = 3 kΩ**

g. (3pts) What is the **on time** (T1), **off time** (T2), and **duty cycle** of the circuit in part f. ?

T1 = 0.693(R_A + R_B)C1 = 0.693(4.5k)10μ = 31.185 ms
T2 = 0.693(R_B)C1 = 0.693(3k)10μ = 20.79 ms
Period T = T1 + T2 = 51.975 ms
Duty cycle = T1/T = 60%

Question 2 (20 Points) Combinational & Sequential Logic Circuits

a. (8pts) The circuit below shows how a simple logic gates can be built out of transistors and resistors. The circuit is inside the dashed box and has three inputs and two outputs. Voltages above 2.5V are logic high and voltages below 2.5V are logic low.



i. (6pts) Complete the table below using logic levels of 0 and 1, not the actual voltages.

Vin1	Vin2	Vin3	A	B
0	0	0	**1**	**1**
0	0	1	**1**	**0**
0	1	0	**0**	**1**
0	1	1	**0**	**1**
1	0	0	**0**	**1**
1	0	1	**0**	**1**
1	1	0	**0**	**1**
1	1	1	**0**	**1**

A = Vin1 **NOR** Vin2 B = A **NAND** Vin3

ii. (2pts) What type of logic gate does output A represent? What logic gate computes B from A and Vin3?

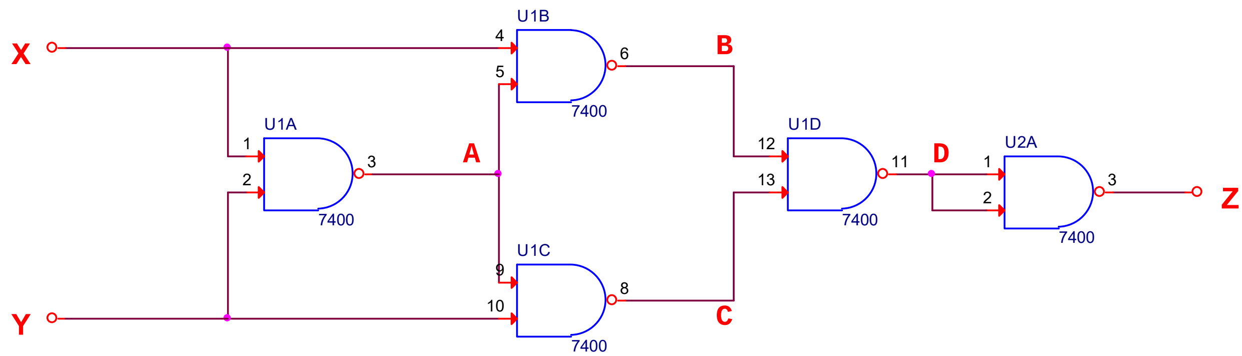
A represents a **NOR** gate
NAND gate computes B from A and Vin3

b. (2pts) A 4-bit counter had an initial state listed as the start state in the table below, and then receives a string of clock pulses. What are QA, QB, QC and QD after 7 clock pulses? Clearly indicate the state of each signal.

	QD	QC	QB	QA
Start state	1	1	0	1
State after 7 counts	**0**	**1**	**0**	**0**

1101 (binary) = 13 (decimal)
Counting sequence starting 13 is 14, 15, 0, 1, 2, 3, 4 … 4 (decimal) = 0100 (binary)

c. (4pts) Complete the truth table below for the following circuit. You need to complete the last column but you **must also support your answer** by computing the logic levels at the four intermediate points in circuit.

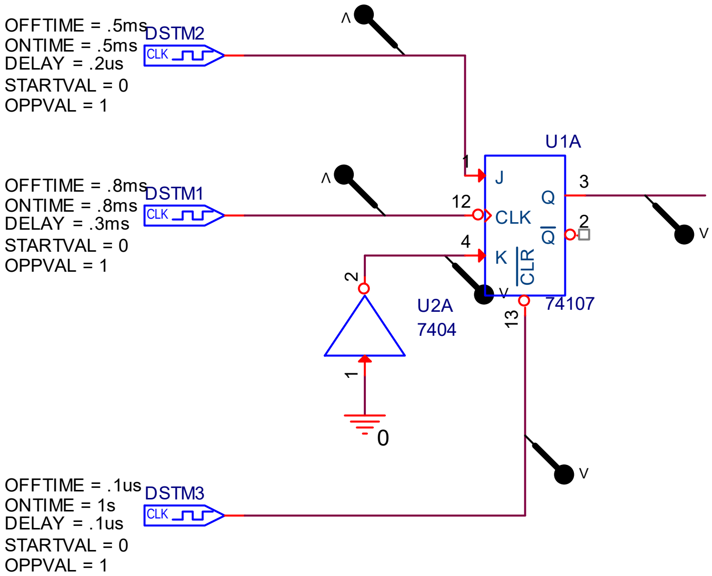


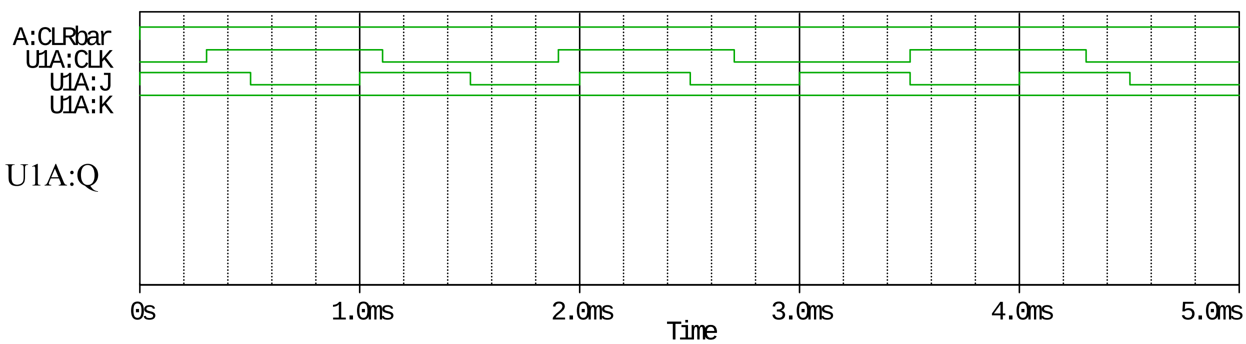
X	Y	A	B	C	D	Z
0	0	**1**	**1**	**1**	**0**	**1**
0	1	**1**	**1**	**0**	**1**	**0**
1	0	**1**	**0**	**1**	**1**	**0**
1	1	**0**	**1**	**1**	**0**	**1**

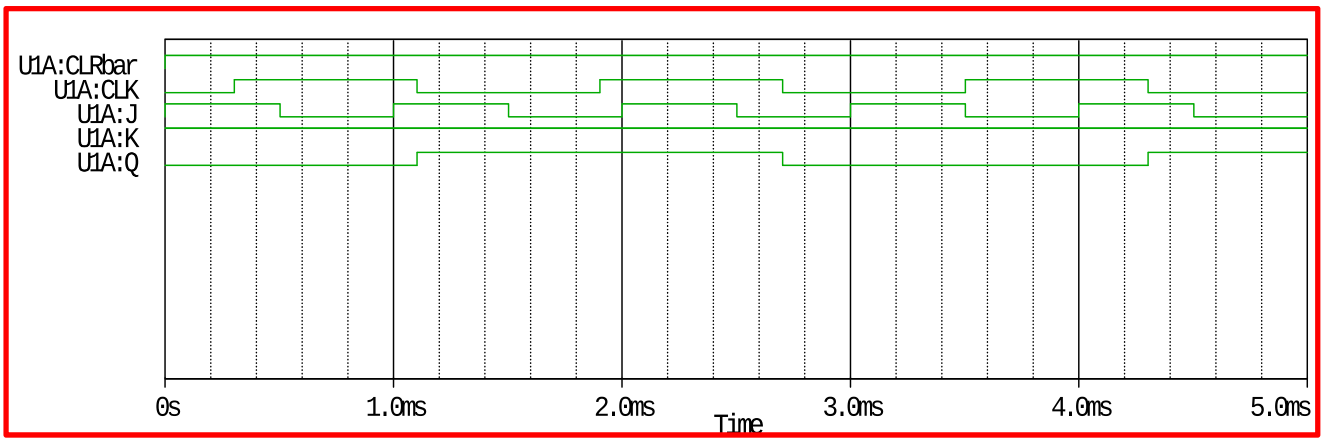
d. (1pt) Given the input values of X and Y, and the corresponding intermediate output D, what logic gate would give the same output (D)?

XOR

e. (5pts) The following is a diagram of one flip flop. Remember that flip flops trigger on the falling edge of the clock pulse. The timing diagram demonstrates the J, K, and clock pulses given. Determine the output Q and write it on the timing diagram. Q starts out low.







First falling edge of clock pulse: J=1; K=1→ JK flip-flop in toggle state→ Q toggles from 0 to 1
Second falling edge of clock pulse: J=0; K=1→ reset state→ Q becomes 0
Third falling edge of clock pulse: J=1; K=1→ toggle state→ Q toggles from 0 to 1