ENGR-4300

Electronic Instrumentation

Quiz 3

Spring 2012

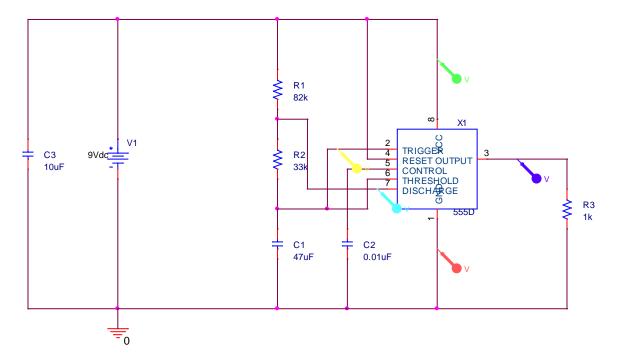
Name _____

Section ____

| Question I (16 points) |
|--------------------------|
| Question II (18 points) |
| Question III (18 points) |
| Question IV (16 points) |
| Question V (16 points) |
| Question VI (16 points) |
| Total (100 points) |

On all questions: SHOW ALL WORK. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES <u>AND UNITS</u>. No credit will be given for numbers that appear without justification or plots without clear labels. Be sure to indicate the values on your plots since drawing exact signals is not always easy.

Question I: Astable Multivibrator (16 points)



1. (4 pts) The 555 timer circuit shown has R1=82k, R2=33k, C1=47 μ F, C2=0.01 μ F, R3=1k, and C3=10 μ F. What is the period of the oscillation produced by this configuration?

 $T = 0.693(R1 + 2R2)C1 = 0.693(82k + 66k)47\mu = 4.82s$

Note that this is also consistent with the plot shown on the next page.

2. (4 pts) What is the duty cycle of the oscillation?

$$DutyCycle = \left(\frac{R1 + R2}{R1 + 2R2}\right) = 78\%$$

Note that this is also consistent with the plot shown on the next page.

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3. (4 pts) For an ideal 555, what are the maximum and minimum voltages on pin 2 above during normal operation?

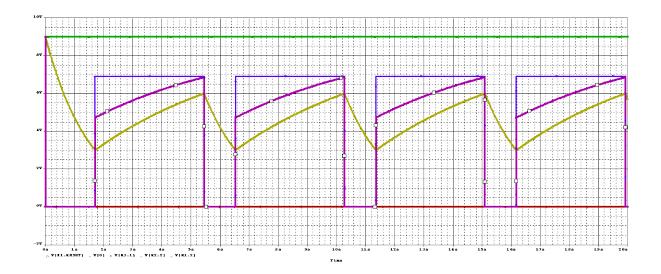
3V and 6V

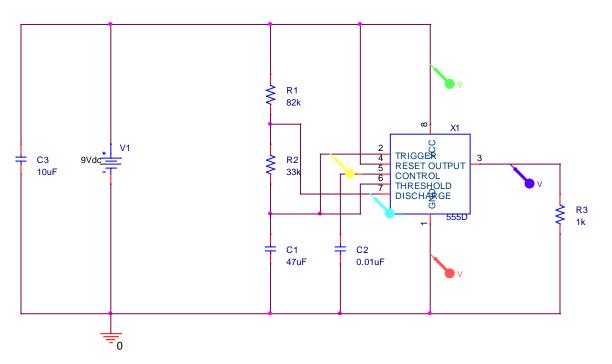
4. (4 pts) For an ideal 555, what are the maximum and minimum voltages on pin 7 above during normal operation?

The minimum is zero when pin 7 is shorted to ground.

The maximum is 6V plus the contribution from the voltage divider from 6V to 9V or

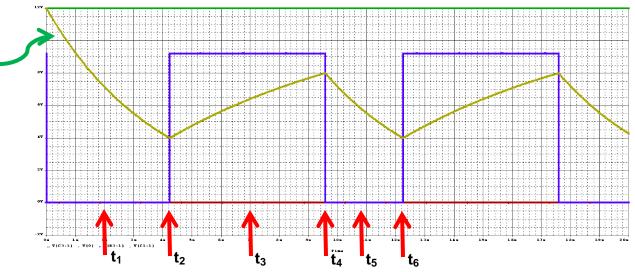
$$6V + \left(\frac{33}{82 + 33}\right)3V = 6.86V$$



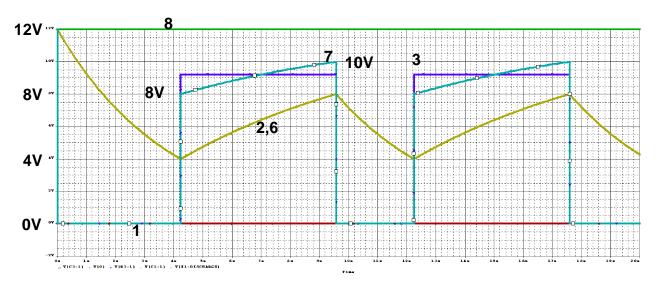


Question II: Astable Multivibrator (18 points)

The circuit addressed in Problem I is changed slightly. The voltage of the DC source (V1) is changed to 12V and R1 and R2 now are the same value of resistance. What we do not know is whether they are both $82k\Omega$ or both $33k\Omega$. What we do know is that the voltages at four of the five locations shown above are:



1. (4 pts) The plot above shows the voltages on 4 of the pins for the circuit above. The vertical scale goes from -2V to 12V and the horizontal scale goes from 0s to 20s. Label each signal with the pin number and carefully sketch over each voltage so that they are easier to identify. Label key values on each plot.



2. (4 pts) From the information given in the plot, determine the values of R1 and R2.

The duty cycle will be the same for both choices so we need to look at the period. The period is about 8s which is larger than the period for problem I and thus the resistors must both be the larger values or $82k\Omega$

3. (6 pts) Next, draw the voltage on the remaining pin of the circuit above and label it with its pin number. First solve for the voltages at the six times marked with straight arrows then use this information to produce your plot. Also, give the values for the times.

 $V(t_1) = V(2) = 0$

$$V(t_2) = V(4.2) = 8V$$

 $V(t_3) = V(7) = 9V$ (approx.)

 $V(t_4) = V(9.6) = 10V$

 $V(t_5) = V(10.8) = 0$

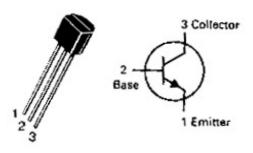
 $V(t_6) = V(12.2) = 8V$

3. (4 pts) For the curve marked with the curved arrow, find the mathematical expression that accurately describes the signal for the time period from t = 0 to $t = t_2$.

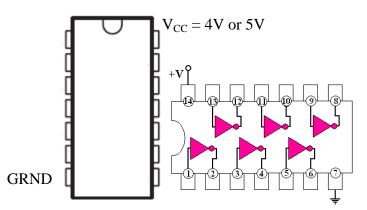
This is an exponential curve starting at 12V and dropping to 4V at 4.2s. Thus the exponential function is $V(t) = 12e^{-t/\tau}$ where $\tau = 3.8s$.

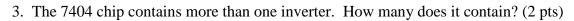
Question III: Practical Circuit Issues & Relays (18 points)

1. Shown is the symbol for an npn transistor and a picture of one of the packages it comes in (the one we used, actually). This is the figure used in Experiment 6, except that the identifying numbers on the transistor symbol have been removed. Add the numbers to the figure. (2pts)



Like op-amps, IC chips need two power connections in order to function. Label the power (Vcc) and ground pins on the 7404 IC chip pictured below with the appropriate *voltage values*. (2 pts)





There are 14 total pins. Two are used for power, leaving 12. Thus, six total inverters.

4. You've primarily used two types of capacitors in the studio: electrolytic and ceramic disc, with examples of each shown below:

Electrolytic:

Ceramic Disc:

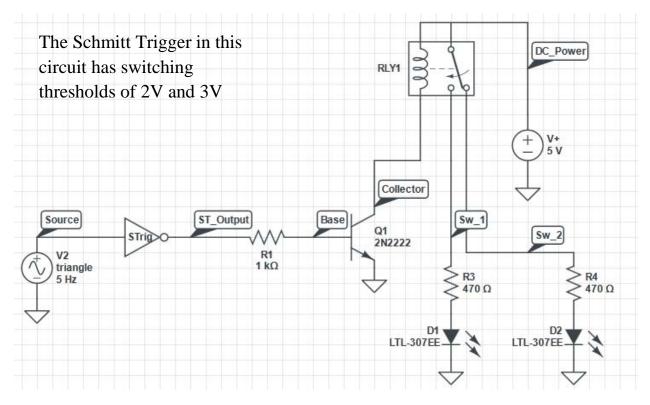


Which one usually has the larger value of capacitance? (2 pts) *Electrolytic*

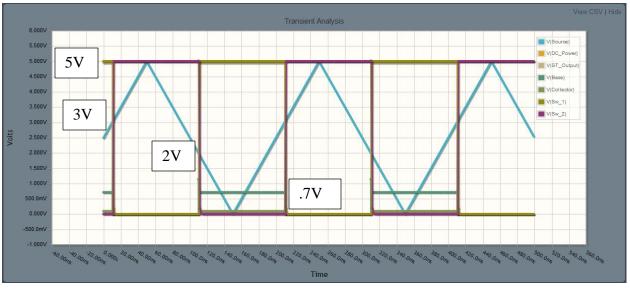


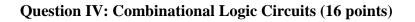
Question II: Practical Circuit Issues & Relays (continued)

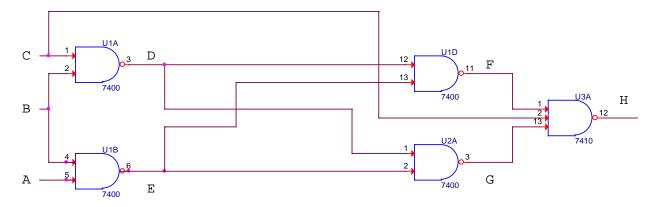
5. There is a free, browser-based Spice program (<u>https://www.circuitlab.com</u>) that can also be used to analyze the circuits we build and study in EI. Shown below is the circuit diagram for a configuration similar to the relay circuit in Experiment 6. Shown also is the **Source** voltage and the **DC Power** voltage for the circuit, both plotted as functions of time.



Sketch and carefully label the other five voltages. The vertical scale is -0.5V to 5.5V. Indicate the voltage values at key points in each plot. (10pts)







1. Complete the table below for the circuit above. (8 pts)

| Α | B | С | D | Ε | F | G | Н |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

2. A logic circuit similar to that in a) (but NOT the same) has the following truth table. Combining CD as a 2-bit binary number, fill in the decimal value in the table. (4 pts)

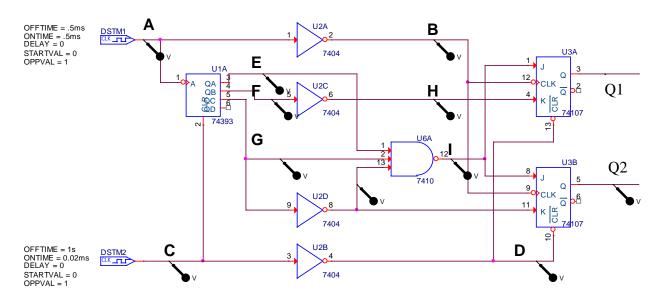
| Α | B | С | D | CD as Decimal Number |
|---|---|---|---|----------------------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 2 |

4. If A and B are treated as binary number inputs, what **Arithmetical** operation is being performed in creating the output CD? (4 pts)

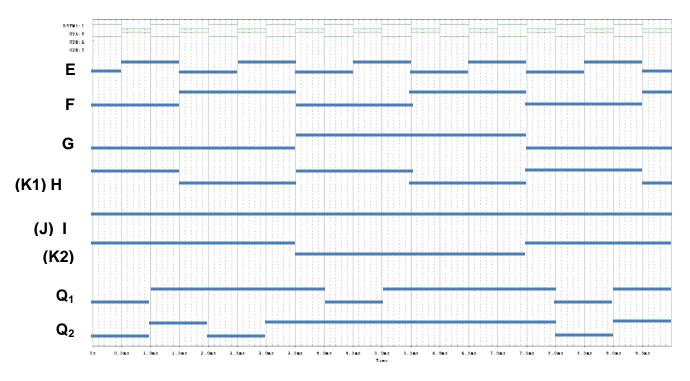
Adding

Question V: Sequential Logic Circuits (16 points)

You are given the following circuit DSTM1 provides the clock for the counter. $\overline{DSTM1}$ provides the clock to the two flip flops. DSTM2 provides an initial reset pulse to all the sequential chips. Therefore, you can assume that QA, QB, QC, QD, Q1, and Q2 are all initially low.

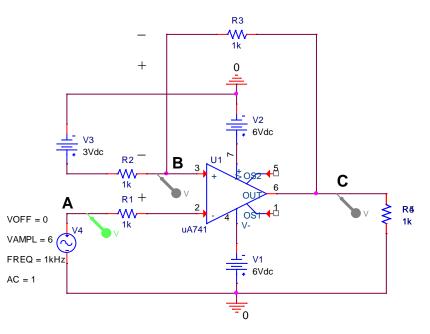


Sketch the timing trace for each of the signals shown. The first 4 signals (A, B, C, D) are given. You need to draw the remaining 7. (E, F, G, H, I: 2pts each, $Q_1 \& Q_2$: 3pts each)









1. What is the reference voltage of the Schmitt trigger model? (2 pts)

3V

2. If the op-amp is putting out its maximum voltage at C, what is the voltage at point B, the non-inverting input to the op-amp? (2 pts)

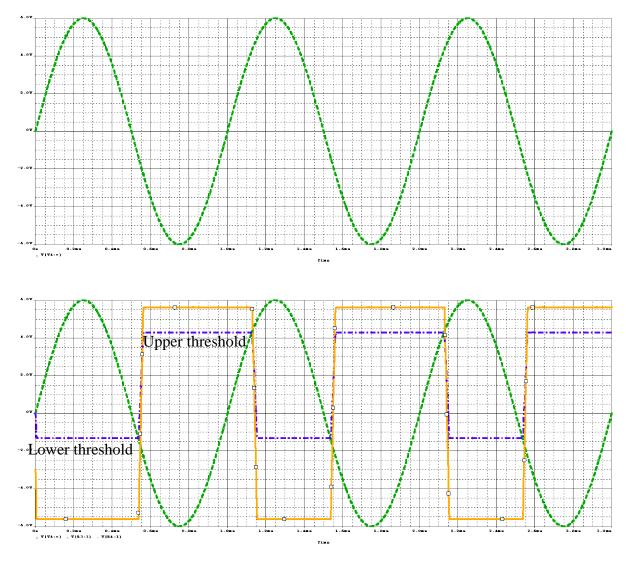
3V + (1/2)3V = 4.5V... this answer is slightly too large because the actual max voltage is a little less than 6V. See the plot on the next page.

3. If the op-amp is putting out is minimum voltage at point C, what is the voltage at point B, the non-inverting input to the op-amp? (2 pts)

3V - (1/2)9V = -1.5V... this answer is slightly too small (in magnitude) because the actual min voltage is a little less than -6V. See the plot on the next page.

- 4. On the following plot, the input at point A is shown.
 - a) Mark the upper and lower thresholds of the hysteresis (2 pts), and
 - b) Sketch and label the voltage at points B & C for the input shown. (8 pts)

Be sure to clearly label the plots so they can be easily recognized by the grader. Indicate key values for each voltage signal.



Note that the max and min are close to 6V and -6V but not quite.