ENGR-4300

Electronic Instrumentation

Quiz 3

Fall 2010

Name _____ Section ____

*You are to complete 5 questions. Question VI is required. You may select any four of the first five questions. You **must** indicate which of the questions you wish to be graded by placing an X in the selection box in the table below. If you do not, you will be penalized 5 points.*

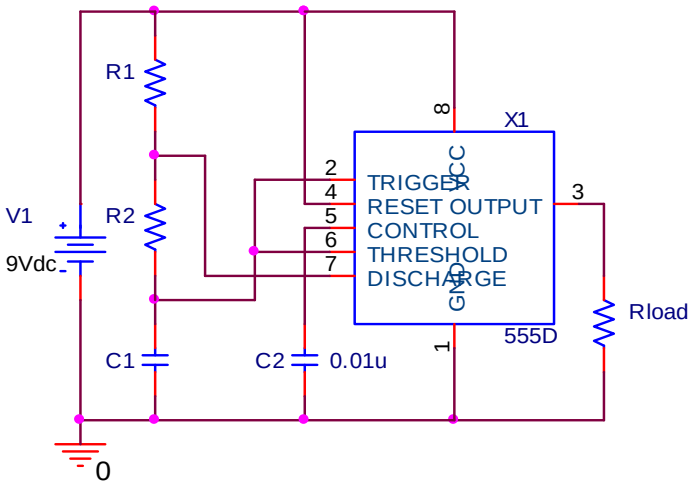
Select	Question	Value	Grade
	I	20	
	II	20	
	III	20	
	IV	20	
	V	20	
X	VI	20	

Total (100 points) _____

On all questions: SHOW ALL WORK. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS. No credit will be given for numbers that appear without justification. Provide as much explanation as possible so that partial credit can be given if appropriate.

Question I – Astable Multivibrator (20 points)

1. (4pt) The 555 timer circuit shown is to have a duty cycle of 75% (3/4). For a given C1, what ratio of resistors R1/R2 will produce this duty cycle



Duty cycle is $\frac{R_1 + R_2}{R_1 + 2R_2} = 0.75$ or R_1 *is twice* R_2.

2. (4pt) Using a ratio from above and C1 = 1μF, calculate the values for R1 and R2 needed to yield a frequency of 440Hz.

Frequency is $f = \frac{1.44}{(R_1 + 2R_2)C} = 440$ or $R_1 = 1637\Omega$ and $R_2 = 818\Omega$

3. (2pt) For an ideal 555, what are the maximum and minimum voltages on pin 2 above during normal operation?

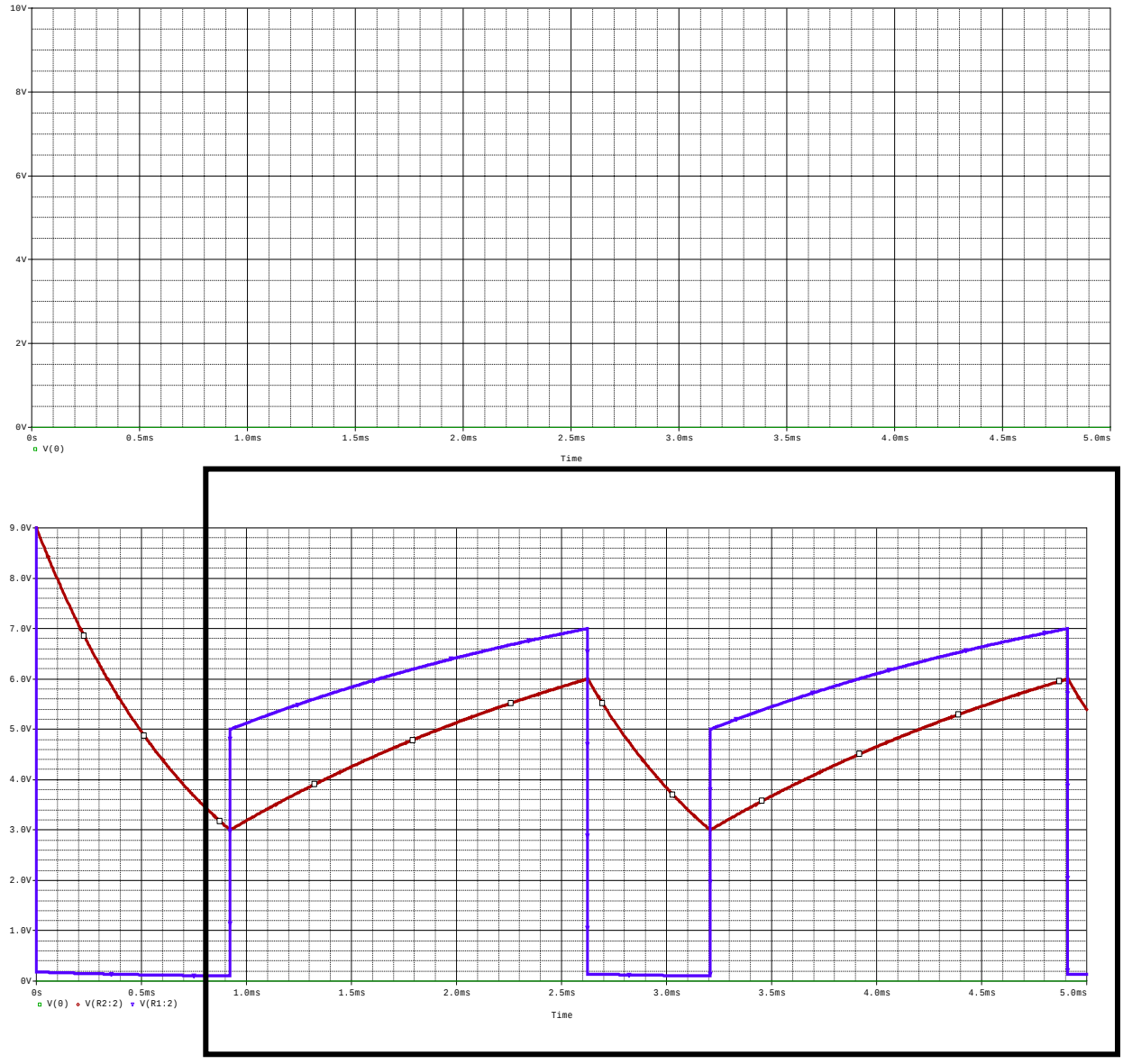
Vmin = 1/3 V1 = 1/3 x 9 =3V **Vmax = 2/3 V1 = 2/3 x 9 =6V**

4. (4pt) For an ideal 555, what are the maximum and minimum voltages on pin 7 above during normal operation?

Vmin = ground =0V **Vmax = R2/(R2+R1)x(9 - 6) + 6 = (1/3)(3)+6 = 7V**

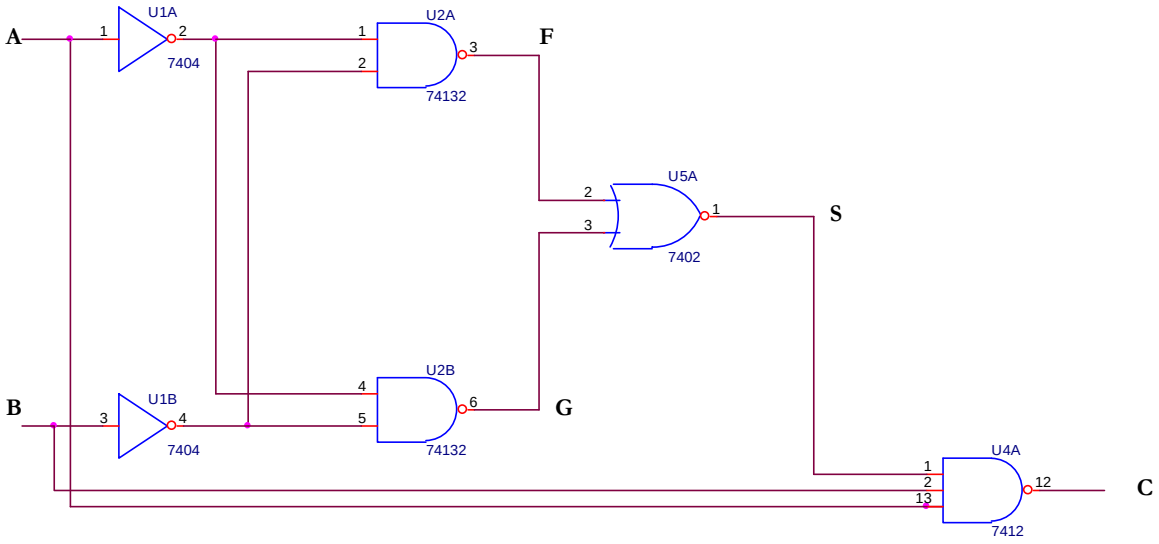
Question I – Astable Multivibrator (continued)

5. (6pt) Plot on the axes below the voltages on pins 2 and 7 of the circuit above and be sure to label each. *HINT: you may want to find the Duty Cycle first.*



PSpice was used to generate the plot. Only the part in the box is required for this answer. The first part of the signal is an artifact of the way PSpice initializes voltages.

Question II – Combinational Logic Circuits (15 points)



1. Complete the table below for the circuit above (***4 pts***: all or nothing, continuation of mistakes will be deducted)

A	B	F	G	S	C
0	0				
0	1				
1	0				
1	1				

A	B	Anot	Bnot	F	G	S	C
0	0	1	1	0	0	1	1
0	1	1	0	1	1	0	1
1	0	0	1	1	1	0	1
1	1	0	0	1	1	0	1

2. A logic circuit (NOT the same as above) has the following truth table. Combining bits RST as a 3-bit binary number, fill in the decimal value in the table (***4 pts***)

A	B	C	R	S	T	RST as a Decimal Number
0	0	1	0	0	1	
0	1	1	0	1	0	
1	0	1	0	1	0	
1	1	1	0	1	1	

Question II – Combinational Logic Circuits (continued)

A	B	C	R	S	T	RST as a Decimal Number
0	0	1	0	0	1	1
0	1	1	0	1	0	2
1	0	1	0	1	0	2
1	1	1	0	1	1	3

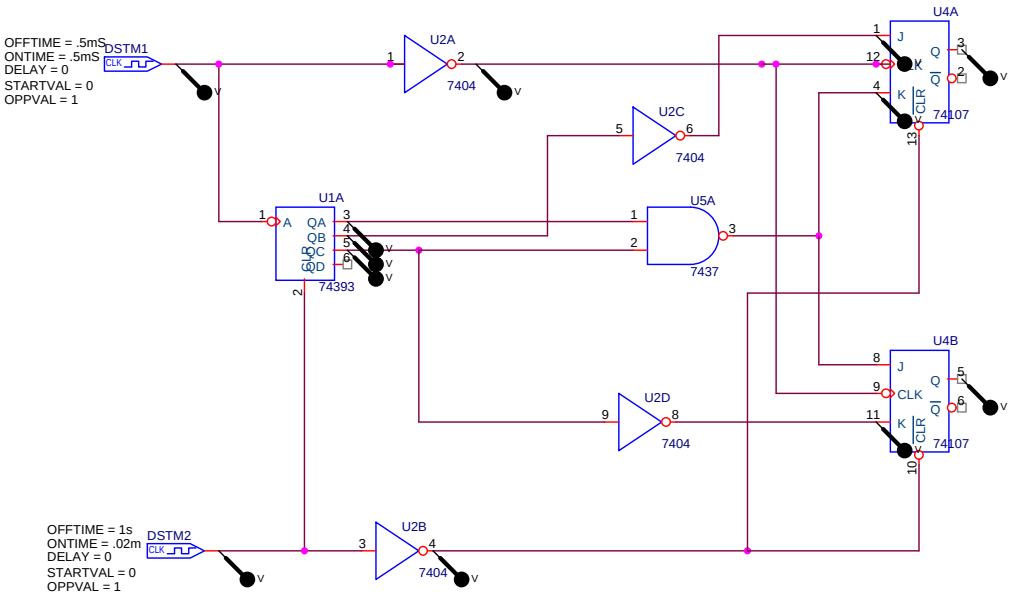
3. If A, B, and C are treated as 1-bit binary number inputs, what ARITHMATIC operation is being performed in creating the output RST? (***4 pts***: continuation of mistake above will be deducted)

Addition

4. Of the basic 2-input logic gates, which could be used for the ARITHMATIC multiply operation of 1-bit binary numbers A and B. (***3 pts***)

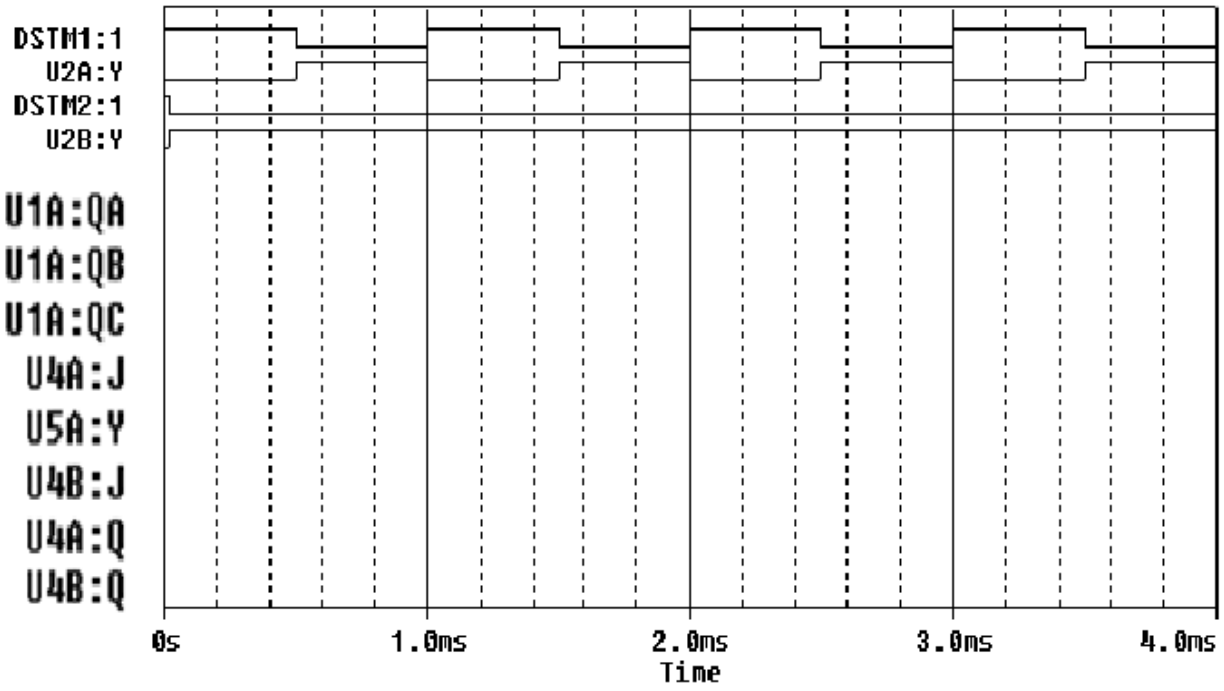
AND

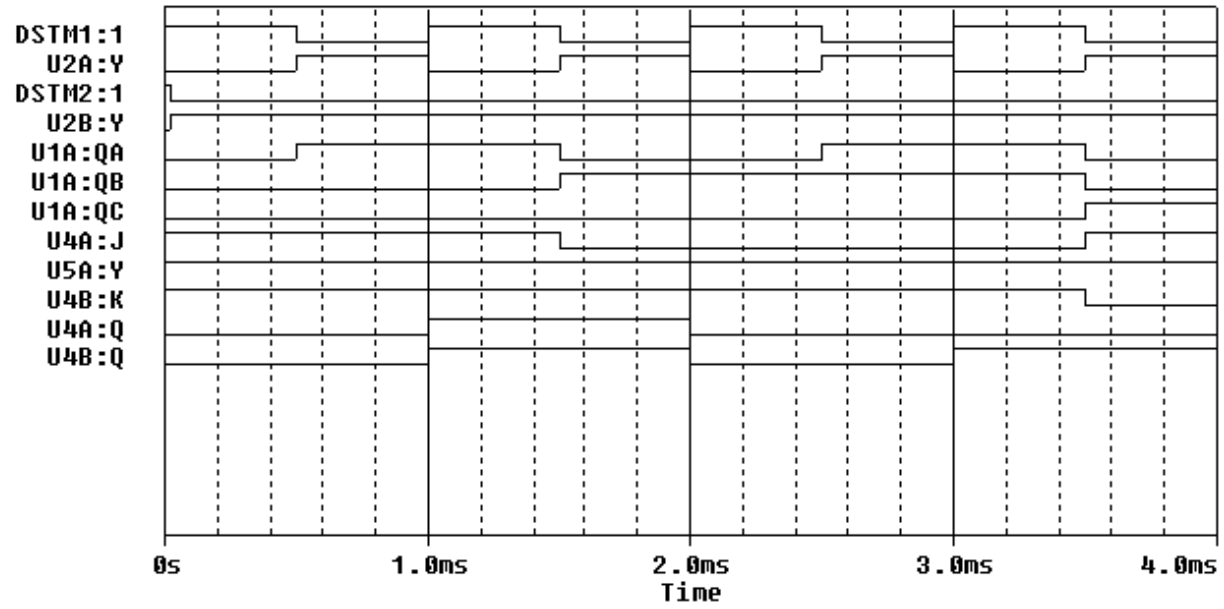
Question III – Sequential Logic Circuits (20 points)



In the circuit pictured above, clock DSTM1 provides a clock signal to a counter and two flip flops. The flip flops are clocked one half cycle after the counter to allow for propagation of the signals through the gates. (The counter changes on the negative edge of DSMT1 and the flop flops change on the negative edge of U2A:Y.) DSTM2 provides an initial reset pulse to both chips. This is required by PSpice to ensure that all sequential devices start in a known state.

1. The timing diagram below shows the reset pulses and the clock signals. Sketch the following signals in the space provided: the output from the counter (U1A:QA, U1A:QB, & U1A:QC); the output from the combinational logic (U2C:Y=U4A:J, U5A:Y=U4A:K=U4B:J, & U2D:Y=U4B:K); and the output from the flip flops (U4A:Q & U5A:Q). (2 pts per trace = ***16 pts***)





2. A 4-bit counter is cleared and then receives a string of clock pulses. What are QA, QB, QC and QD after 11 clock pulses? Clearly indicate the state of each signal. (***2 pts***)

QD	QC	QB	QA

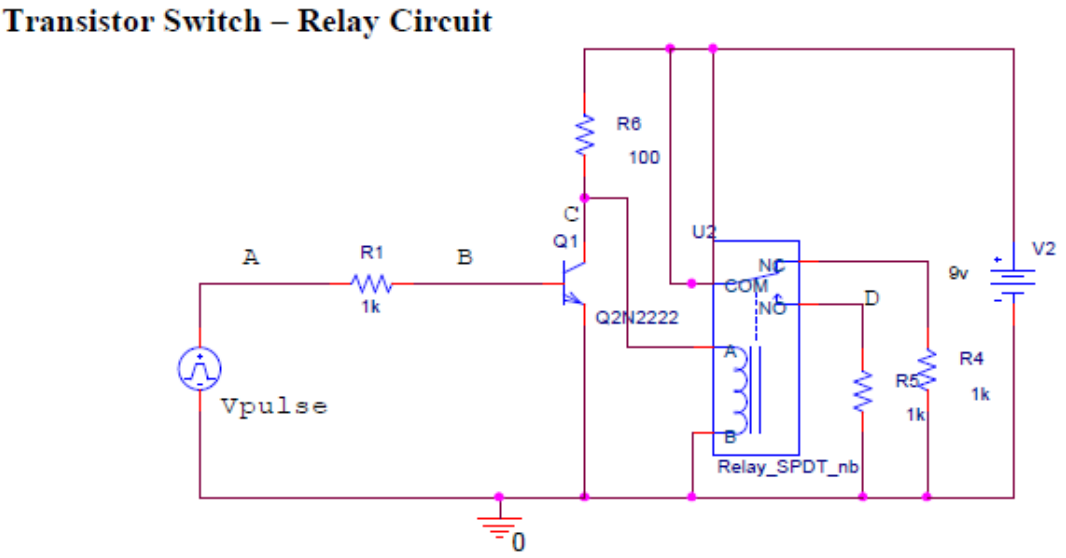
QD	QC	QB	QA
1	0	1	1

3. A 4-bit counter is cleared and then receives a string of clock pulses. What are QA, QB, QC and QD after 21 clock pulses? Clearly indicate the state of each signal. (***2pts***)

QD	QC	QB	QA

QD	QC	QB	QA
0	1	0	1

Question IV – Switching Circuits (20 points)



In the circuit above, the voltage source Vpulse puts out a sequence of pulses and the voltages at the source and three other points are monitored (marked A, B, C, and D). The relay model used by PSpice lists ***the resistance of the coil to be 100 ohms*** (***This is important!***):

1. If Vpulse is off:

   a) What is the voltage at point D? (***1 pt***) Explain why (circuit drawing with comments) (***1 pt***).

   b) What is the voltage at point C? (***1 pt***) Explain why (circuit drawing with comments) (***1 pt***).

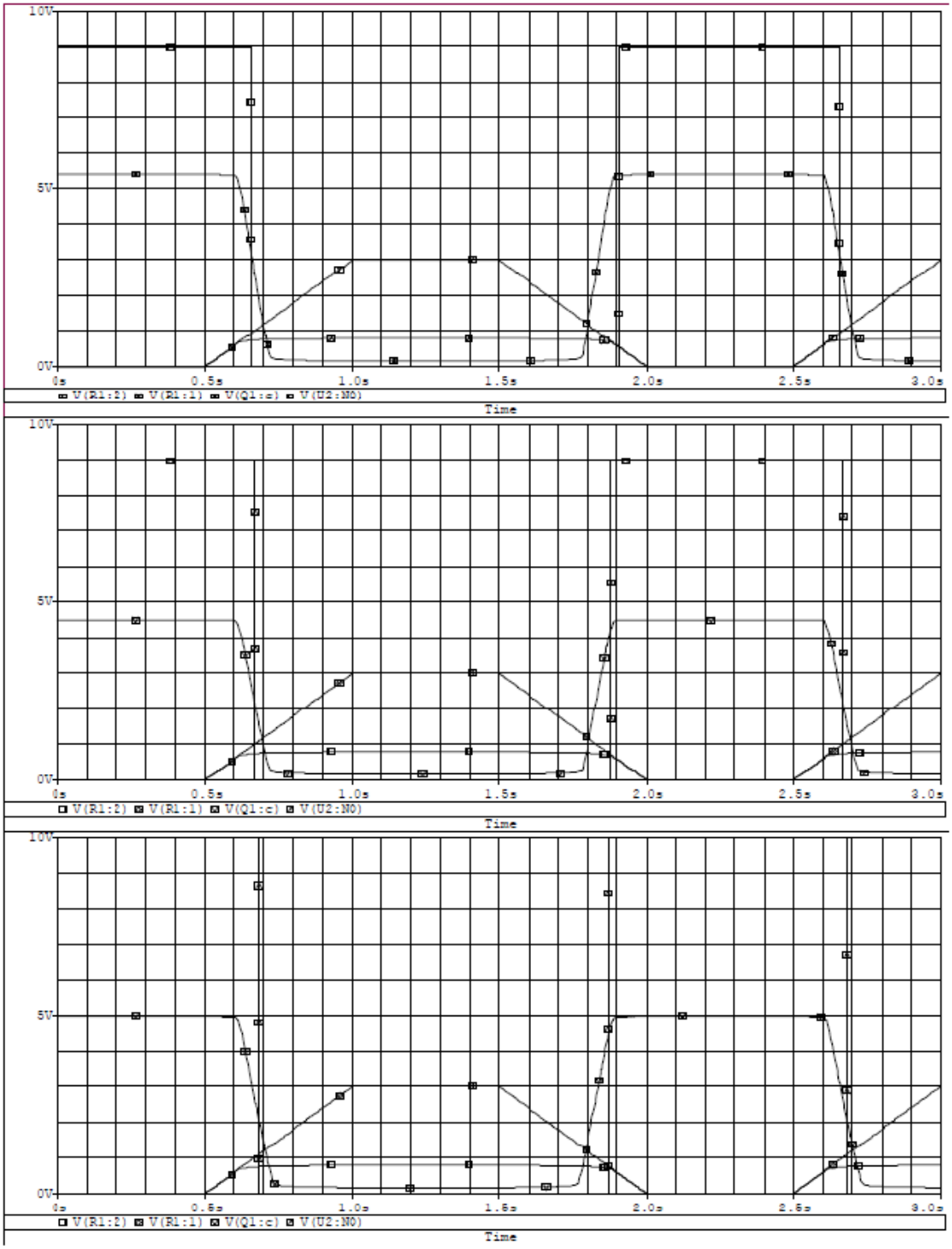
2. If Vpulse is on (3V):

   a) What is the voltage at point D? (***1 pt***) Explain why (circuit drawing with comments) (***1 pt***).

   b) What is the voltage at point C? (***1 pt***) Explain why (circuit drawing with comments) (***1 pt***).

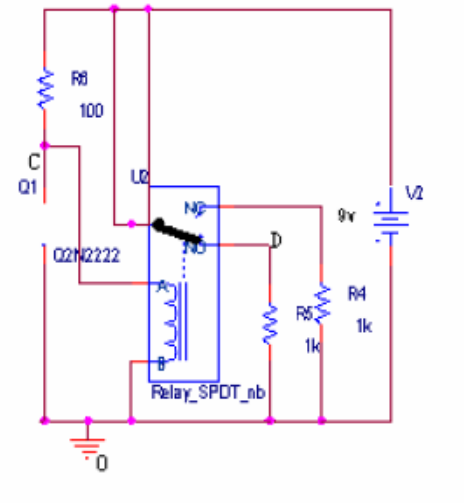
Question IV – Switching Circuits (continued)

3. Using this information and the overall circuit diagram, ***identify*** which of the following plots goes with this circuit (***4 pts***) ***AND label points A, B, C and D*** (***8 pts***) on the plot. (Mistakes will be carried over from parts b and c as a deduction).



Answer:

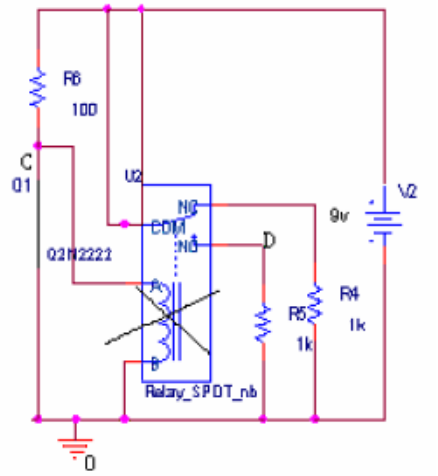
Vpulse is off(0 volts) ⇙ VA = 0V (pulse low) and VB = 0V (pulse low) ⇙ diode is off ⇙ current flows through relay ⇙ relay switch at NO



VD = 9V

*VC = V2*R_{relay}/(R_{relay} + R6) =9(100)/(100+100) = 4.5V*

Vpulse is on(3 volts) ⇙ VA = 3V (pulse high) and VB = 0.6 volts (drop across diode when on) ⇙ diode is on ⇙ no current flows through relay ⇙ relay switch at NC



VC = 0 V (There is actually a 0.2 voltage drop across the transistor when it is shorted which you can see, if you look.)

VD = 0 V (NO is not attached to anything)

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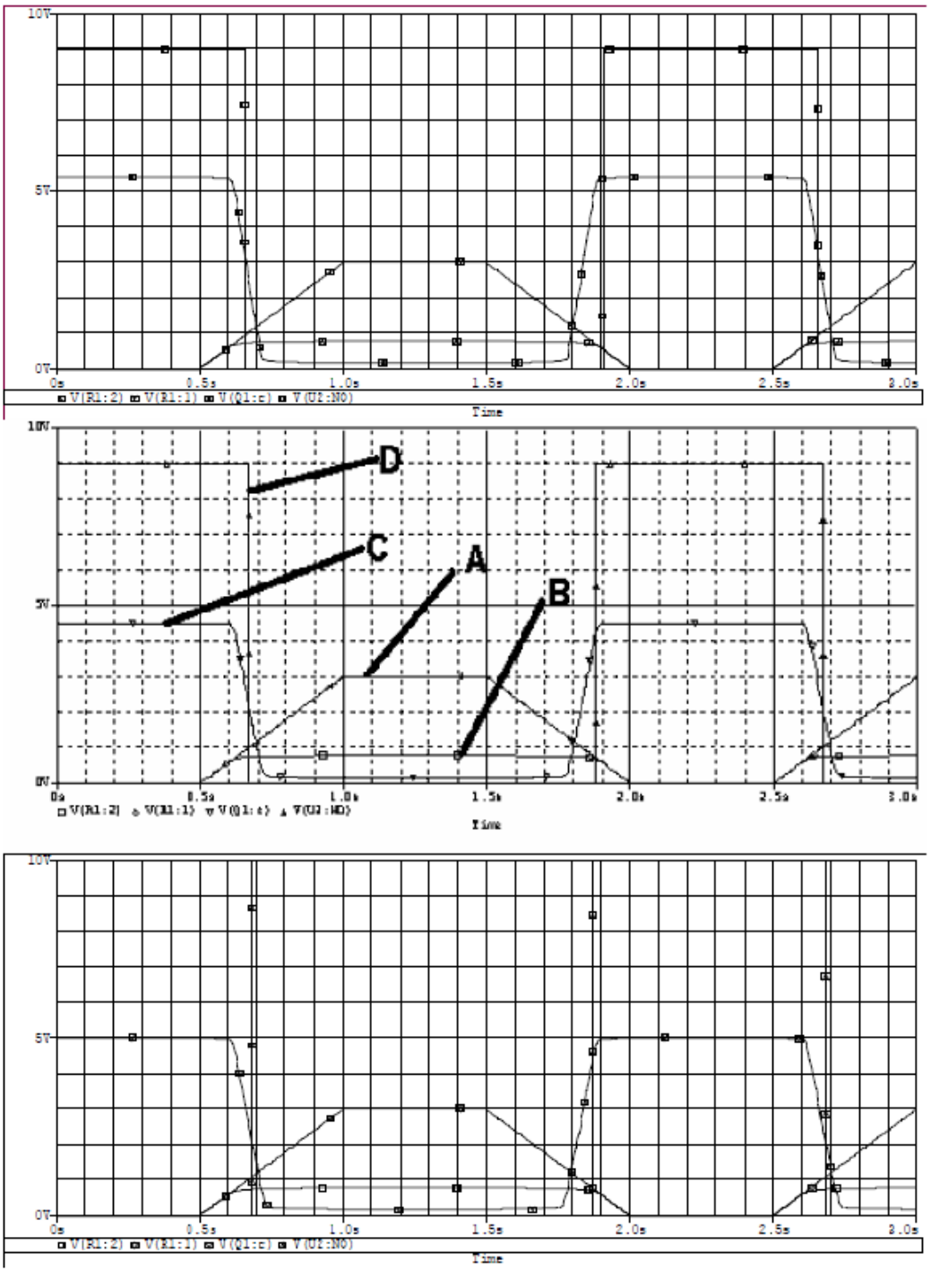
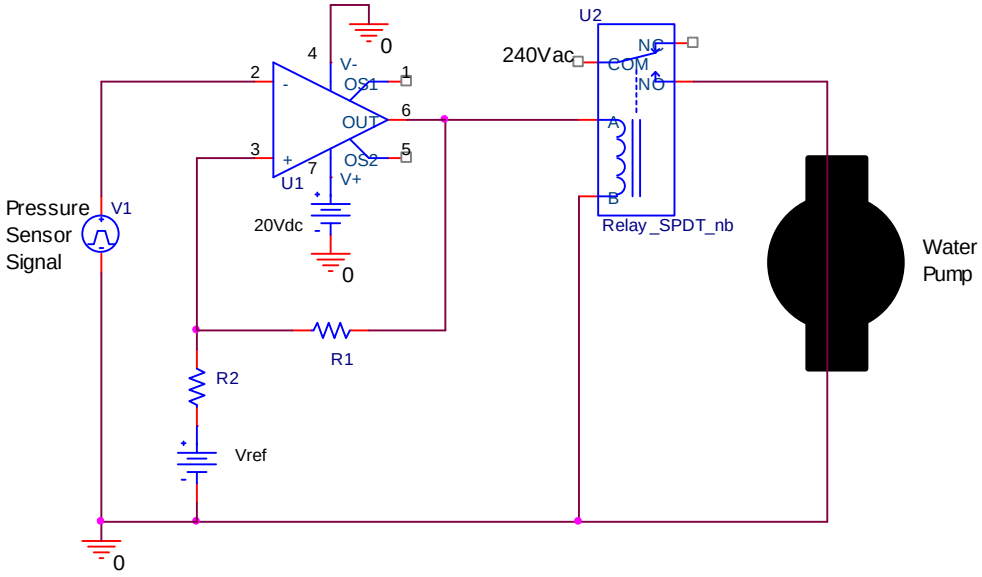


Question V – Comparators and Schmitt Triggers (25 points)

1. (2pt) A typical rural dwelling has a well, pump, and pressure tank to supply the household water. The system is designed to turn on the pump when the tank water pressure is 20psi and turn it off when it reaches 40psi. What is the name associated with a switching system exhibiting this behavior?

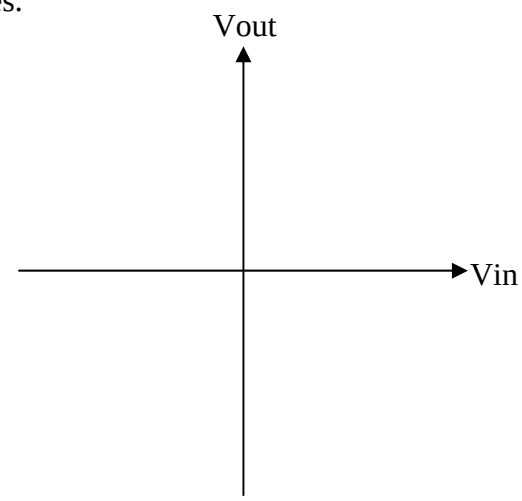
Schmitt trigger or Hysteresis



2. (3pt) Given a tank pressure sensor transducer circuit that outputs 0.5V/psi (V1 in the above circuit), what would be appropriate voltage thresholds for the high power ideal op-amp circuit to match the pump's two switching points?

$V+_{low}$ = 20psi x 0.5V/psi = 10V **$V+_{high}$ = 40psi x 0.5V/psi = 20V**

3. (5pt) On the axes below sketch the input-output curve for the circuit in 1. Be sure to scale both axes.



Question V – Comparators and Schmitt Triggers (continued)

4. (6pt) Set up the equations to find appropriate values for R1, R2, and Vref in the circuit above in terms of the op-amp's supply voltages and the desired switch points for the water pump.

$$v+ = \frac{R2}{R1+R2}(v_{out} - V_{ref}) + V_{ref}$$
$$v+_{high} = \frac{R2}{R1+R2}(+20 - v_{ref}) + v_{ref} = +20V$$
$$v+_{low} = \frac{R2}{R1+R2}(0 - v_{ref}) + v_{ref} = +10V$$

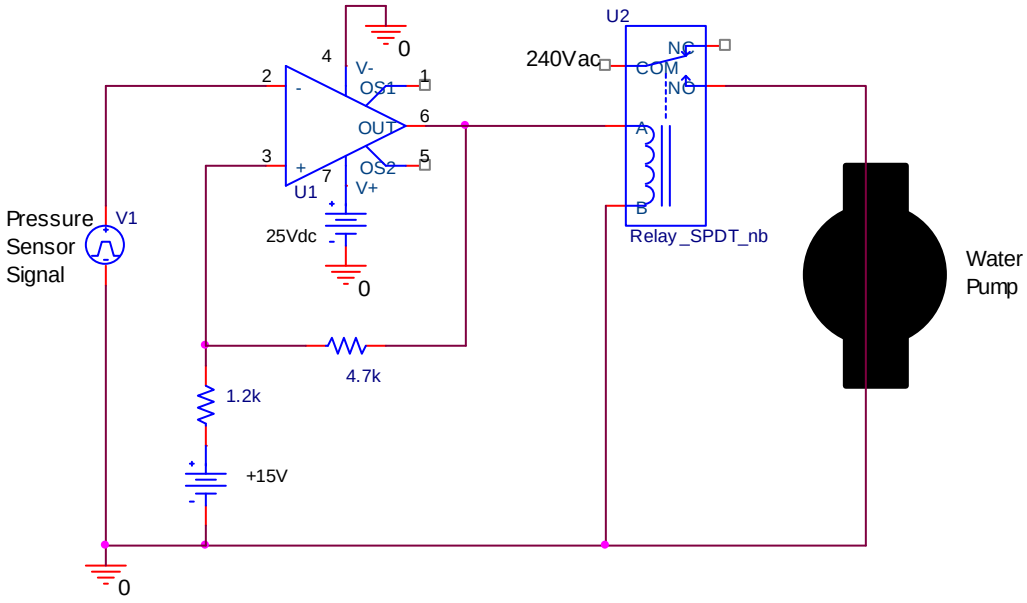
5. (4pt) Given that R2 = 1k, find the values of R1 and Vref. (hint: two equations two unknowns: simplify $v+_{high}$ and/or $v+_{low}$)

May solve simultaneous system of equations, but by inspection:

if R1 = 1k and Vref = 20V then

$$v+_{low} = \frac{1}{2}(0 - 20) + 20 = -10 + 20 = +10V$$
$$v+_{high} = \frac{1}{2}(+20 - 20) + 20 = +20V$$

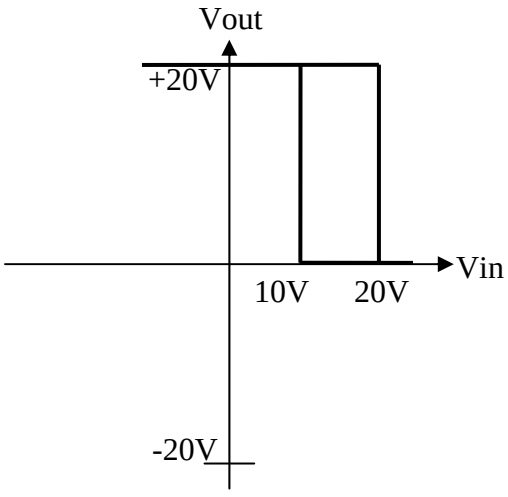
6. (5pt) If the circuit below is built (note new op-amp V+ supply), what are the high and low pressure switching points, given the same pressure transducer?



$$v+_{high} = \frac{1.2k}{1.2k+4.7k}(+25-15)+15 = +17.0V \rightarrow \text{Pressure}_{high} = 34\,psi$$

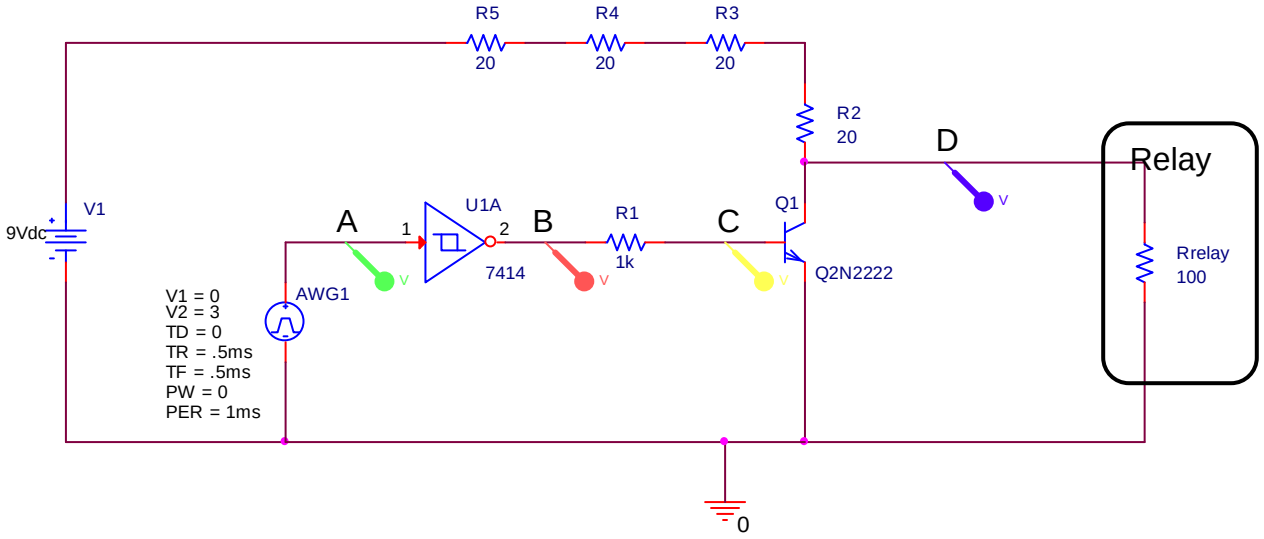
$$v+_{low} = \frac{1.2k}{1.2k+4.7k}(0-15)+15 = +11.95V \rightarrow \text{Pressure}_{low} = 23.9\,psi$$

Answer to part 3.

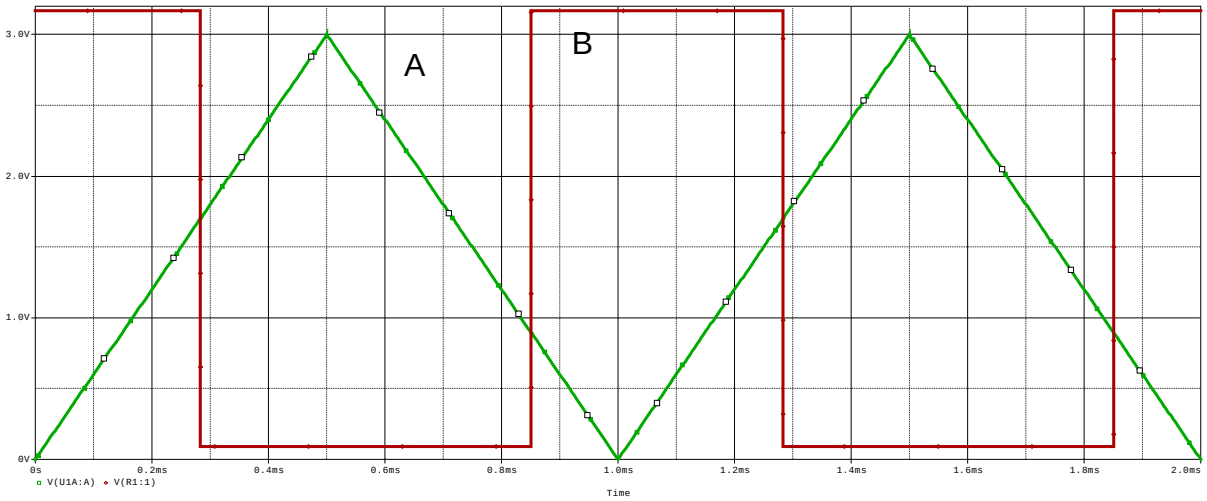


Question VI – Measurements (20 points)

Consider a setup similar to the test you did in Experiment 6 on triggering the relay. Here the relay is represented using only its coil resistance. This is the version of the circuit recommended to assure a full 5 Volts to operate the relay coil. The PSpice circuit shows the voltage being measured at 4 locations.

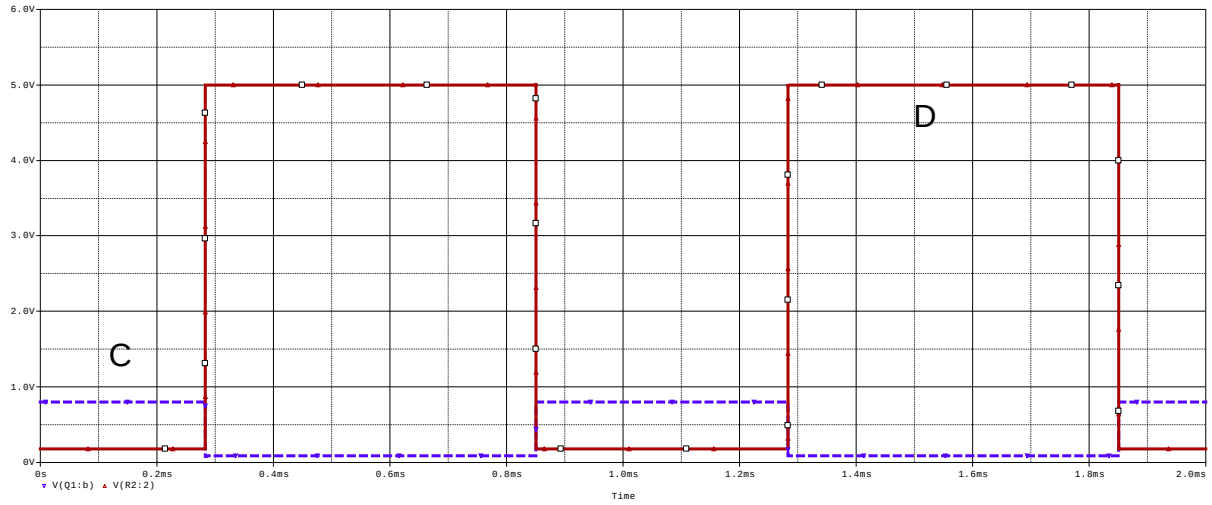


1. (8pts) Shown below are the four measured voltages.
   a. Label each plot with the location where it is measured (e.g. A, B, C or D)
   b. Clearly identify each feature of the four plots and why the information in the plot makes sense.



A: Triangular wave rising from zero to 3V and back in 1ms, which is what the vpulse is set up to do. B: The triangular wave triggers the Schmitt trigger at around 1.7V and about 0.8V which is what it is designed to do. The output voltage goes high when triggered on (above 3V) and low (near zero) when off. The hysteresis of the Schmitt trigger is clear from these different levels.

Question VI – Measurements (continued)



C: The output voltage from the Schmitt trigger is stepped down with the 1k Ohm resistor to levels (of current too) sufficient to trigger the transistor on and off.
D: When the transistor is an open switch, the voltage across the relay coil is determined from the voltage divider action of the four 20 Ohm resistors and the coil resistance, so that the voltage is 9(50/90)=5V as expected. The voltage when the transistor switch is closed is near zero.

2. (4pts) The circuit has two states – one where the relay is on and one where it is off. For each of the two states, determine the power dissipated in the six resistors. The relay coil is designed to handle 5V or more but the other resistors we are using are limited to operate at up to only a quarter of a Watt. Have the resistors been chosen correctly so that no individual resistor must handle more than this limit?

Max Voltages: The voltage across each of the 20 Ohm resistors is (9/4)V. The voltage across the relay coil is 5V and the voltage across the 1k resistor on the base of the transistor is a little less than 3V. The power is the square of the voltage divided by the resistance, which is about 250mW for the 20 Ohm resistors and also the coil resistance. For the 1k Ohm resistor, the power is about 9mW.

Min Voltages: For the four 20 Ohm resistors, the min voltage is 1V. The minimum voltage across the coils is about zero so the power is zero. For A, the voltage rises from zero to 3 or $V=3/(5\times10^{-4})$ and then drops. The power for the 20 Ohm resistors is 50mW. The min power for the 1k resistor is also near zero.

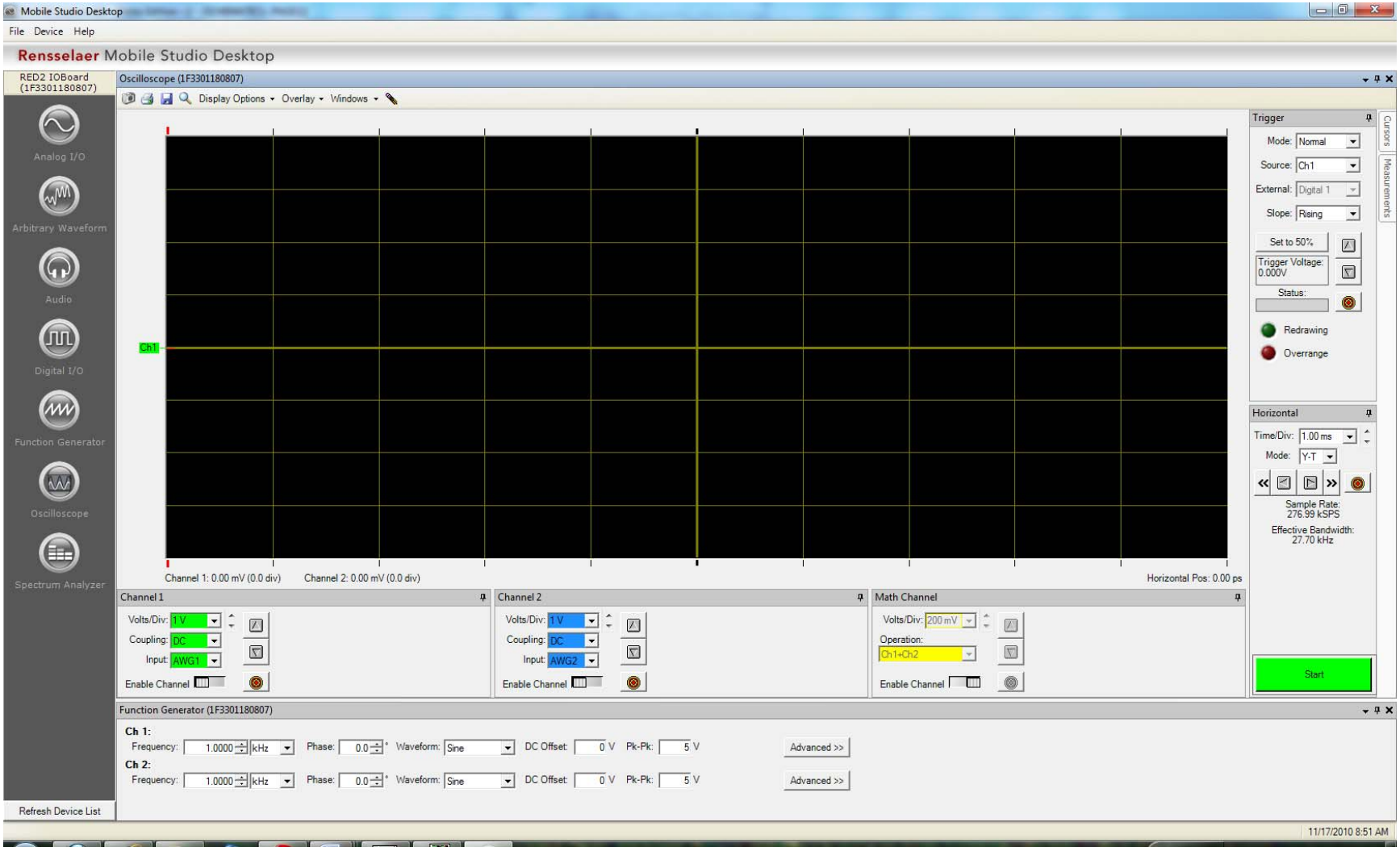
Question VI – Measurements (continued)

3. (4pts) On the following page is a screen shot for the Mobile Studio Desktop. Describe how to setup the function generator (AWG1) to produce the signal from the source in the PSpice simulation.

   See next page. Note that an offset is required of 1.5V and Vpp is 3 volts. The frequency is 1kHz.

4. (4pts) Describe how to set up the oscilloscope in the Mobile Studio so that channel one can be used to measure any of the 4 voltages. That is, what options should one choose from the various drop down menus for the oscilloscope to produce plots that look roughly like the ones generated using PSpice? It is not necessary to produce exactly the same plots, but they should look similar and the complete signals should be visible.

See next page.


Mobile Studio Desktop
File Device Help
Rensselaer Mobile Studio Desktop
RED2 IOBoard (1F3301180807)
Analog I/O
Arbitrary Waveform
Audio
Digital I/O
Function Generator
Oscilloscope
Spectrum Analyzer
Refresh Device List
Oscilloscope (1F3301180807)
Display Options
Overlay
Windows
Ch1
Channel 1: 0.00 mV (0.0 div)
Channel 2: 0.00 mV (0.0 div)
Horizontal Pos: 0.00 ps
Trigger
Mode: Normal
Source: Ch1
External: Digital 1
Slope: Rising
Set to 50%
Trigger Voltage: 0.000V
Status:
Redrawing
Overrange
Horizontal
Time/Div: 1.00 ms
Mode: Y-T
Sample Rate: 276.99 kSPS
Effective Bandwidth: 27.70 kHz
Start
Cursors
Measurements
Channel 1
Volts/Div: 1 V
Coupling: DC
Input: AWG1
Enable Channel
Channel 2
Volts/Div: 1 V
Coupling: DC
Input: AWG2
Enable Channel
Math Channel
Volts/Div: 200 mV
Operation: Ch1+Ch2
Enable Channel
Function Generator (1F3301180807)
Ch 1:
Frequency: 1.0000 kHz
Phase: 0.0 °
Waveform: Sine
DC Offset: 0 V
Pk-Pk: 5 V
Advanced >>
Ch 2:
Frequency: 1.0000 kHz
Phase: 0.0 °
Waveform: Sine
DC Offset: 0 V
Pk-Pk: 5 V
Advanced >>
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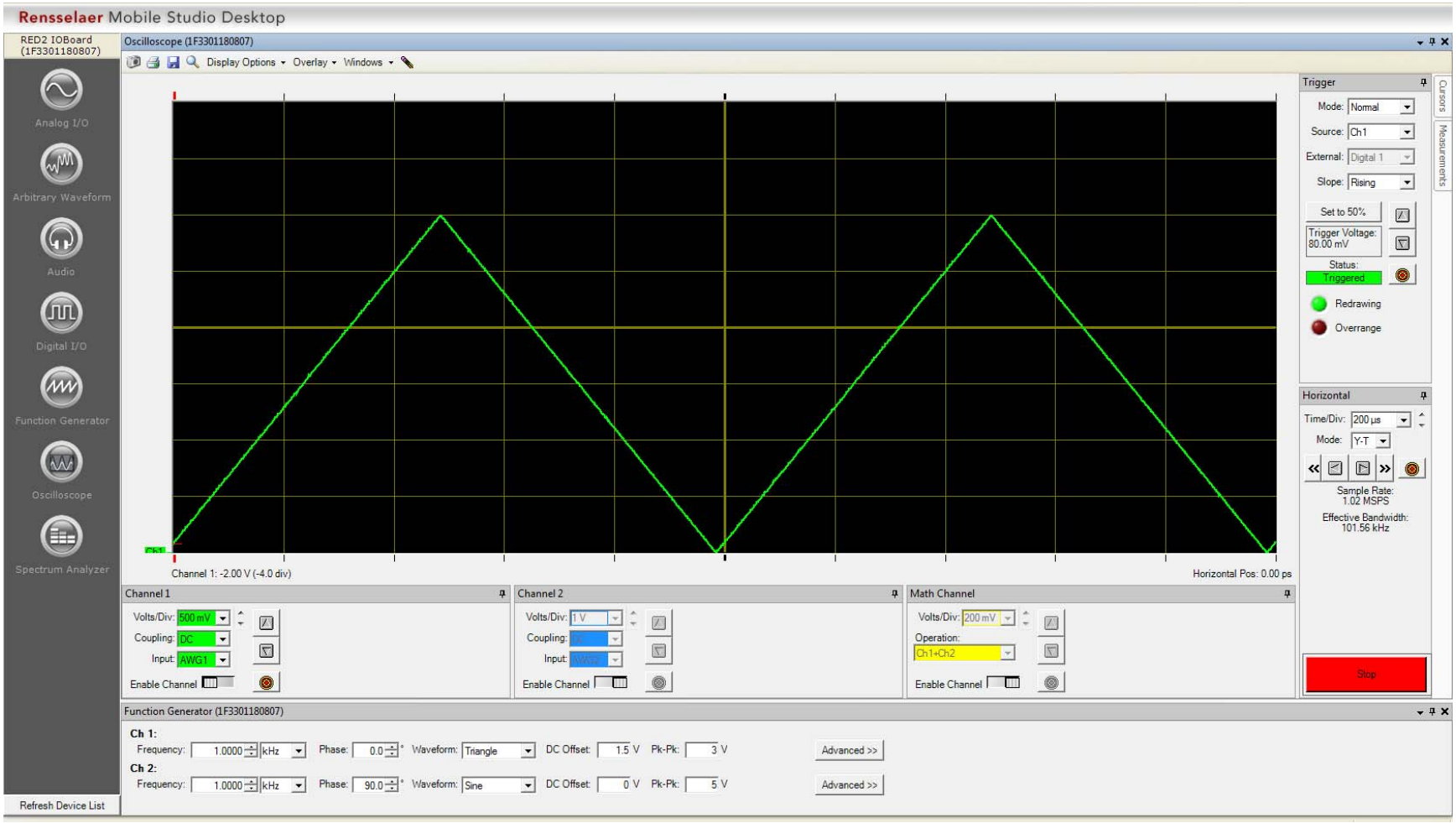

This shows the most reliable way to accomplish this, since the input impedance for the scope channel is very large at 500mV/div. This requires moving the zero line down to the bottom of the display. One could also do 1V/div, which will slightly modify the results and thus is not as good as this approach. One can also leave the zero line in the middle and add a big voltage divider across the measured points so that the voltages at the four locations will not be modified by the measurement and the high input impedance scale can still be used. (In the figure above, the trigger had to be set a little above zero or the signal never crosses the threshold.)