Mushroom Timer Circuit

The timer circuit described in the leda.lycaeum.com link in Exp 7 was simulated using PSpice. Since the timing is very different from any other problem we have solved, it was necessary to modify one of the default simulation parameters. This is described on the last page of this report.



The top trace shows the output from pin 3 of the 555 chip, while the bottom trace shows the output from the transistor. The transistor output inverts the input voltage.

From the cursors placed on the figure, the total on plus off time is equal to 1218 seconds. The on time is about 20 seconds and the off time is about 20 minutes.

A 555 timer designer program was downloaded from a very useful website <u>http://www.electronicsaustralia.com.au/cgi-bin/downloads.pl?area=7</u>



This does the simple calculations showing the high and low times for the choice of resistors and capacitor. This also confirms that the components chosen work as indicated.

Modifications to PSpice to simulate a circuit for over 20 minutes.

First, the simulation settings must be specified. Note that the run to time (TSTOP parameter) is set to 3000 seconds. The first step in the simulation is very, very small. The simulation begins with a time step of about .03ns to keep the changes in voltages small. Since the total time is so long, the program gives up after only a few nano seconds.

Simulation Settings - test 🛛 🛛 🗙					
General Analysis Include Files Analysis type: Time Domain (Transient) Image: Comparison of Comparison	s Libraries Stimulus Options Data Collection Probe Window Run to time: 3000s seconds (TSTOP) Start saving data after: 1000s seconds Transient options Maximum step size: 1 Maximum step size: 1 seconds Skip the initial transient bias point calculation (SKIPBP) Output File Options				
	OK Cancel Apply Help				

To fix this problem, we need to go to the options tab above and change the relative accuracy parameter (RELTOL) from .001 to .1.

Simulation Settings - test					
General Analysis Include Files Libraries Stimulus Options Data Collection Probe Window					
Category:				(.OPTION)	
Analog Simulation	Relative accuracy of V's and I's:	.001		(RELTOL)	
Gate-level Simulation	Best accuracy of voltages:	1.0u	volts	(VNTOL)	
j Uutput nie	Best accuracy of currents:	1.0p	amps	(ABSTOL)	
	Best accuracy of charges:	0.01p	coulomb	s (CHGTOL)	
Minimum conductance for any branch:		1.0E-12	1/ohm	(GMIN)	
	DC and bias "blind" iteration limit:			(ITL1)	
	DC and bias "best guess" iteration limit:	20		(ITL2)	
	Transient time point iteration limit:	10		(ITL4)	
Default nominal temperature:		27.0	°C	(TNOM)	
	Use GMIN stepping to improve convergence. (STEPG Use preordering to reduce matrix fill-in. (PREOR)				
MOSFET Options Advanced Options Reset					
OK Cancel Apply Help					

This changes the minimum time step according to the following:

Minimum Time Step = TSTOP/(dynamic range of time)

where, dynamic range of time =

15 digits - the number of digits of accuracy required by RELTOL.

For example, if TSTOP =1us and RELTOL=.001, then the minimum time step is: 1E-6/(1E15-1E3)=1E-18.

Thus, for our case, the minimum time step is: 3000/(1e15-1e1)=3e3/1e14=3e-11. Before we changed RELTOL, the minimum time step was 3e-13. With such a small time step, the program gave up before it got past a few nanoseconds.