

ENGR-2300  
Electronic Instrumentation  
**Quiz 3, Spring 2019**

Name: \_\_\_\_\_ **Solution** \_\_\_\_\_  
Please write your name on each page

Section: 1 or 2

4 Questions Sets, Total of 80 Points  
LMS Portion, 20 Points

- |                 |  |
|-----------------|--|
| Question Set 1) | <b>Astable Multivibrator</b>                           |
| Question Set 2) | <b>Combination &amp; Sequential<br/>Logic Circuits</b> |
| Question Set 3) | <b>Diodes and Rectifiers</b>                           |
| Question Set 4) | <b>Comparators and Schmitt<br/>Triggers</b>            |

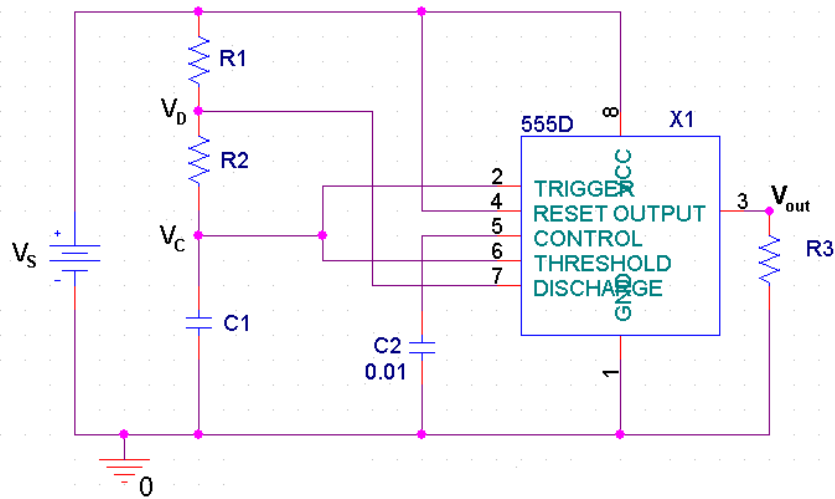
On all questions:

**SHOW ALL WORK. BEGIN WITH FORMULAS,  
THEN SUBSTITUTE VALUES AND UNITS.**

No credit will be given for numbers that appear without justification.  
Unless otherwise stated in a problem, provide 3 significant digits in answers.  
It may be easier to answer parts of questions out of order.

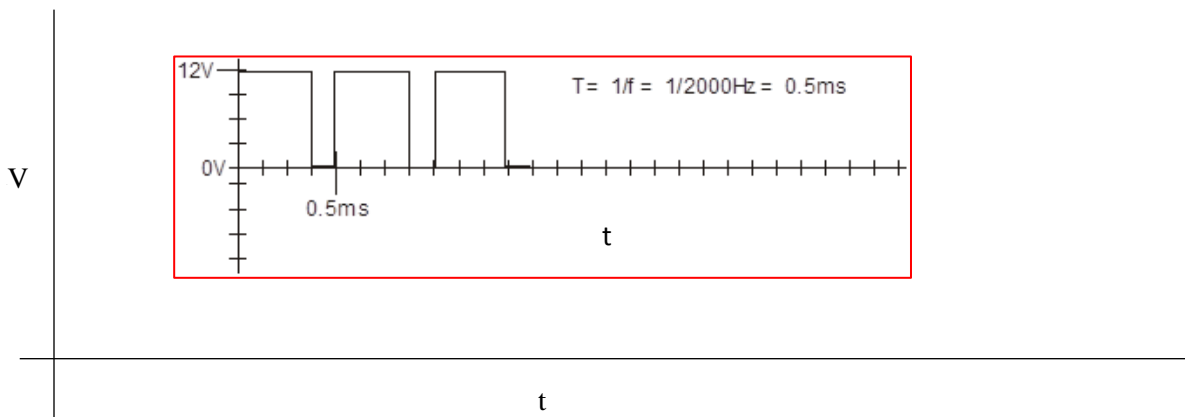
If you need extra room, make it clear in the main problem statement that work is  
continuing on the back of the page.

**Question Set 1) Astable Multivibrator (20 pts)**



The multivibrator above was built with the 555 timer chip shown. In the diagram,  $V_s$  is the source voltage,  $V_c$  is the voltage across the capacitor  $C_1$ , and  $V_D$  is the voltage at the discharge pin of the timer. You have access to a 12VDC battery to power your timer and you want to use it to control motor speed by building a PWM motor controller (disregard the fact that you can't directly drive much of a motor with the 555 output). To achieve the speed you want, the PWM signal must have a duty cycle of 75%. You've decided the PWM frequency should be 2kHz to achieve sufficiently smooth speed regulation for your application.

1.a) (2 pts) Draw the waveform you need at  $V_{out}$  given the requirements above and label zero volts, max voltage (give the number on the axis), and label the time axis (again giving numbers and units). Show THREE periods of the signal. (2 pt)



1.b) (1 pt) What is the required ON time of the multivibrator?

$$75\% * 0.5\text{ms} = 0.375\text{ms}$$

1.c) (1 pt) What is the required OFF time of the multivibrator?

$$25\% * 0.5\text{ms} = 0.125\text{ms} \text{ (or could have used } 0.5\text{ms} - 0.375\text{ms on time} = \text{off time)}$$

1.d) (4 pt) You only have a 2.2uF capacitor available but many resistors to select from, so find R1 & R2 that will achieve the desired on and off times.

$$T_{\text{off}} = 0.693 * R_2 * C_1; R_2 = T_{\text{off}} / (.693 * C_1) = .125\text{ms} / (.693 * 2.2\mu\text{F}) = 81.99 \text{ ohm}$$

$$T_{\text{on}} = 0.693 * (R_1 + R_2) * C_1; R_1 = T_{\text{on}} / (.693 * C_1) - R_2 = 163.98 \text{ ohm}$$

$$R_1: 163.98 \text{ ohm}$$

$$R_2: 81.99 \text{ ohm}$$

1.e) (2 pt) Using the equation for astable multivibrator frequency provided on the crib sheet, confirm that the operating frequency of your device is correct.

$$f = 1.44 / (R_1 + 2 * R_2) * C_1 = 1.44 / (163.98 + 2 * 81.99) * 2.2\mu\text{F} = 1.996\text{kHz} \approx 2\text{kHz}$$

1.f) (2 pt) In theory, what are the maximum and minimum voltages that should be observed across capacitor C1 while the circuit is functioning? (Give numbers and units please, ignore initial startup conditions at the time power is first applied to the circuit)

$$\text{Max} = 2/3 * V_{\text{cc}} = 8\text{V}; \text{Min} = 1/3 * V_{\text{cc}} = 4\text{V}$$

1.g) (3 pt) When the transistor inside the 555 timer is closed, the output at pin 7 is grounded, and therefore, equal to zero. When the transistor is open, the voltage at pin 7 can be found using the voltage divider formed by R1 and R2. Find an expression for the voltage at pin 7 (when pin 7 is not grounded) in terms of the voltage across the capacitor,  $V_c$ , the source voltage,  $V_s$ , and the two resistors R1 and R2. [Hint: Recall how you calculate the voltage at the non-inverting input for a Schmitt trigger.] Do not substitute values.

Voltage divider sits on top of capacitor voltage, so we use voltage difference across two resistors to figure out voltage drop across bottom resistor and then add back whatever voltage is on the capacitor:

$$V_{r2} \text{ (voltage drop across R2)} = V_{r12} \text{ (voltage drop across both resistors)} * R_2 / (R_1 + R_2);$$

$$\text{Voltage drop across both resistors also} = V_s - V_c$$

$$V_{pin7} = V_c + V_{r2} = V_c + (V_s - V_c) * R_2 / (R_1 + R_2)$$

1.h) (2 pt) Use the equation in 1.g) to find the maximum and minimum voltage that is ever possible at pin 7 when the transistor is open. [Hint: assume that the capacitor is completely discharged when power is first applied to your circuit.]

Voltage is zero (or  $V_{ce} \sim 0.2V$  when transistor is closed [on]), but we're asking about open. Depending on where cap C1 is in charge cycle, it is at extremes found in part 6.

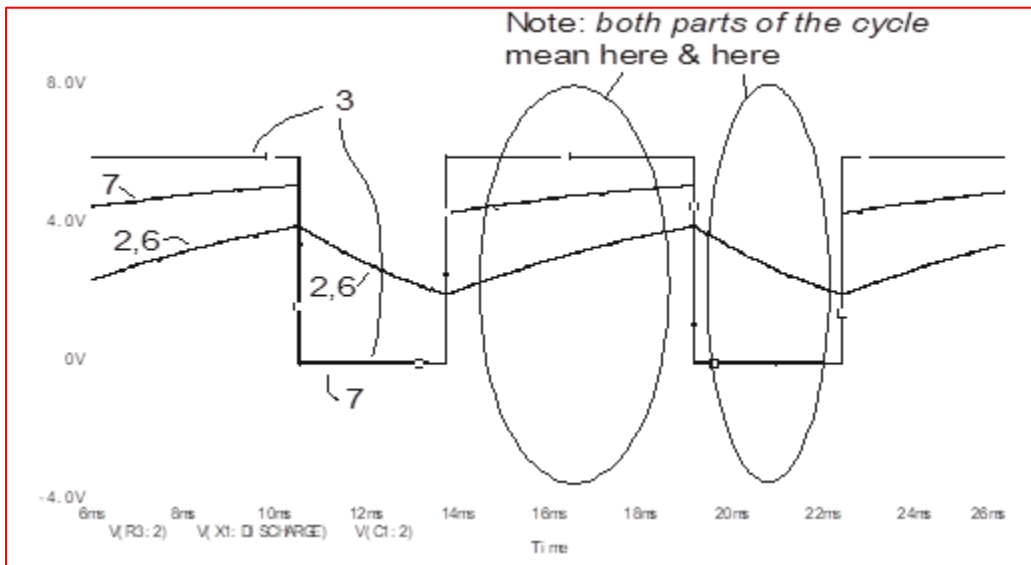
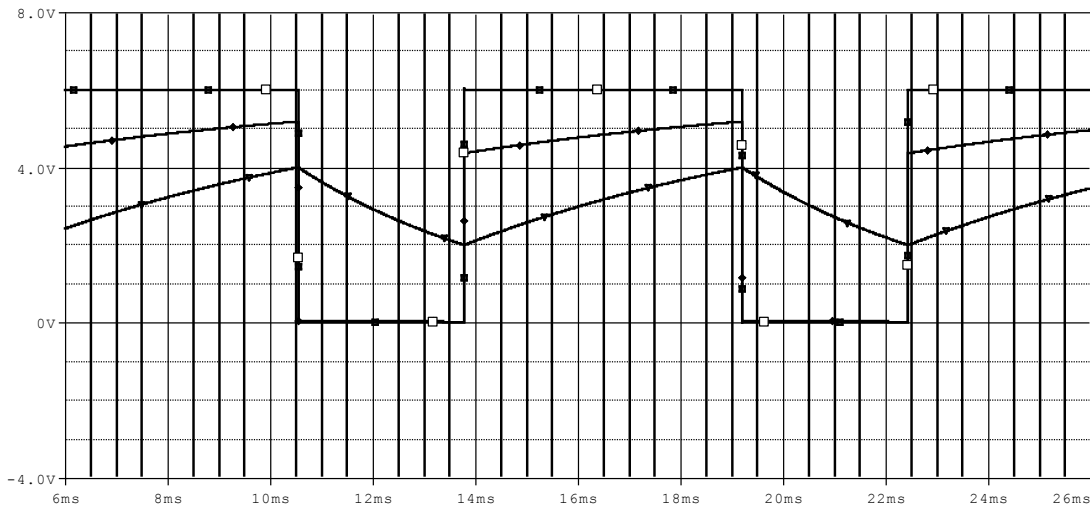
$$V_{c\_min} = 4V; V_{c\_max} = 8V \text{ from part 6.}$$

$$V_{pin7} = V_c + (V_s - V_c) * R_2 / (R_1 + R_2), \text{ so}$$

$$V_{pin7\_min} = V_{c\_min} + (V_s - V_{c\_min}) * R_2 / (R_1 + R_2) = 4V + (12 - 4) * 82 / (82 + 164) = 6.67V$$

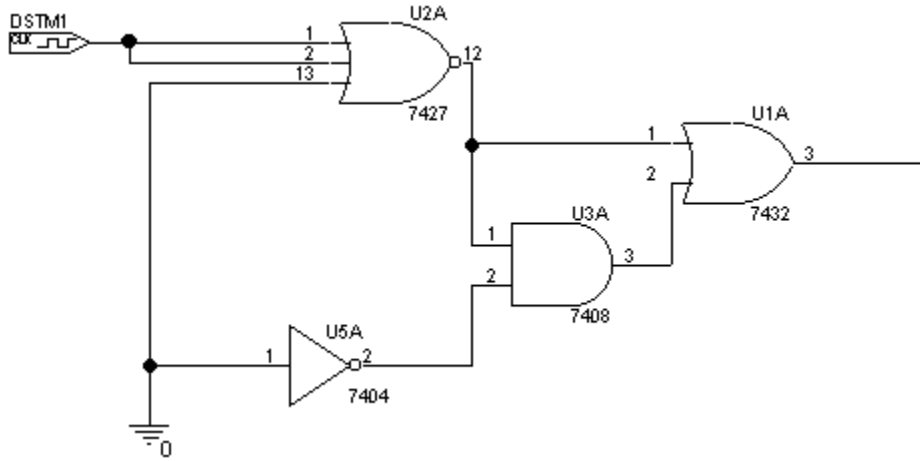
$$V_{pin7\_max} = V_{c\_max} + (V_s - V_{c\_max}) * R_2 / (R_1 + R_2), = 8V + (12 - 8) * 82 / (82 + 164) = 9.33V$$

1.i) (3 pt) On the graph below (for a different 555 astable multivibrator circuit) identify the outputs at pins (2 & 6), 7 and 3 of the multivibrator. Identify both parts of the cycle for each.



**Question Set 2) Combination & Sequential Logic Circuits (23 pts)**

You should recognize the digital gates in the following circuit as the ones introduced in the lab and/or in class.



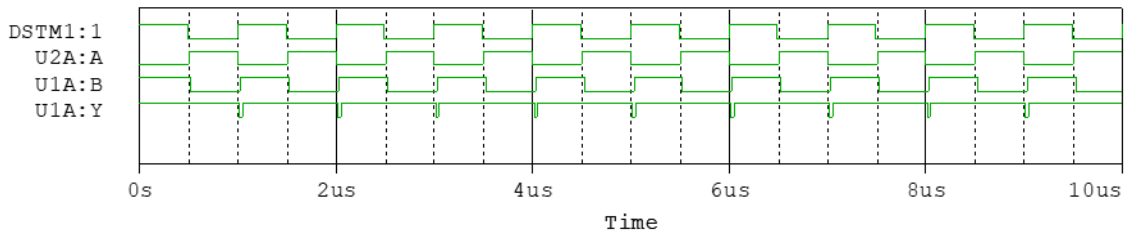
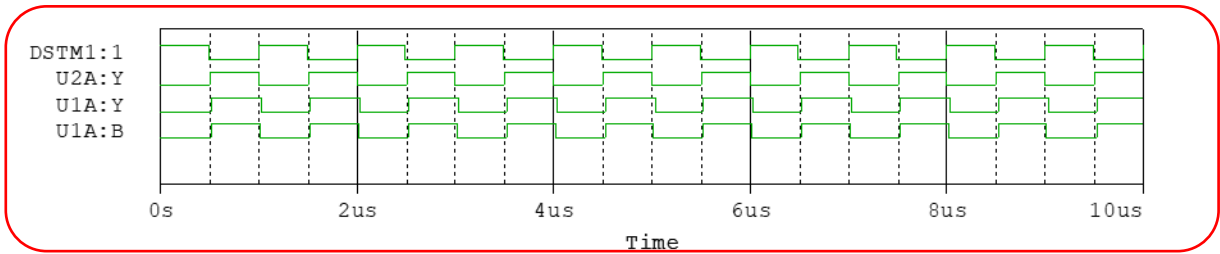
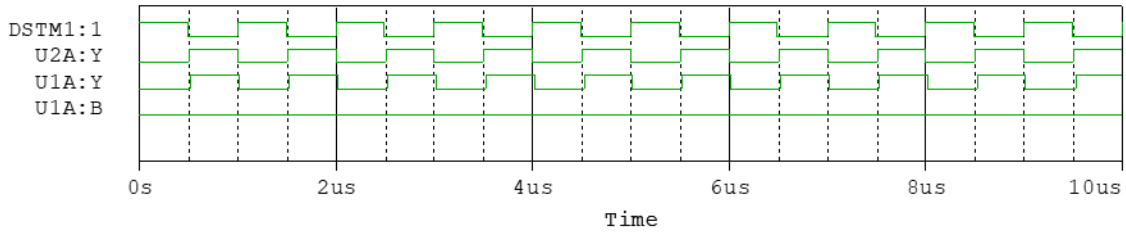
2.a) (2 pts) What kind of gate is U2A?

U2A is a three input **NOR** gate (answer is still correct if student doesn't mention the number of inputs)

2.b) (3 pts) What is the truth table for gate U2A? **Note: You are given more rows and columns than needed. Fit your truth table anywhere within table below. Label the columns.**

Input 1	Input 2	Input 3	Output	
0	0	0	1	
0	0	1	0	
0	1	0	0	
0	1	1	0	
1	0	0	0	
1	0	1	0	
1	1	0	0	
1	1	1	0	

2.c) (5 pts) Indicate which of the three plots below represents the output of the circuit. Show any work for partial credit.

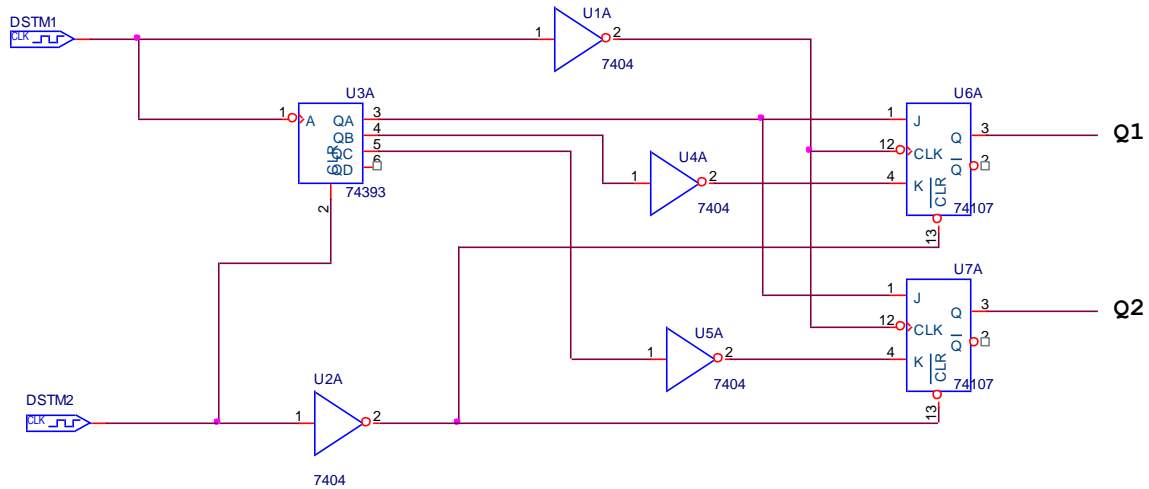


*work:*

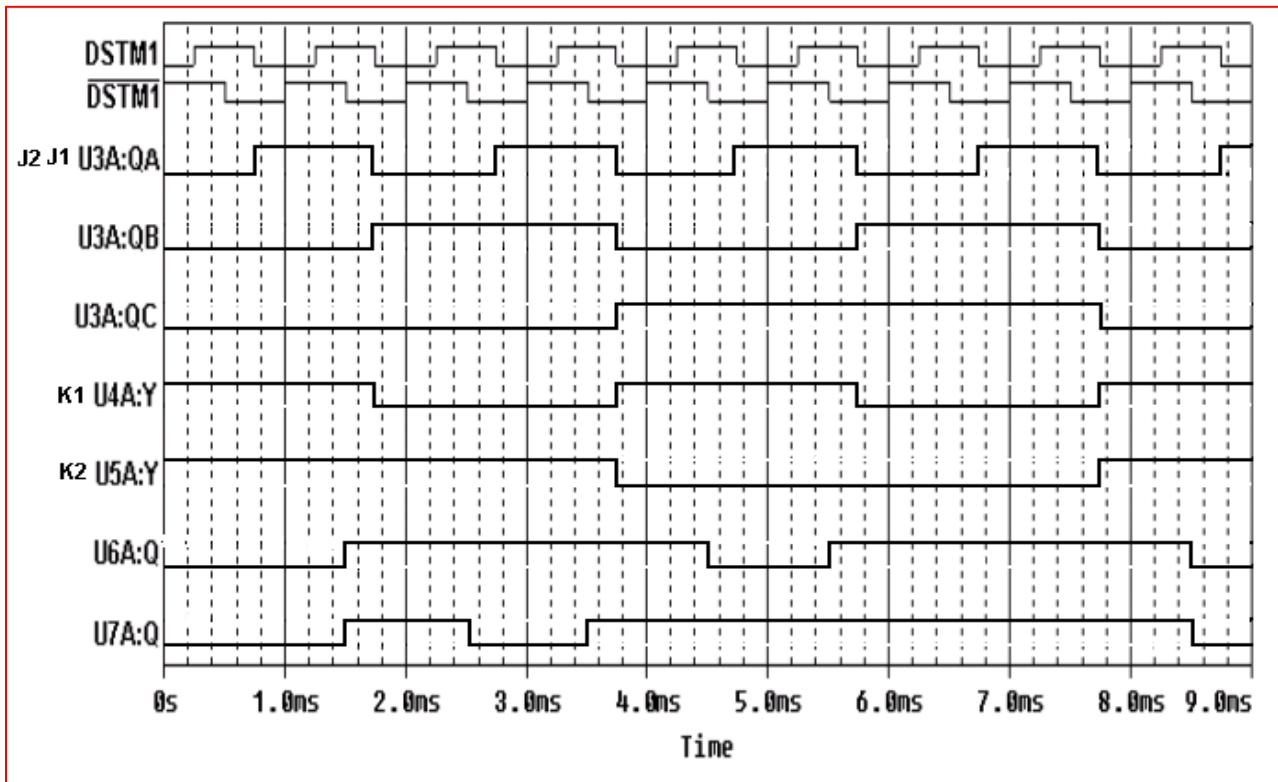
<i>DSTM1</i>	<i>U2A:Y</i>	<i>U5A:Y</i>	<i>U3A:Y</i>	<i>U1A:Y</i>
<i>0</i>	<i>1</i>	<i>1</i>	<i>1</i>	<i>1</i>
<i>1</i>	<i>0</i>	<i>1</i>	<i>0</i>	<i>0</i>

*Note: U1A:B is the same as U3A:Y*

You are given the following circuit where DSTM1 provides the clock for the counter. *DSTM 1* provides the clock to the two flip flops. *DSTM2* provides an initial reset pulse to all the sequential chips. Therefore, you can assume that QA, QB, QC, QD, Q1, and Q2 are all initially low.

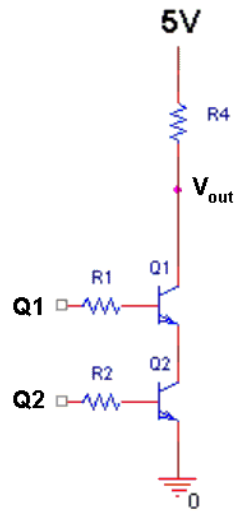


2.d) (7 pts) Sketch the timing trace for each of the signals shown.





2.e) (3 pts) Take the output of the previous circuit and use it as the input to the transistor circuit shown below. Fill in the state table for all possible values of Q1 and Q2.



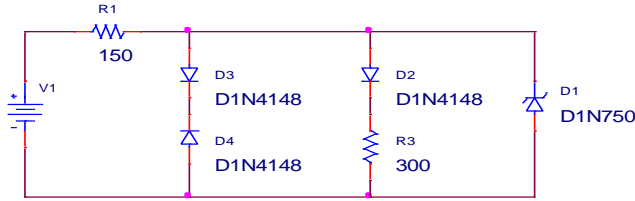
Q1	Q2	Vout
0V	0V	5V
0V	5V	5V
5V	0V	5V
5V	5V	0V

f) (3 pt) What are the values of the signals at Q1, Q2 and Vout after 8.9 milliseconds?

**All Tests: Q1: 0V Q2: 0V Vout: 5V**

**Question Set 3) Diodes and Rectifiers (19 pts)**

3.a) (4 pts) The circuit below has been assembled for...reasons. Find the voltage across the load resistor, R3, given the source voltages listed in the table.



V1	V <sub>R3</sub>
0.5 V	0.00 V
1 V	0.20 V
2.5 V	1.20 V
5 V	2.87 V
10 V	4.00 V
20 V	4.00 V

D3 and D4 are opposing directions, can be ignored completely

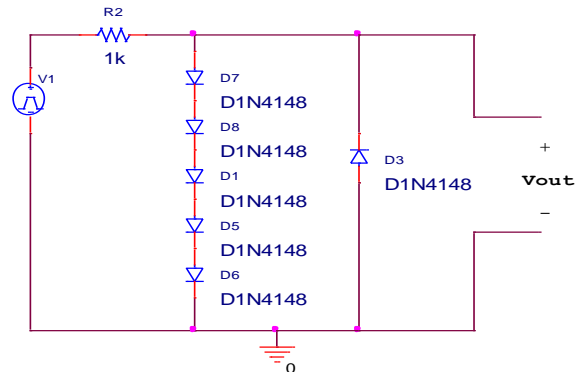
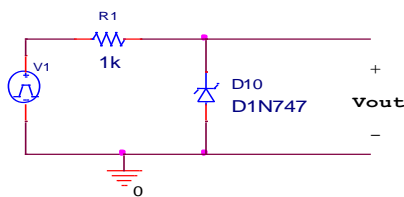
Zener OFF for V1 = 0.5 V, 1 V, 2.5 V, ON for V1 = 5 V and 10 V

For V1 = 0.5 V: voltage not large enough to overcome D2 diode drop, therefore no current through R3 -> 0 V

For V1 = 1 V, 2.5 V: D2 active, giving 0.7 V drop. Left with voltage divider of R1 and R3 with V1 - 0.7 V input.

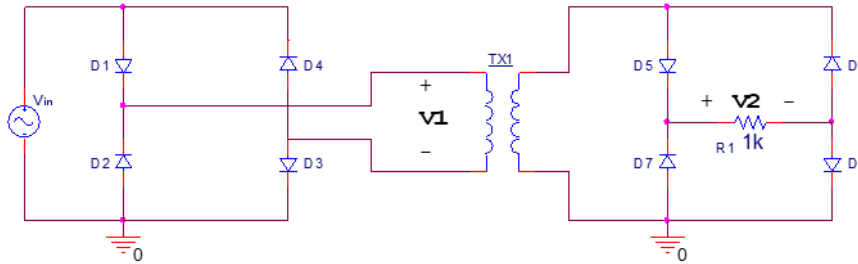
For rest, calculate voltage divider as above and check if VD1 (= VR3+0.7 V) > 4.7 V (Zener voltage-crib sheet). If no, then keep calculated VR3. If yes, then Zener is ON and voltage across D2+R3 is forced down to 4.7 V. Voltage across R3 is then calculated as 4.7 V Zener voltage - 0.7 V diode drop = 4 V.

3.b) (4 pts) We want to build the circuit below, but unfortunately, do not have any D1N747 diodes. Luckily, D1N4148 diodes are scattered all over the place. Redraw the circuit below using only D1N4148 diodes so that the replacement circuit will operate in the same way, approximately. Note: D1N747 have a Zener voltage of 3.6 V.



The Zener voltage is a 3.6 V drop. 5 D1N4148 diodes in gives approximately the same voltage drop (3.5 V). The upwards diode represents the forward bias region of the Zener, 0.7 V.

A rectifier is built as shown below. Assume that the transformer is ideal and has a turns ratio of 1:1.



3.c) (3 pts) If the frequency of  $V_{in}$  is 1 kHz and it has an amplitude of 20 V, what is the dominant frequency of the output of the first rectifier,  $V_1$ ? Also, what is the dominant frequency of the signal being applied to the load resistor,  $V_2$ ?

A half-wave rectifier doubles the frequency of the signal, therefore:  $f_{V1} = 2 \text{ kHz}$

The second rectifier is acting on the rectified input, therefore doubled again:  $f_{V2} = 4 \text{ kHz}$

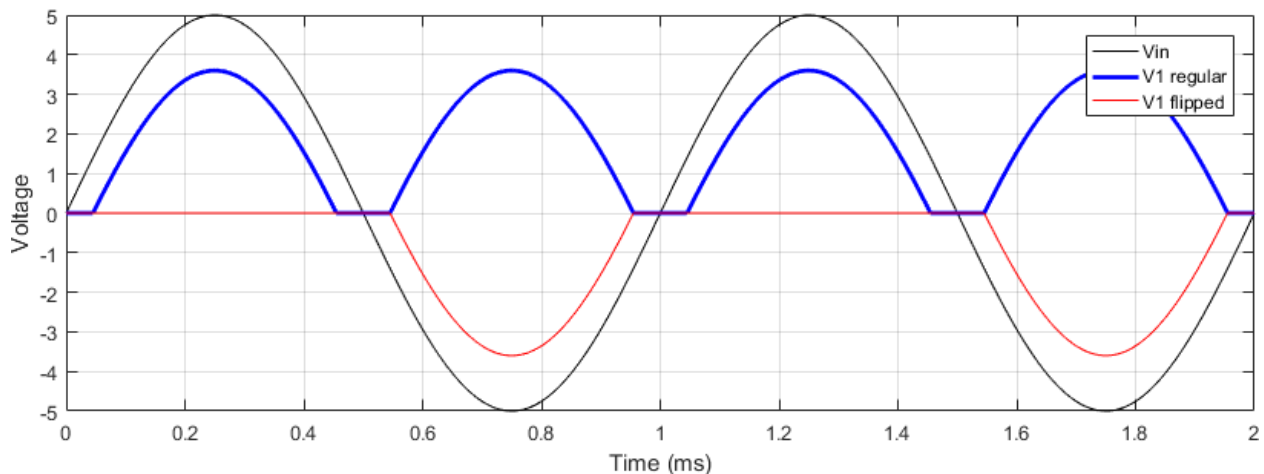
3.d) (2 pts) What is the purpose of the transformer in the above circuit?

The transformer removes the DC offset from the output of the first rectifier so that its oscillation is centered about 0. Without this, the second rectifier would only rectify the top half of the signal since the minimum voltage of the wave is 0V. This wouldn't be an issue if there was no ground on the second rectifier though.

3.e) (2 pts) How would your answer change for part 3.c if the transformer was removed, e.g., the top two wires were connected together and the bottom two wires were connected together?

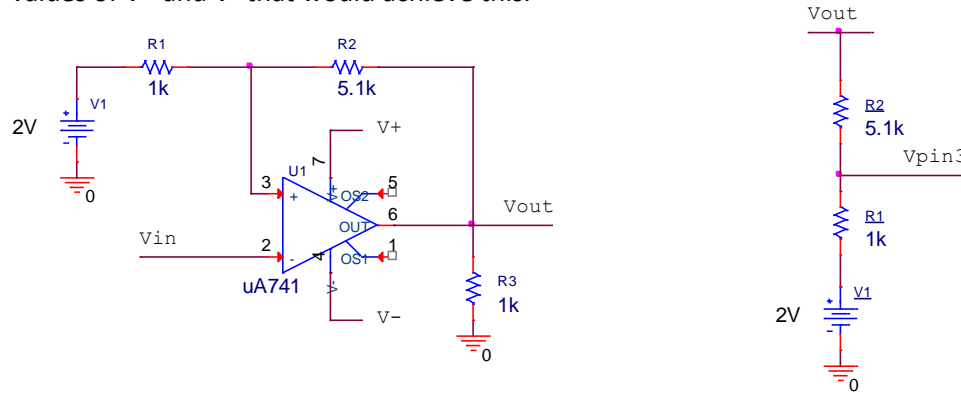
$V_2$  would not be doubled, it would remain at  $f_{V2} = 2 \text{ kHz}$

3.f) (4 pts) Sketch what you expect  $V_1$  to look like given  $V_{in}$ . Additionally, sketch  $V_1$  for the case where the orientations of diodes  $D_1$  and  $D_4$  were flipped (i.e.,  $D_1$  points in same direction as  $D_2$ , etc).



**Question Set 4) Comparators and Schmitt Triggers (18 pts)**

4.a) (4 pts) In the circuit below, it is desired to have the threshold voltages set to 3 V and 5 V. Select the values of V+ and V- that would achieve this.



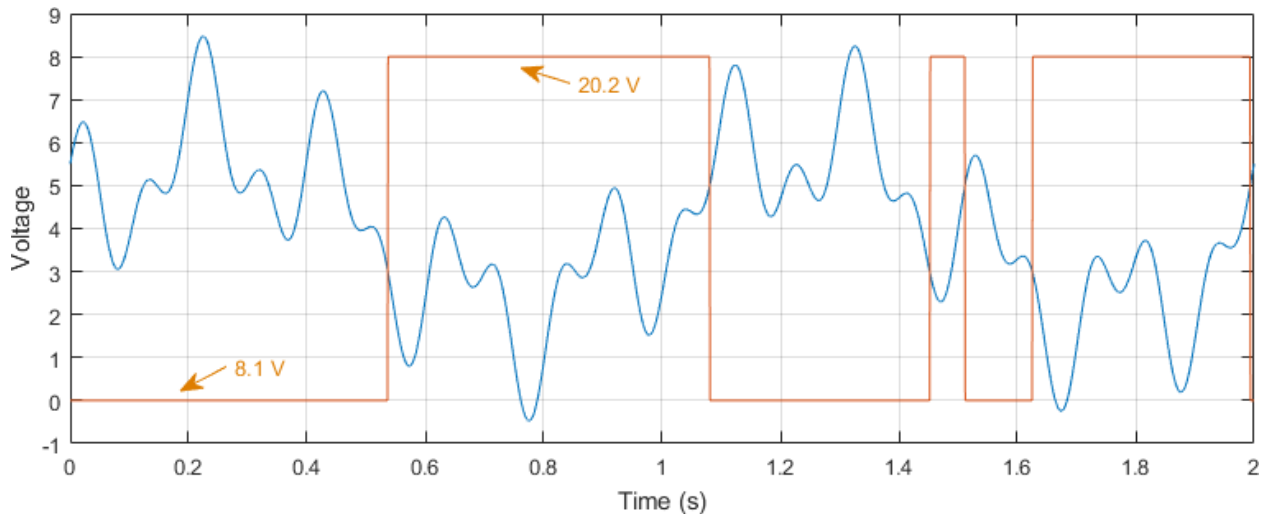
Vout can only be V+ or V- in this configuration. The voltage threshold is the value on pin3 of the op-amp. This may be represented by the voltage divider above-right.

$$V_{pin3} - V1 = (V_{out} - V1) \frac{R1}{R1 + R2} \rightarrow V_{pin3} - 2 = 0.164 (V_{out} - 2)$$

Solving the above for Vpin3 = 3V and 5V gives:

V-	8.10 V
V+	20.3 V

4.b) (4 pts) Below is a plot of the voltage on Vin. Considering your solution above, sketch the expected value of Vout. If the y-scale given doesn't meet your needs, clearly mark the important values on your added sketch.



4.c) (2 pts) In the circuit schematic of 4.a, R1 is replaced with a  $0\ \Omega$  valued resistor. What would you call the circuit now?

Comparator

4.d) (2 pts) In the circuit schematic of 4.a, pins 2 and 3 are switched such that  $V_{in}$  is now connected to the + input. What would you call the circuit now? Ignore the change from 4.c.

Non-inverting Amplifier.

4.e) (2 pts) Assume a  $100\ \Omega$  resistor was added in series between  $V_{in}$  and pin 2 of the schematic of 4.a. Assuming  $V_{in}$  is 4 V, determine what the voltage drop is across this resistor, if possible. If not possible, write "INDETERMINATE."

Current into the + and – pins of an op-amp is ideally 0 A; therefore no current is flowing through the resistor and the voltage drop is 0 V

4.e) (2 pts) On the crib sheet, we give you the schematic of an inverting comparator. How would you go about making a non-inverting comparator?

Switch the  $V_{ref}$  and  $V_{in}$  pins

4.f) (2 pts) Do you expect to take the optional final? Your answer here is NON-BINDING.

The optional final will:

- cover all topics in the class,
- Not have an LMS portion,
- generally be more difficult than the quizzes (mainly because of points above),
- replace your lowest quiz grade, which includes the LMS portion,
- NOT replace your lowest quiz grade, IF the final grade is the lowest.
  - That is: you cannot hurt you overall grade by attempting the final.

YES

NO