Experiment 7

**Submission Template**

# The following should be included in your experimental checklist. Everything should be labeled and easy to find. Credit will be deducted for poor labeling or unclear presentation. ALL PLOTS SHOULD INDICATE WHICH TRACE CORRESPONDS TO THE SIGNAL AT WHICH POINT AND ALL KEY FEATURES SHOULD BE LABELED.

**Hand written schematics are required for physically built circuits, ONLY!!!**

**Truth Tables:** Note for all truth tables generated, you should include a screen capture of the Static I/O (Waveforms) or Digital IO (Scopy) configuration for at least one of the input conditions (one of the rows of the table).

# Part A – Basic Logic Gates (12 pts)

A.1 NOR gate truth table and M2k/Analog Discovery screen capture of a single input/output configuration. (2 pt)

***Double click on picture placeholder to add plots/tables!!***



A.2 NAND gate truth table and M2k/Analog Discovery screen capture of a single input/output configuration. (2 pt)



A.3.NOT gate truth table and M2k/Analog Discovery screen capture of a single input/output configuration. (2 pt)



A.4. LTspice timing diagram for the three gates in the circuit with output traces marked. (2 pt)



Answer PART A questions:

1. How do the truth tables generated using the actual chips correspond to the truth tables you generated using your LTspice output? (2 pt

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1. If you had a gate with four inputs, how many cases would you have to consider to create its truth table? (2 pt)

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**Part B – Flip Flops (10 points)**

B.1. Flip flop truth table and M2k/Analog Discovery screen capture when inputs J = K = 1. (2 pt)

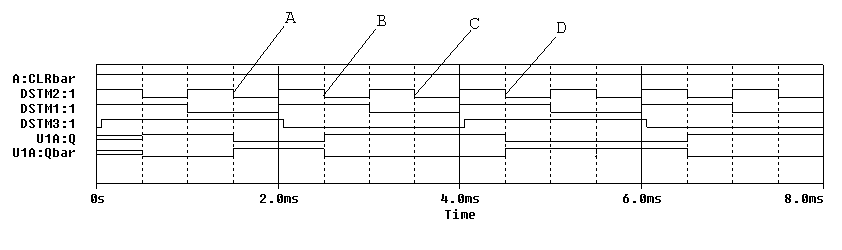


Answer the following questions:

1. Flip flops are called memory devices. Why do you think this is true? (2 pts)

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1. Show that the flip flop is giving the correct output at the clock cycles (A, B, C and D) indicated on the timing diagram in Figure S-1. DSTM2 is the clock signal, DSTM1 is J, and DSTM3 is K. Show how the truth table you found for the actual flip flop is consistent with the timing diagram at those four points. (6 pt)



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**Part C – Counters (14 points)**

Include the following plots (plots C.2-C.5 are best combined in the same figure):

C.1. LTspice timing diagram of counters. (2 pt)



Plot for C.2-C.5.

C.2. M2k/Analog Discovery plot of clock and QA. (2 pt)

C.3. M2k/Analog Discovery plot of clock and QB. (2 pt)

C.4. M2k/Analog Discovery plot of clock and QC. (2 pt)

C.5. M2k/Analog Discovery plot of clock and QD. (2 pt)



Answer the following questions:

1. For the counter circuit configuration just studied, what is the highest number it counts to in the time shown on your output? Express as both a binary and decimal number. (2 pt)

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1. What is the count value just before the second reset pulse and at what time does it reset? (1 pt)

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1. If 8 gates were used what is the maximum count that can be obtained, assuming no reset pulses? (1 pt)

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**Part D – The 555-Timer (36 points)**

D.1. LTspice plot for the astable circuit with R1 = 10k and R2 = 10k. (2 pt)



D.2 State the average value of the output voltage as determined by LTspice for the astable circuit with R1 = R2 = 10k. (1 pt)

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D.3 LTspice plot the astable circuit Vout with highest duty cycle and state the average value as determined by LTspice. (1 pt)



D.4. LTspice plot the astable circuit Vout with lowest duty cycle and state the average value as determined by LTspice. (1 pt)



D.5. M2k/M2k/Analog Discovery plot of output from 555-timer circuit when R1 = 1.5k, R2 = 6.8k and C1 = 0.1µF. (4 pt)



Answer the following questions:

1. What are the on-time, the off-time, and the period of the signal in plot D.1.? What are the calculated values for these? Are they consistent? (4 pt)

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1. What are the maximum and minimum values for the voltage across the capacitor C1 (at pins 2 and 6)? (Ignore the voltage at times before it reaches steady state.) Why do these values make sense? (3 pt)

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1. Calculate the value of τ (the decay constant) that controls the rate at which the capacitor C1 charges. Calculate the value of τ (the decay constant) that controls the rate at which the capacitor C1 discharges. (4 pt)

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1. What was the average voltage for your original circuit? What were the minimum and maximum average voltages when you considered different combinations of R1 and R2? (3 pt)

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1. What are the on-time, the off-time, and the period of the signal in plot D.5.? What are the calculated values for these? Are they consistent? (4 pt)

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1. How did you find the value for C1 that gave the circuit you built a one second period? What value did you find? (2 pt)

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1. What are the calculated on-time, off-time and period values for your circuit with the new capacitor? How do these relate to the initial values? Why? (4 pt)

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1. With the NE555 timer driving the 74393 counter, do the LEDs cycle as expected? Explain your answer. (3pts)

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**Organization:** Material should be in logical order, easy to follow and complete. Offer any comments below but none are required. (8pts)

**List group member *responsibilities*. (0 to -4pts)** During COVID classes: State in 25 words or less what was the group interaction. For example which group members, including yourself, actively helped others? If nobody did, state that, it is a valid response.

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**Summary/Overview** (0 to -10 pts) There are two parts to this section, both of which require revisiting everything done on this experiment and addressing broad issues. Grading for this section works a bit differently in that the overall report grade will be reduced if the responses are not satisfactory.

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***Experiment 7***

***Checklist w/ Signatures for Main Concepts***

INSERT SIGNED COPY OF CHECKLIST BELOW (OR ADD SCANNED PDF VERSION)



***Experiment 7***

***Hand Drawn Schematics***

INSERT HAND DRAWN SCHEMATICS FOR ALL CIRCUITS BUILT

