ENGR-4300
Spring 2010
Test 3

Name _____

Section 1(MR 8:00) 2(MR 4:00) 3(TF 8:00)
(circle one)

Question I (20 points) _____

Question II (20 points) _____

Question III (20 points) _____

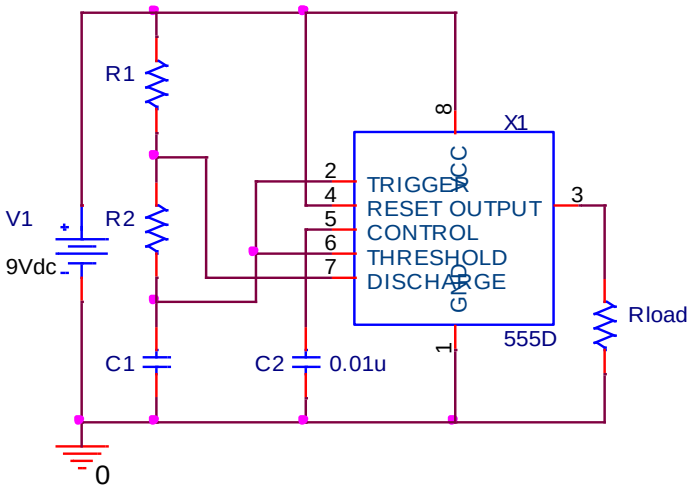
Question IV (20 points) _____

Question V (20 points) _____

Total (100 points): _____

On all questions: SHOW ALL WORK. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS. No credit will be given for numbers that appear without justification. ***Be sure to read the entire quiz before solving any problems.***

Question I – Astable Multivibrator (20 points)



1. (4pt) The 555 timer circuit shown is to have a duty cycle of 80% (4/5). For a given C1, what ratio of resistors R1/R2 will produce this duty cycle

$$T1 = 0.693(R1 + R2)C1$$

$$T = 0.693(R1 + 2R2)C1$$

$$\frac{T1}{T} = \frac{0.693(R1 + R2)C1}{0.693(R1 * 2R2)C1} = \frac{R1 + R2}{R1 + 2R2} = .8$$

$$\frac{R1}{R2} = 3$$

2. (4pt) Using this ratio of R1/R2 and C1 = 10μF, calculate the values for R1 and R2 needed to yield a frequency of 20Hz.

$$f = \frac{1.44}{(R1 + 2R2)C1} = 20 = \frac{1.44}{(3R2 + 2R2)10^{-5}}$$

$$R2 = 1.44k \text{ and } R1 = 4.32k$$

3. (2pt) For an ideal 555, what are the maximum and minimum voltages on pin 2 above during normal operation?

Max = 6V, Min = 3 because of the internal divider of the 555

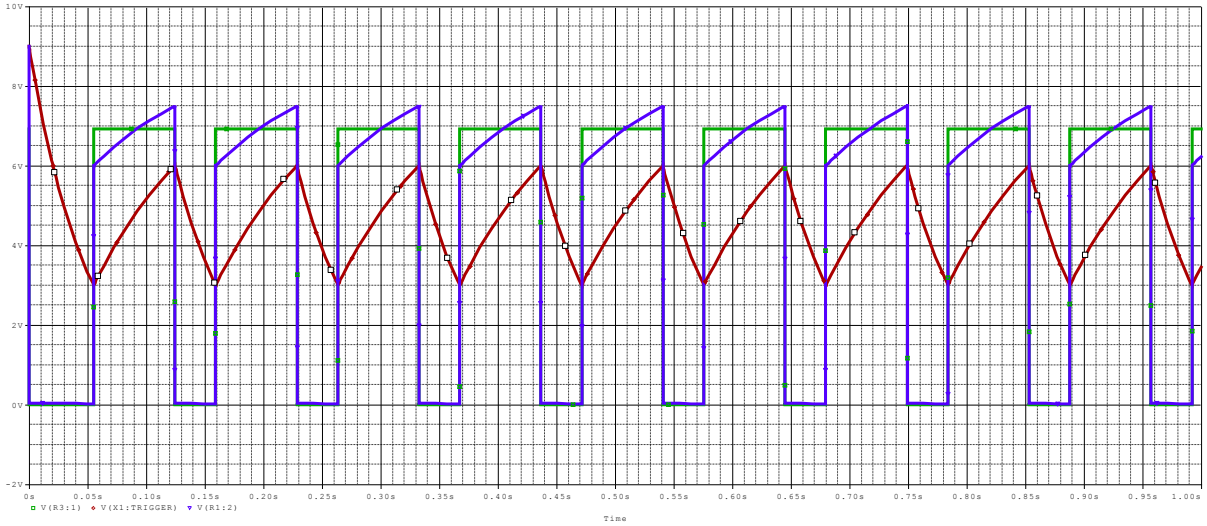
4. (4pt) For an ideal 555, what are the maximum and minimum voltages on pin 7 above during normal operation?

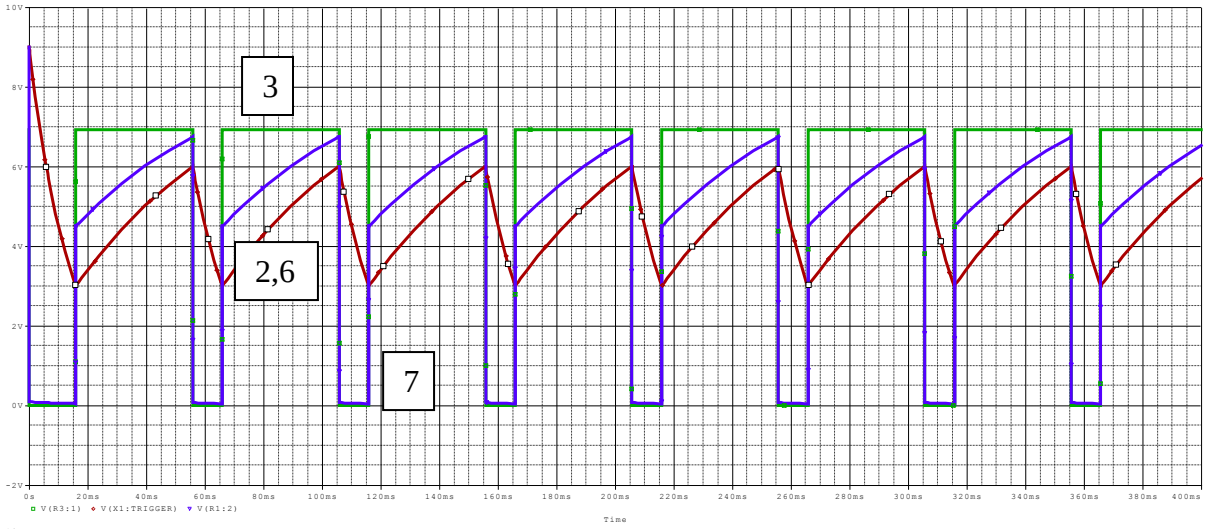
Min = 0 since on pin 7 the transistor connects to zero
Max = 6V plus the voltage across R2 or 6 + (0.25)3=6.75V

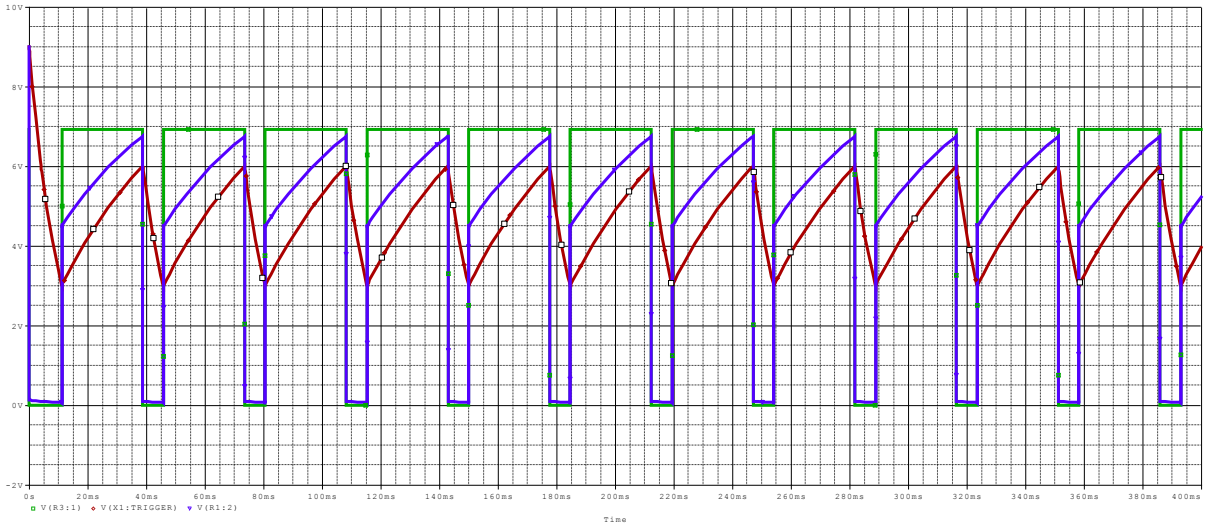
On the next page, the freq must be 20 Hz so the period must be 1/20=50ms so the 3rd plot is out. The 2nd plot has the correct frequency. The first plot does not have an 80% duty cycle, so it has to be the middle plot. The individual curves must satisfy the voltages listed above so they are as labeled.

Question I – Astable Multivibrator (continued)

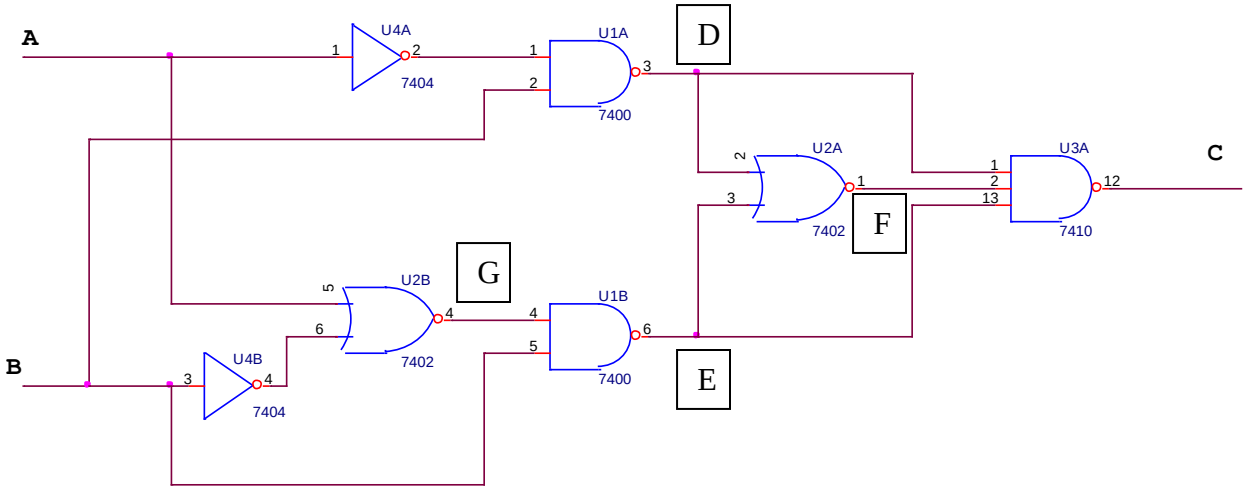
5. (6pt) Which of the sets of plots below shows the voltages on pins 2, 3, 6 and 7 for the case considered here? Label which plot is which in the correct figure.





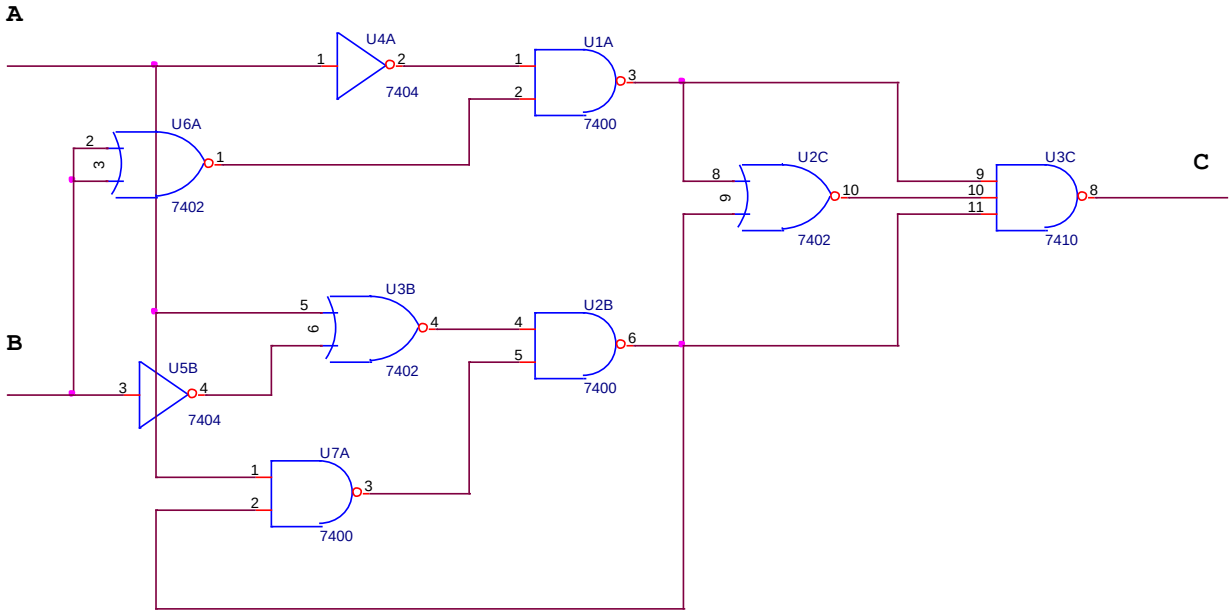


Question II – Combinational Logic Circuits (20 points)



1. Complete the table below for the circuit above (***8 pts***: all or nothing, continuation of mistakes will be deducted)

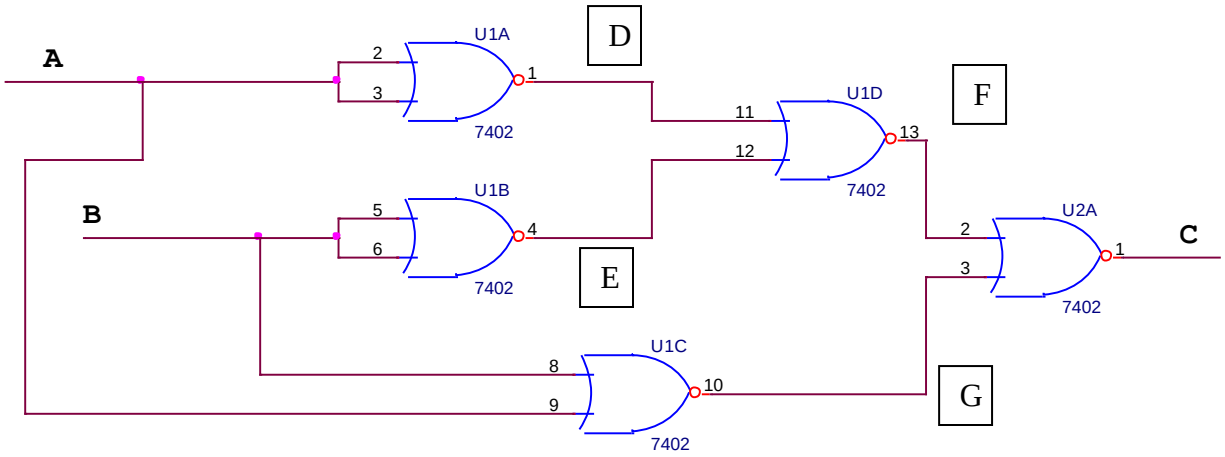
A	B	Not A	Not B	G	D	E	F		C
0	0	1	1	0	1	1	0		1
0	1	1	0	1	0	0	1		1
1	0	0	1	0	1	1	0		1
1	1	0	0	0	1	1	0		1



2. Complete the table below for the circuit above (6 ***pts***: all or nothing, continuation of mistakes will be deducted)

A	B		Mehmed		Chris				C
0	0		Abouzar		Dylan				
0	1		David		Dave				
1	0		Yiran						
1	1		Jun				Last	Names	OK

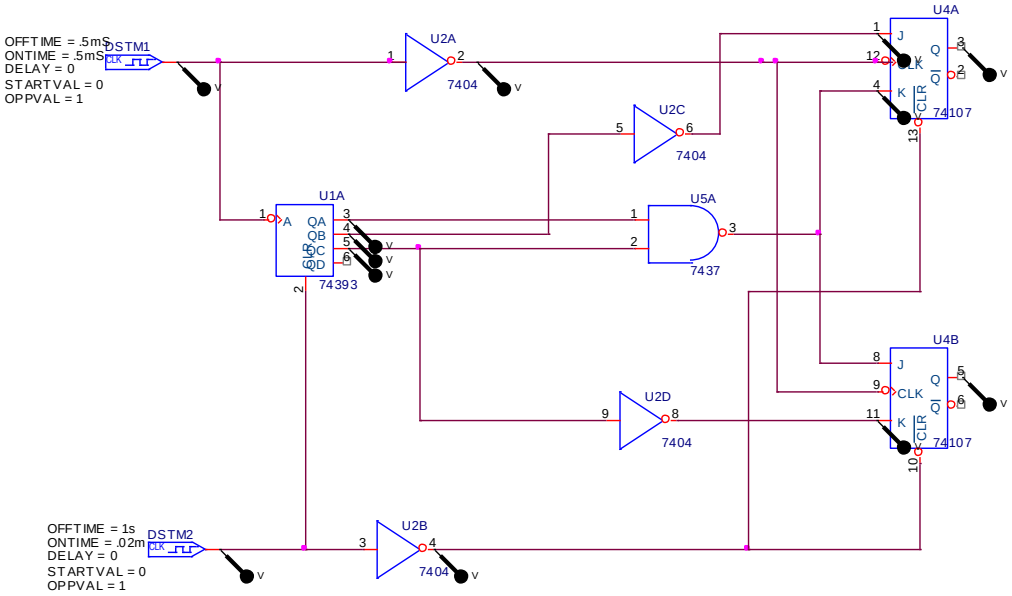
Question II – Combinational Logic Circuits (continued)



3. Complete the table below for the circuit above (6***pt***: all or nothing, continuation of mistakes will be deducted) This combination of gates performs the function of a single gate. Identify that gate. XOR

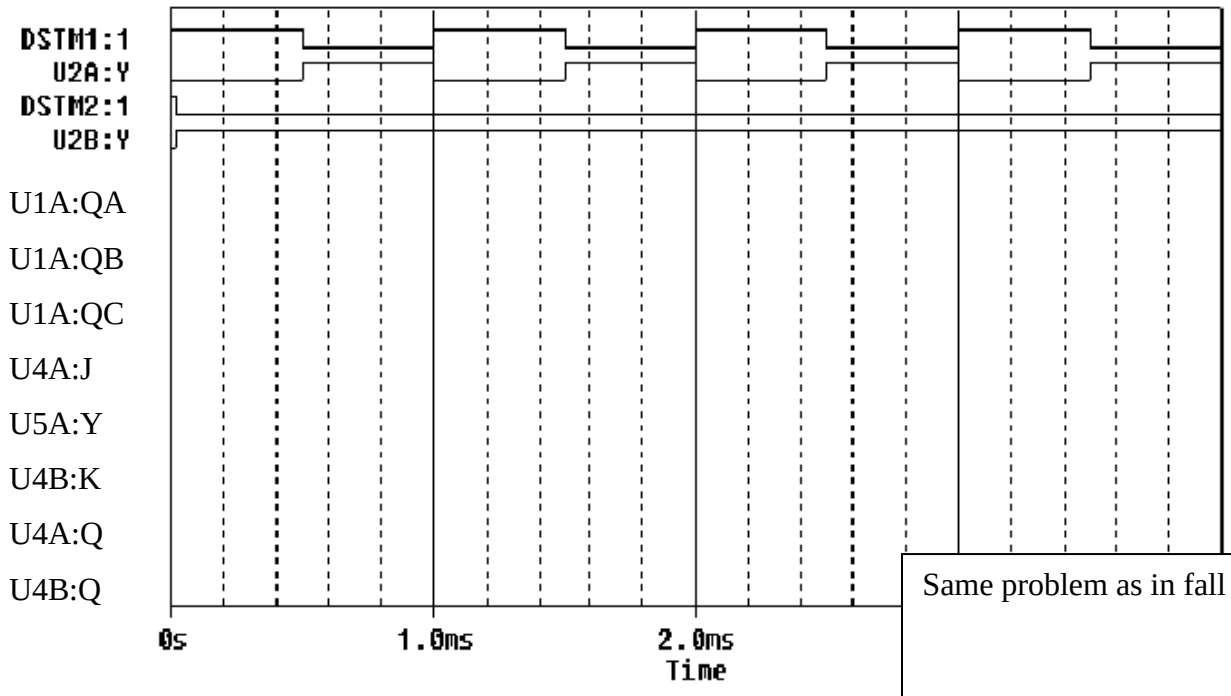
A	B	D	E	F	G				C
0	0	1	1	0	1				0
0	1	1	0	0	0				1
1	0	0	1	0	0				1
1	1	0	0	1	0				0

Question III – Sequential Logic Circuits (20 points)



In the circuit pictured above, clock DSTM1 provides a clock signal to a counter and two flip flops. The flip flops are clocked one half cycle after the counter to allow for propagation of the signals through the gates. (The counter changes on the negative edge of DSMT1 and the flop flops change on the negative edge of U2A:Y.) DSTM2 provides an initial reset pulse to both chips. This is required by PSpice to ensure that all sequential devices start in a known state.

1. The timing diagram below shows the reset pulses and the clock signals. Sketch the following signals in the space provided: the output from the counter (U1A:QA, U1A:QB, & U1A:QC); the output from the combinational logic (U2C:Y=U4A:J, U5A:Y=U4A:K=U4B:J, & U2D:Y=U4B:K); and the output from the flip flops (U4A:Q & U5A:Q). (2pt per trace = ***16pt***)



Same problem as in fall 2008

2. A 4-bit counter is cleared and then receives a string of clock pulses. What are QA, QB, QC and QD after 9 clock pulses? Clearly indicate the state of each signal. (***2pt***)

QD	QC	QB	QA

1001 is the number 9

3. A 4-bit counter is cleared and then receives a string of clock pulses. What are QA, QB, QC and QD after 25 clock pulses? Clearly indicate the state of each signal. (***2pt***)

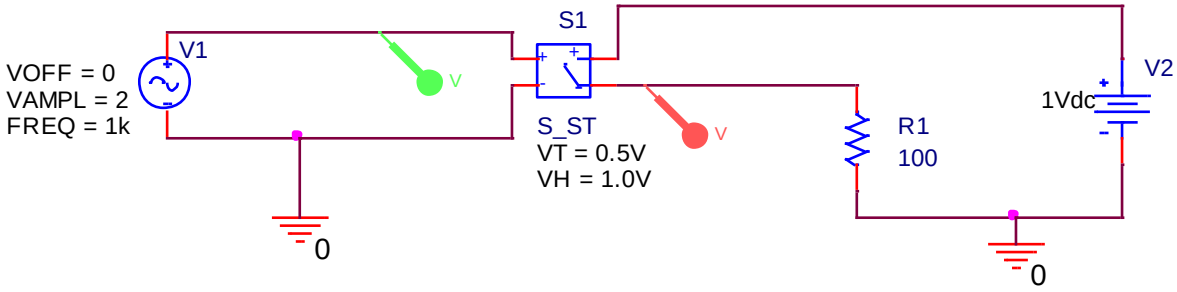
QD	QC	QB	QA

25 – 16 = 9 so it is 1001, it cycles through the entire 1 to 15 back to 0 (sixteen steps) then 9 more steps to get to 25 clock pulses.

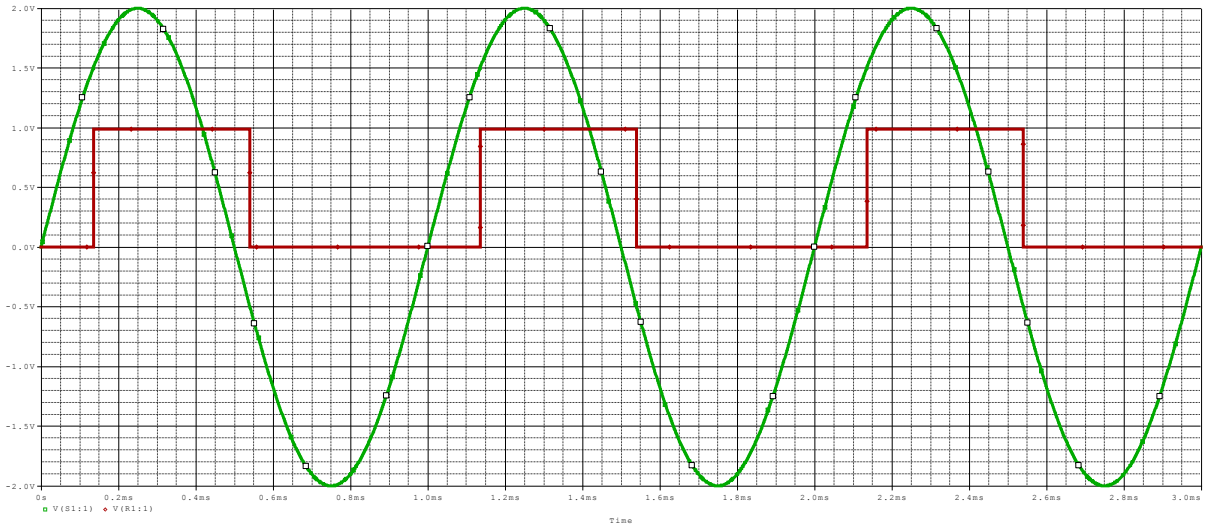
Question IV – Switching Circuits (20 points)

Another Switch from PSpice

1. In the PSpice library, there are many devices modeled that we have not yet studied. One such device is shown in the circuit below.



The source voltage and the voltage at the bottom right pin of this device are shown below.



(4pt) Using the information from the circuit diagram and from the plot, determine the switching rules for this device in terms of VT and VH.

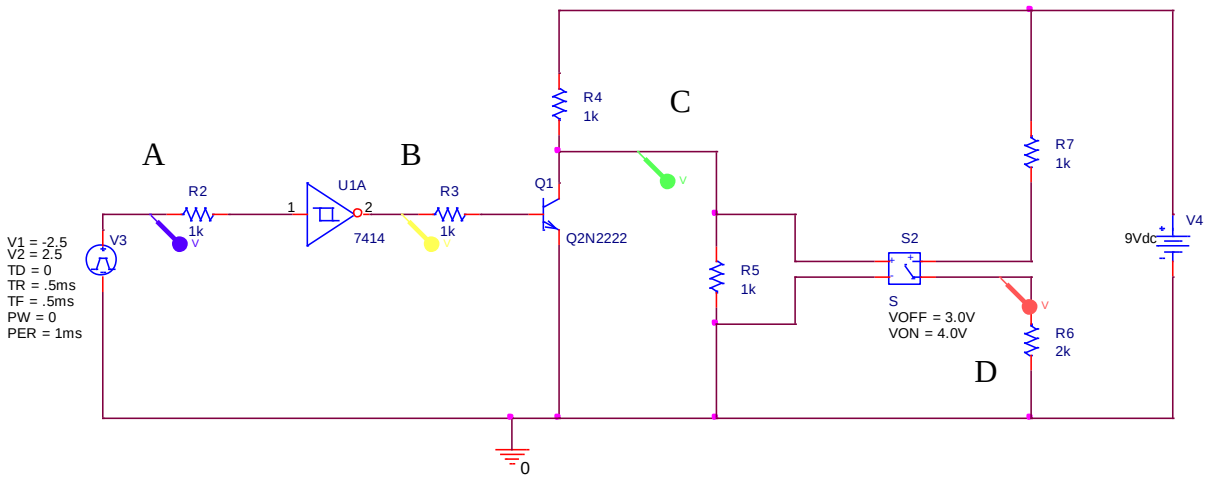
It is switching at 1.5V and -.5V or at VT+VH and VT-VH

(1pt) What does the H stand for in VH?

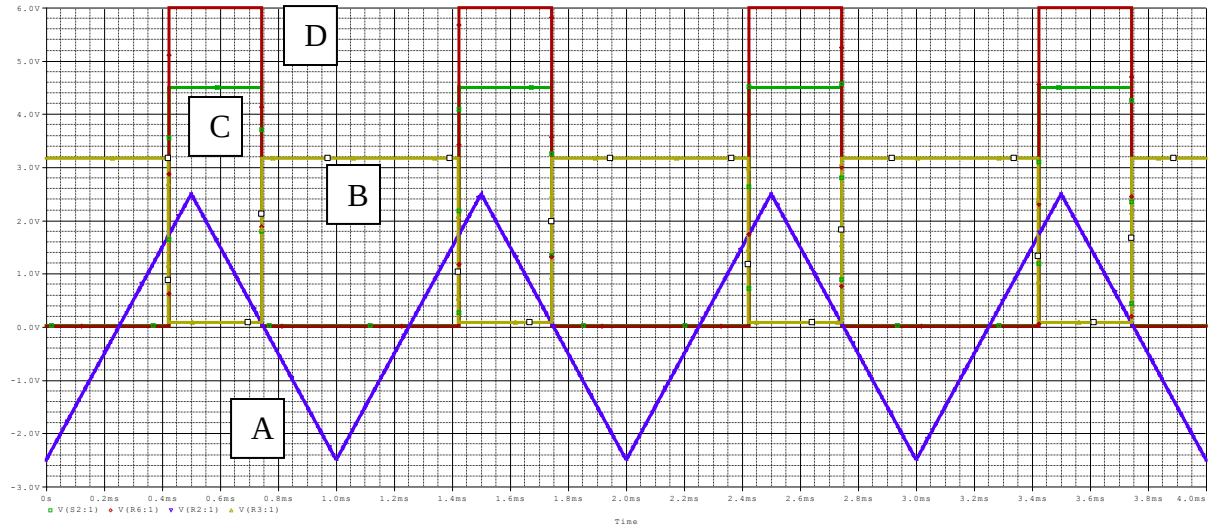
Hysteresis … the hysteresis is actually 2VH

Relay Model

2. Using a variation of this switch, we can model a relay



(8pt) Running PSpice, we can observe the voltages at the 4 locations indicated above. Label which is which in the figure below.



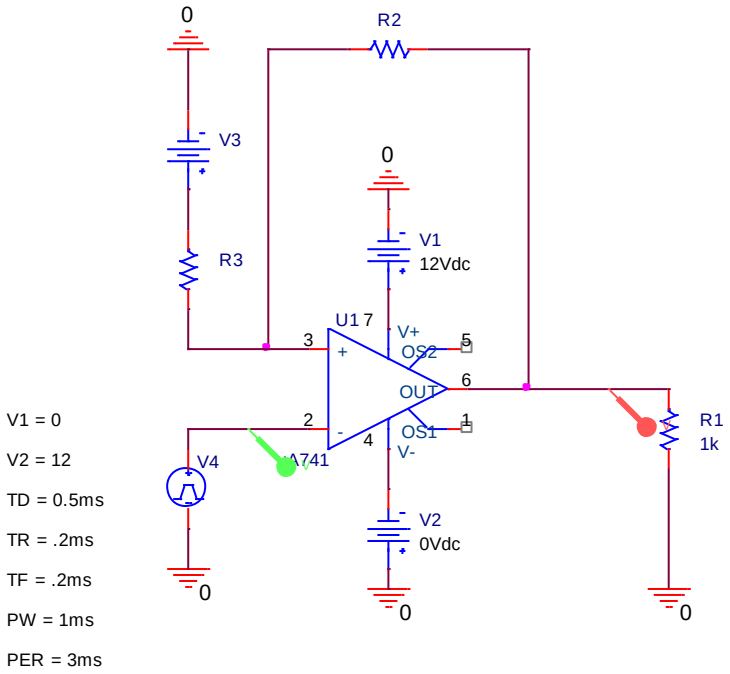
3. (6pt) Assume that we replace the source with a DC voltage of either 5V or 0V. Fill out the following table with the voltages at the four locations. Close answers are OK.

A	B	C	D
0V	3.15	0	0
5V	.05	5	6

4. (1pt) In problem II, you will receive full credit for part 2 if you write the name (first or last) of any teaching assistant in this course in the table. Now back to this question. For the following figures, circle any that are not switches. All are switches

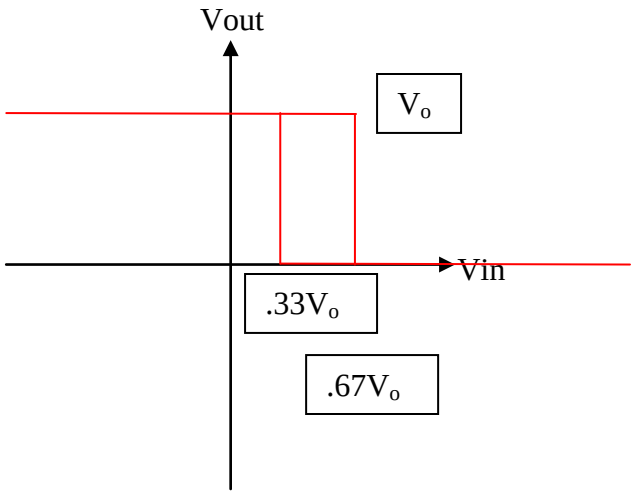
Question V – Comparators and Schmitt Triggers (20 points)

There are almost unlimited applications of light sensors (more on these in Experiment 8) including such simple and important devices as the beam break sensors used to protect children from closing garage doors. The Schmitt Trigger plays a critical role in the design of such devices. In the circuit below, the voltage source represents the signal coming from the light sensor. The output of the Schmitt Trigger is then used to control the power to some device, such as a garage door.



1. (2pt) What property of the Schmitt Trigger is being used in such an application?
Hysteresis

2. (3pt) Assume that we wish to design a system that turns off the garage door power when the signal from the light beam drops to 2/3 of its typical value (call it V_o) and then turns it back on at 1/3 of its typical value. On the axes below sketch the general input-output curve for this application. Be sure to scale both axes.



Question V – Comparators and Schmitt Triggers (continued)

3. (6pt) Set up the equations to find appropriate values for R2, R3, and V3 in the circuit above in terms of the op-amp's supply voltages and the desired switch points for the light beam detector.

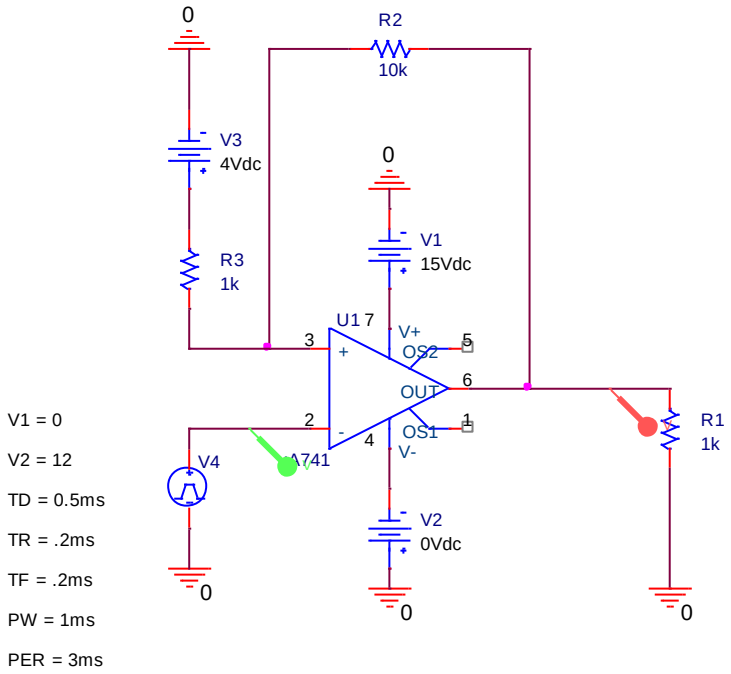
$$v+ = \left(\frac{R_3}{R_2 + R_3}\right)(v_{out} - V3) + V3 \text{ so that } v+ = \left(\frac{R_3}{R_2 + R_3}\right)(12 - V3) + V3 \text{ and}$$

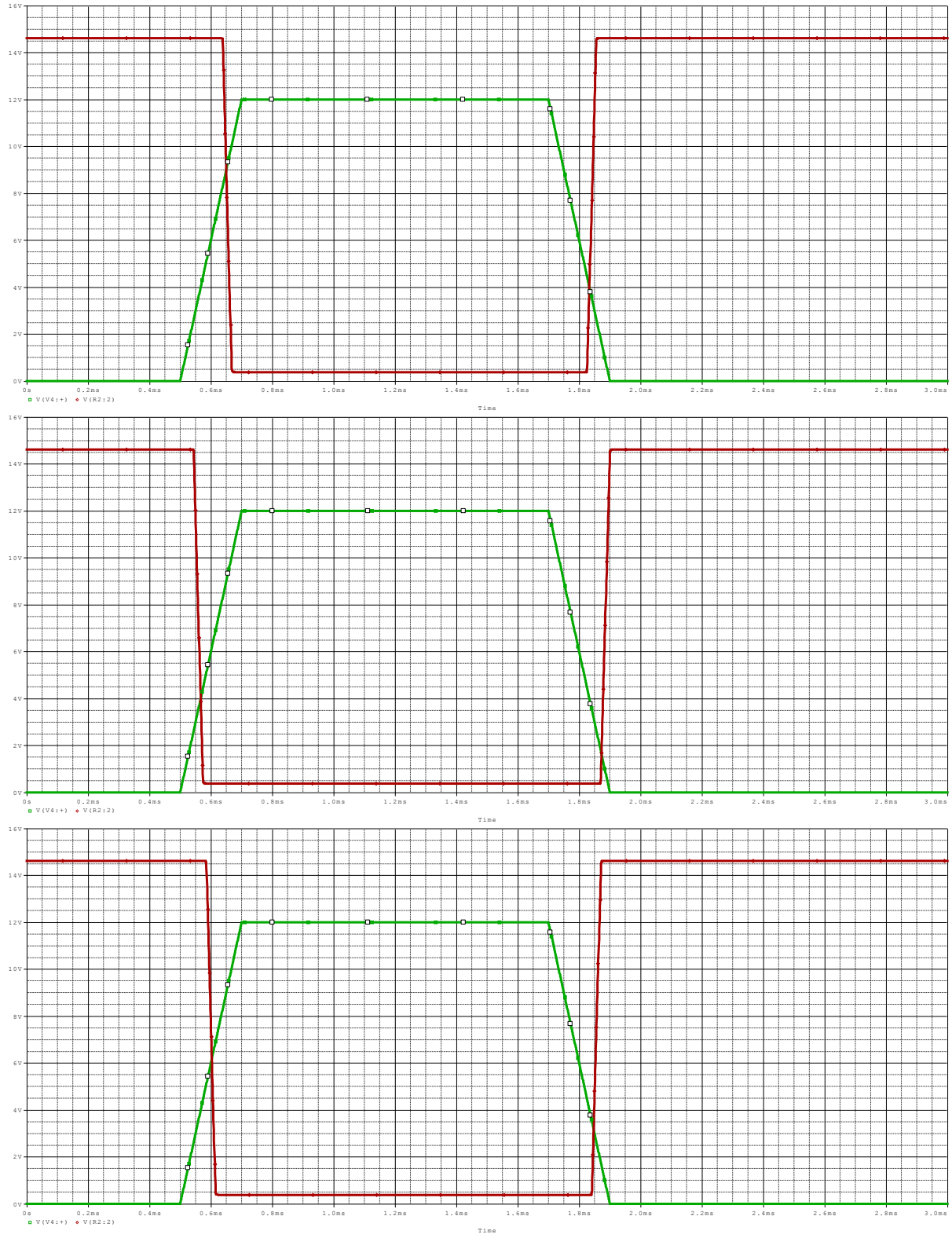
$$v+ = \left(\frac{R_3}{R_2 + R_3}\right)(0 - V3) + V3$$

5. (4pt) Given that R3 = 2k, find the values of R2 and V3. (hint: two equations two unknowns: simplify $v+_{high}$ and/or $v+_{low}$)

R2 = 4k and V3 = 6V

6. (5pt) If the circuit below is built (note: new op-amp V+ supply), which of the following plots correctly shows the voltage at the load for the given input conditions?





$v+ = \frac{1}{11}(15-4)+4 = 5$ and $v+ = \frac{1}{11}(0-4)+4 = 3.6$ so it is the bottom plot. It is hard to read the numbers exactly, but the others are quite far from these values.