ENGR-4300
Fall 2007
Test 3

Name _____SOLUTION_____

Section 1(MR) 2(TF)
(circle one)

Question I (20 points) _____

Question II (20 points) _____

Question III (20 points) _____

Question IV (20 points) _____

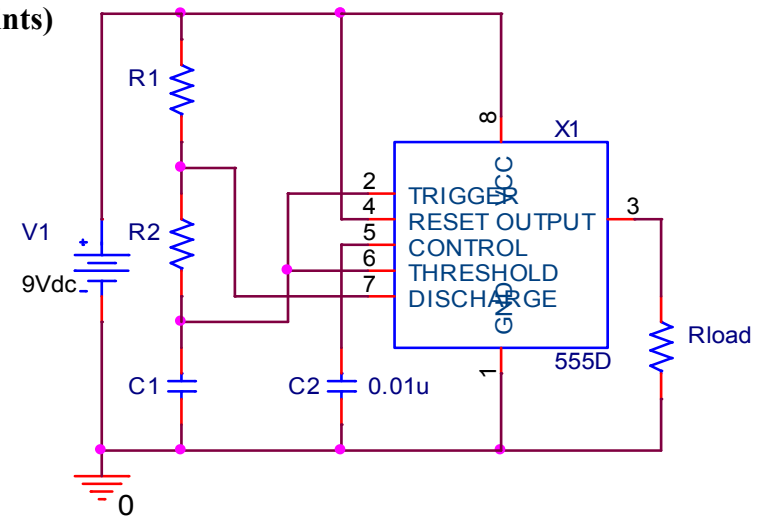
Question V (20 points) _____

Total (100 points): _____

On all questions: SHOW ALL WORK. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS. No credit will be given for numbers that appear without justification.

Question I – Astable Multivibrator (20 points)

The 555 timer circuit shown is found to have an output on pin 3 plotted below.



1. (1pt) Find the period of the output signal.

50µs

2. (3pt) From the plot determine the duty cycle of the output.

Duty cycle = T1/T
= 40µs/50µs = 80%

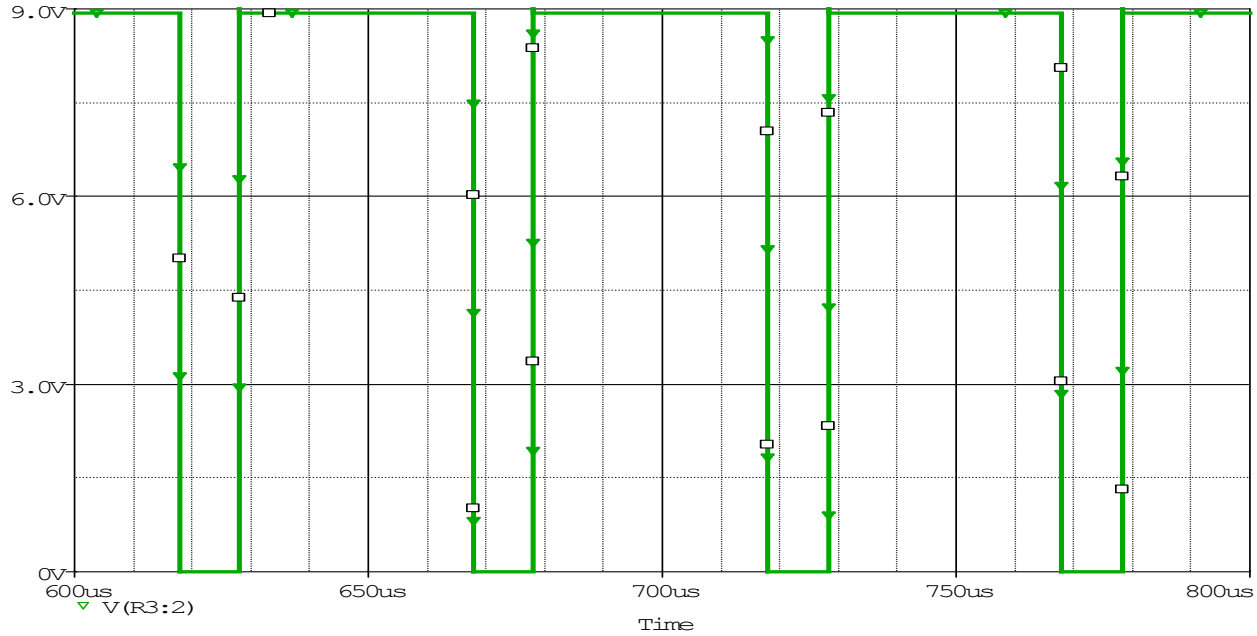
3. (3pt) Assuming that R1 = nR2, find the value of n from the duty cycle found in 2.

80% = [R1 + R2]/[R1 + 2R2] = [(n+1)R2]/[(n+2)R2]
4/5 = (n+1)/(n+2) => n = 3

4. (2pt) For R2 = 1k, find R1.

R1 = 3R2 = 3 x 1kΩ = 3kΩ

5. (8pt) Add traces to the plot sketching the voltages on pin 2 and 7 of the circuit above and be sure to label each.



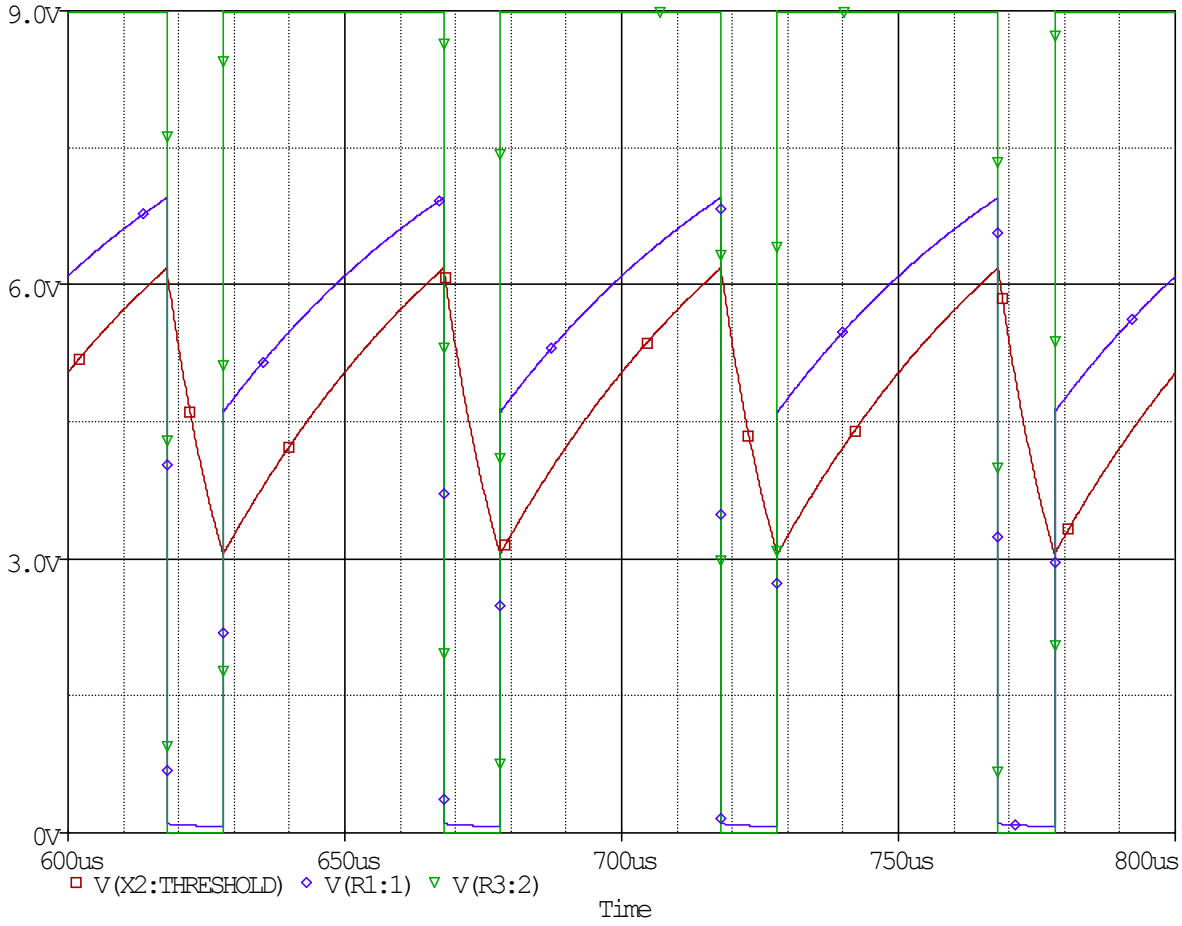
Question I – Astable Multivibrator (continued)

6. (2pt) For the period found in 1. and the resistors in 4. find the value of C1.

T = (R1 + 2R2)C1/1.44
C1 = (1.44T)/(R1 +2R2) = (1.44 x 50µ)/(3k + 2k) = 0.0144µF

7. (1pt) Find the average voltage of the output signal on pin 3.

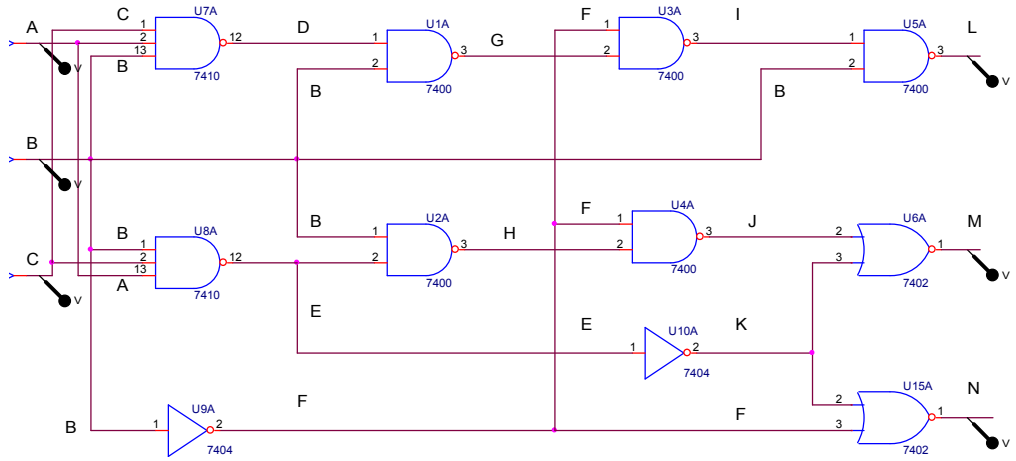
Vavg = (duty cycle) x 9V = 0.80 x 9V = 7.2V



Vpin2 swings between 3V and 6V (1/3 & 2/3 of 9V)
Vpin7 is either grounded (0V) or R2/(R1 + R2) = 1/4 of the voltage between Vpin2 and 9V

Question II – Combinational Logic Circuits (20 points)

1. (14pt) For the following circuit, complete the truth table. That is, find the three outputs for all possible input conditions. Note that it is not necessary to fill out the entire table of values at all possible locations in the table, but this is the best way to solve this problem. It will also help us to understand where you may have gone wrong if your answers for the three outputs are not correct. Note that the circuit is very well labeled so you can easily identify which location goes with each letter.

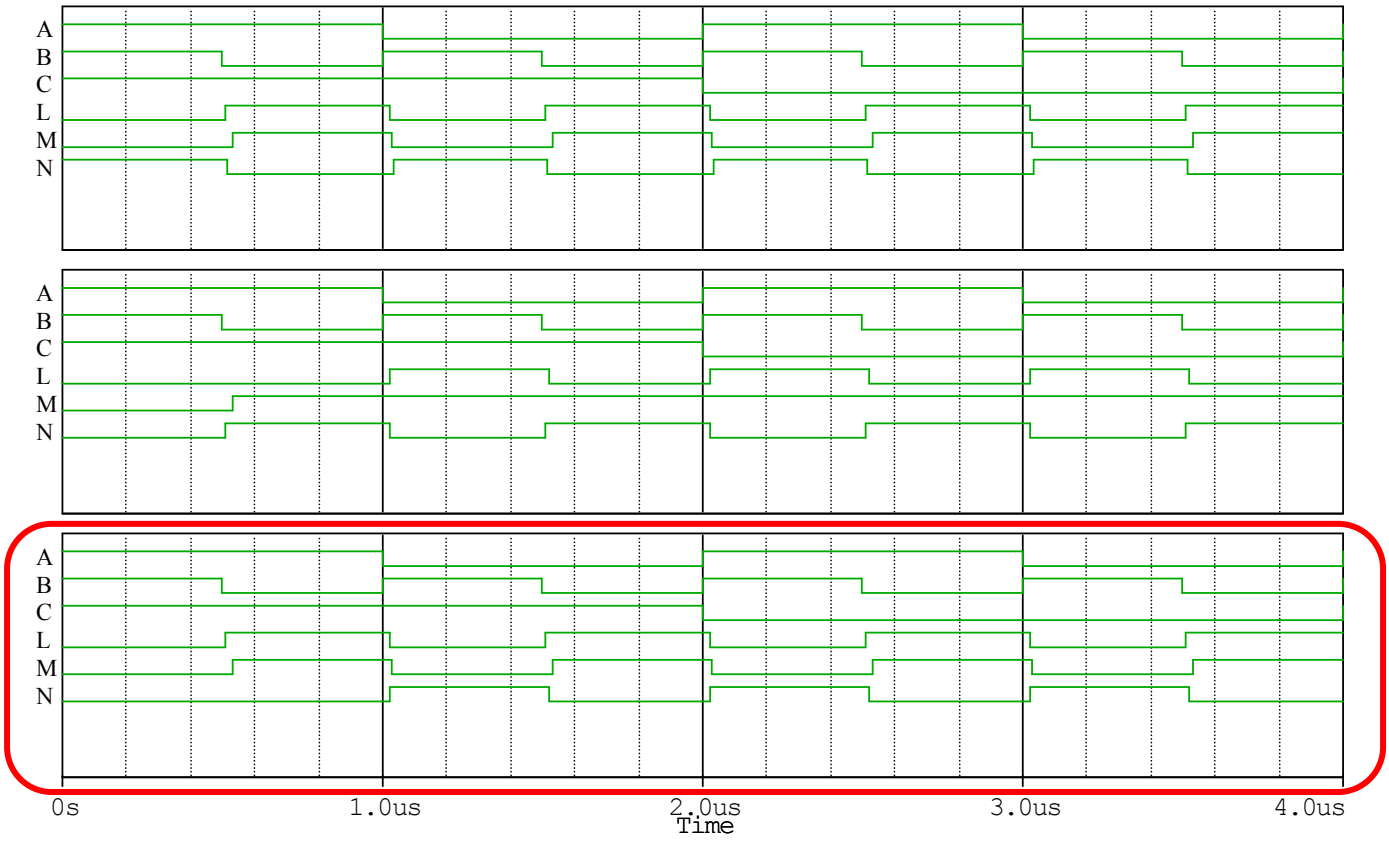


A	B	C	D	E	F	G	H	I	J	K	L	M	N
0	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**0**
0	0	1	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**0**
0	1	0	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**
0	1	1	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**
1	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**0**
1	0	1	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**0**
1	1	0	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**
1	1	1	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**

NOTE FROM CIRCUIT: D = E, F = NOT(B), G = H, I = J, K = NOT(E)

Question II – Combinational Logic Circuits (continued)

2. (6pt) PSpice is used to determine the timing diagram for this circuit. Shown below are three possible outputs L, M, N for the given three inputs A, B, C. The top three timing traces are for the inputs and the bottom three traces are for the outputs. Which of the three cases shown corresponds to the given configuration? Note that the beginnings and ends of each pulse do not exactly coincide with the input pulse trains. This is because there some inherent delays in the system. However, the bulk of each pulse does line up with the inputs. Circle the correct set of traces and **explain** your answer.



This is the only timing diagram that matches the table for at least the first (000) and last (111) cases.

Note that they correspond to this truth table. L and M must be the same traces and N has 5 low and 3 high states

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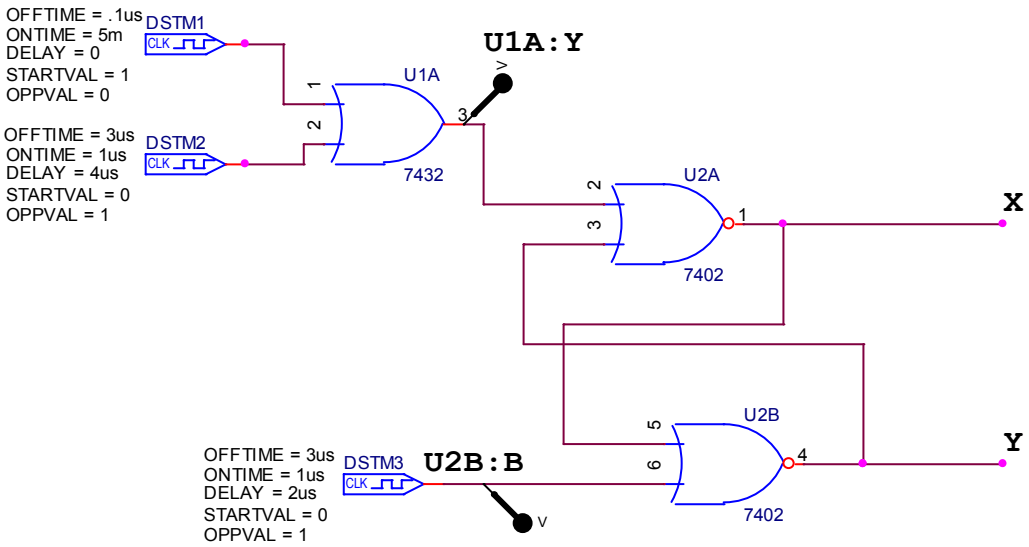
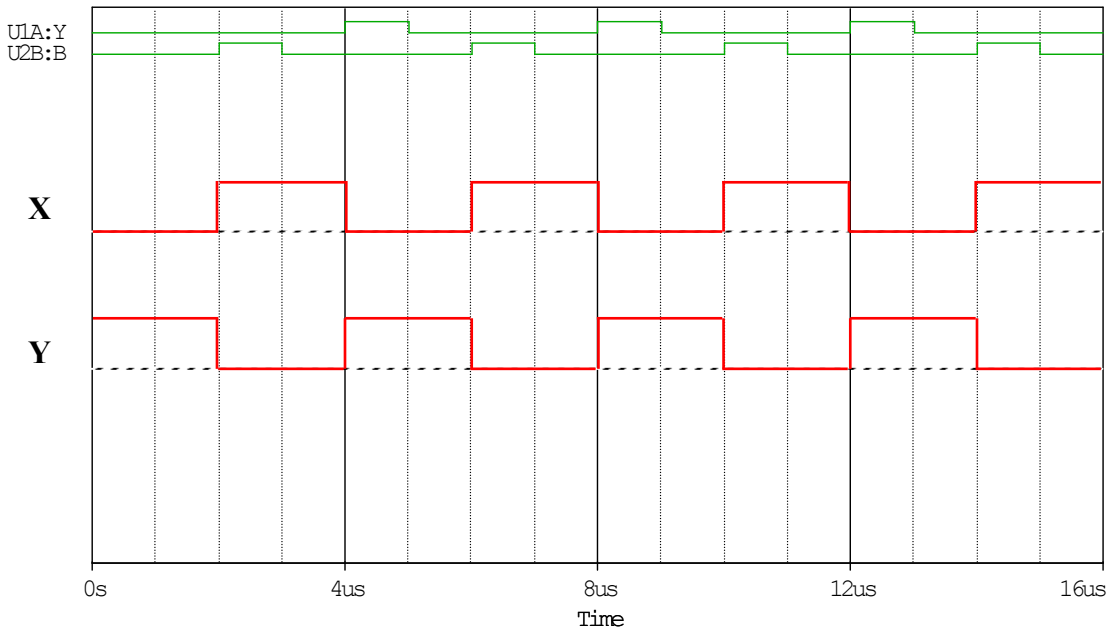
Question III – Sequential Logic Circuits (20 points)

1. (4pt) In the circuit below, the timing traces at nodes U1A:Y and U2B:B are shown below. You don't need to worry about the details of the clocks. Assume that X starts low. Plot the time trace for X and Y.

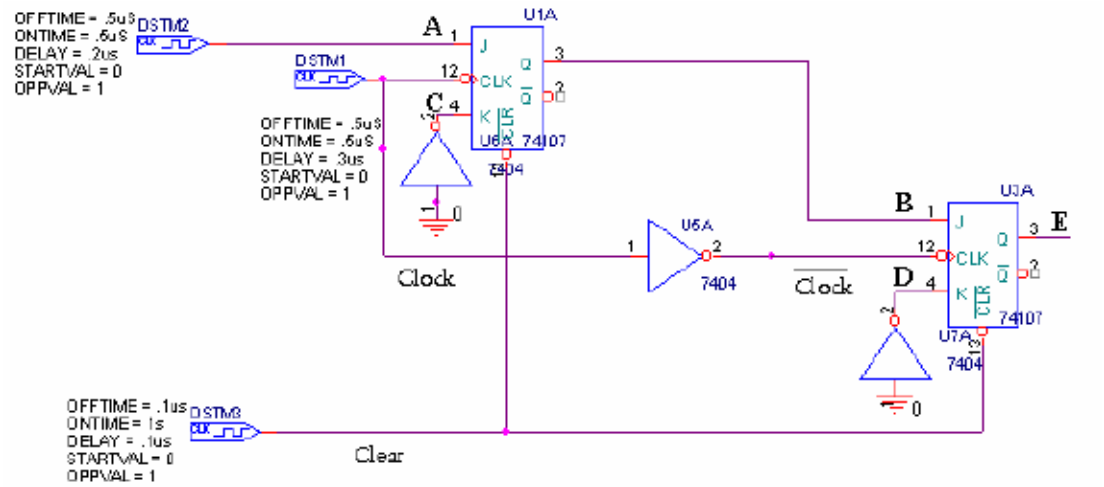




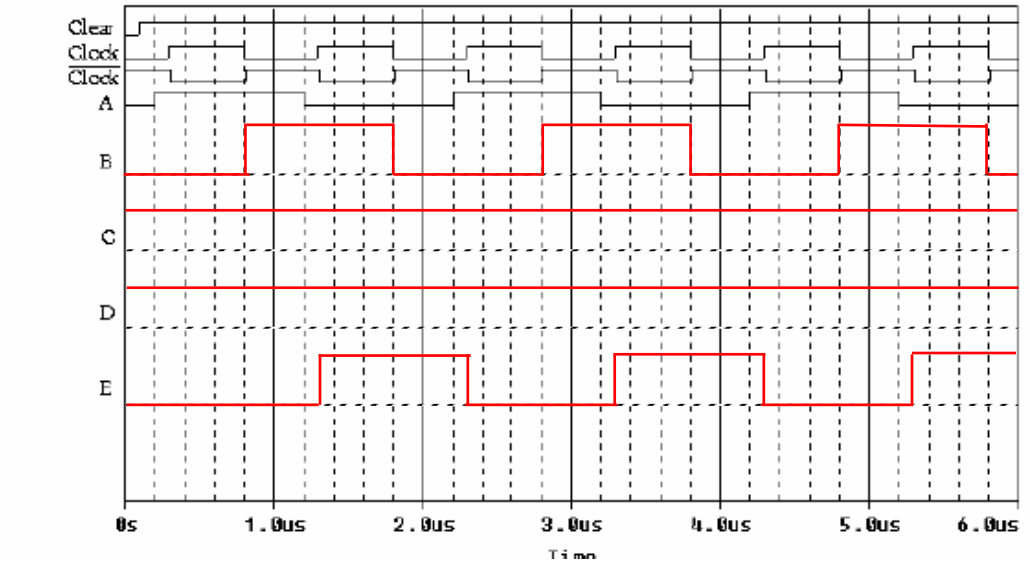
Question III – Sequential Logic Circuits (continued)

Flip Flops and Counters

The following is a diagram of a circuit from PSpice. The "Clear" signal initializes the flip flop. Therefore, once it goes high, the flip flop outputs Q=0 and Q_bar=1. The clock for the first flip flop is DSTM1 and the clock for the second flip flop is DSTM1 *inverted.* Remember that the flip flops and counters trigger on the falling edge of the clock pulse.



2. (12pt) The following diagram shows the clear signal, the clocks and the input at A. Draw the traces at B, C, D, and E. (8 points)



Question III – Sequential Logic Circuits (continued)

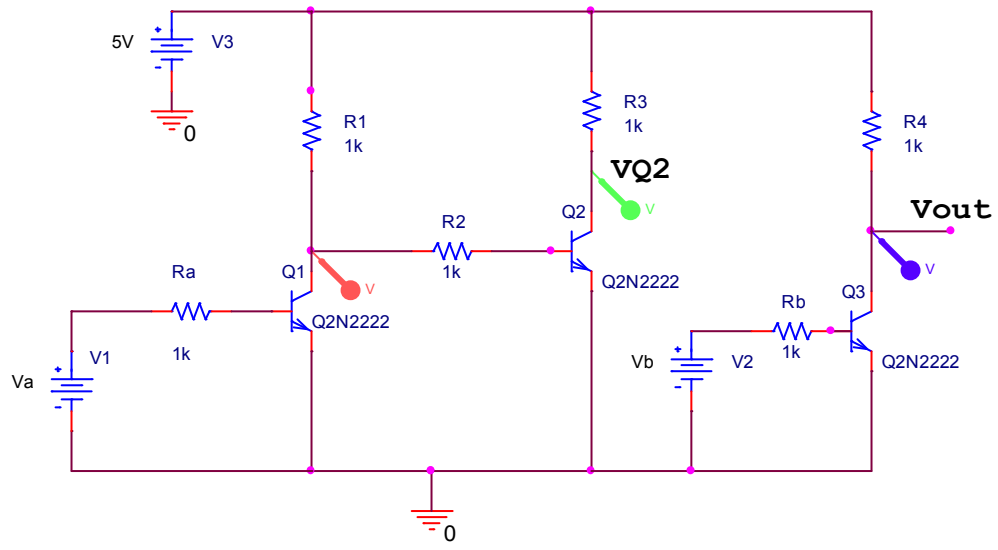
3. (2pt)A 4-bit counter is cleared and then receives a string of clock pulses. What are QA, QB, QC and QD after 9 clock pulses? Clearly indicate the state of each signal.

QD	QC	QB	QA
1	**0**	**0**	**1**

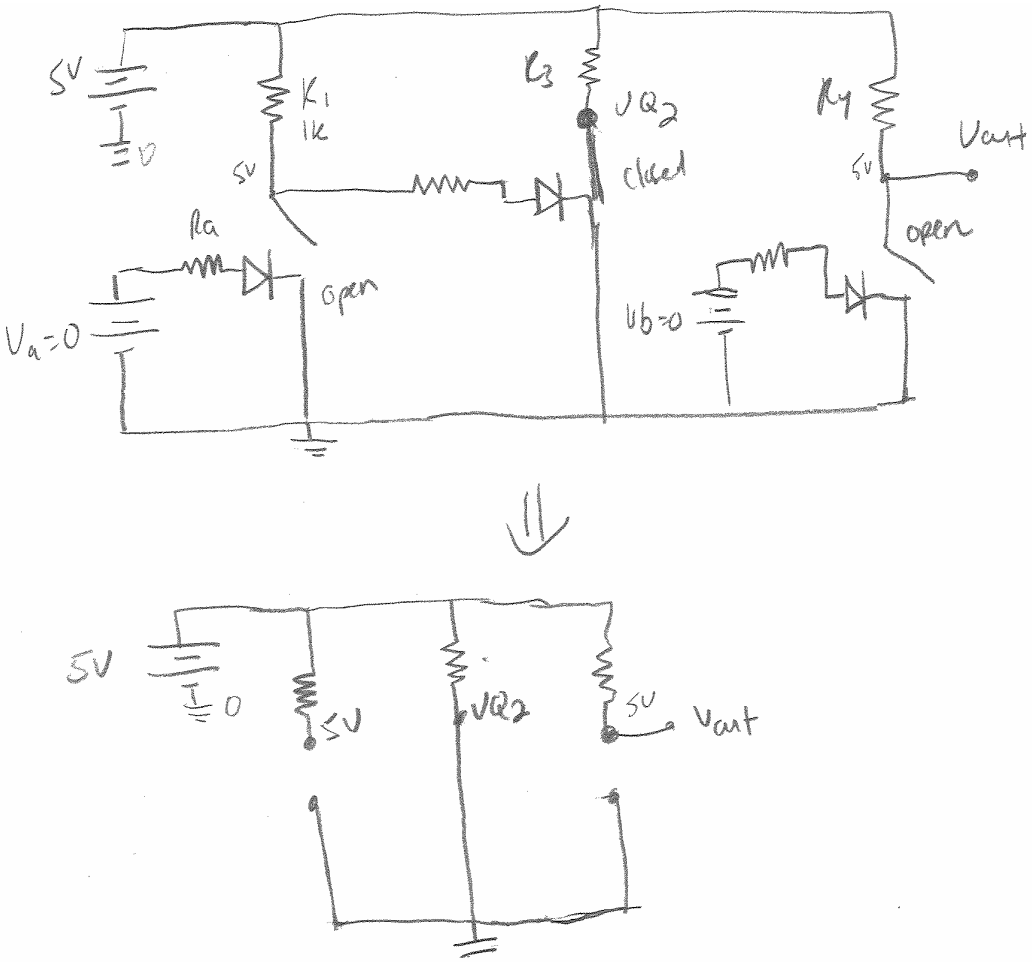
4. (2pt) What are QA, QB, QC and QD after 19 clock pulses? Clearly indicate the state of each signal. (2pt)

QD	QC	QB	QA
0	**0**	**1**	**1**

Question IV – Switching Circuits (20 points)

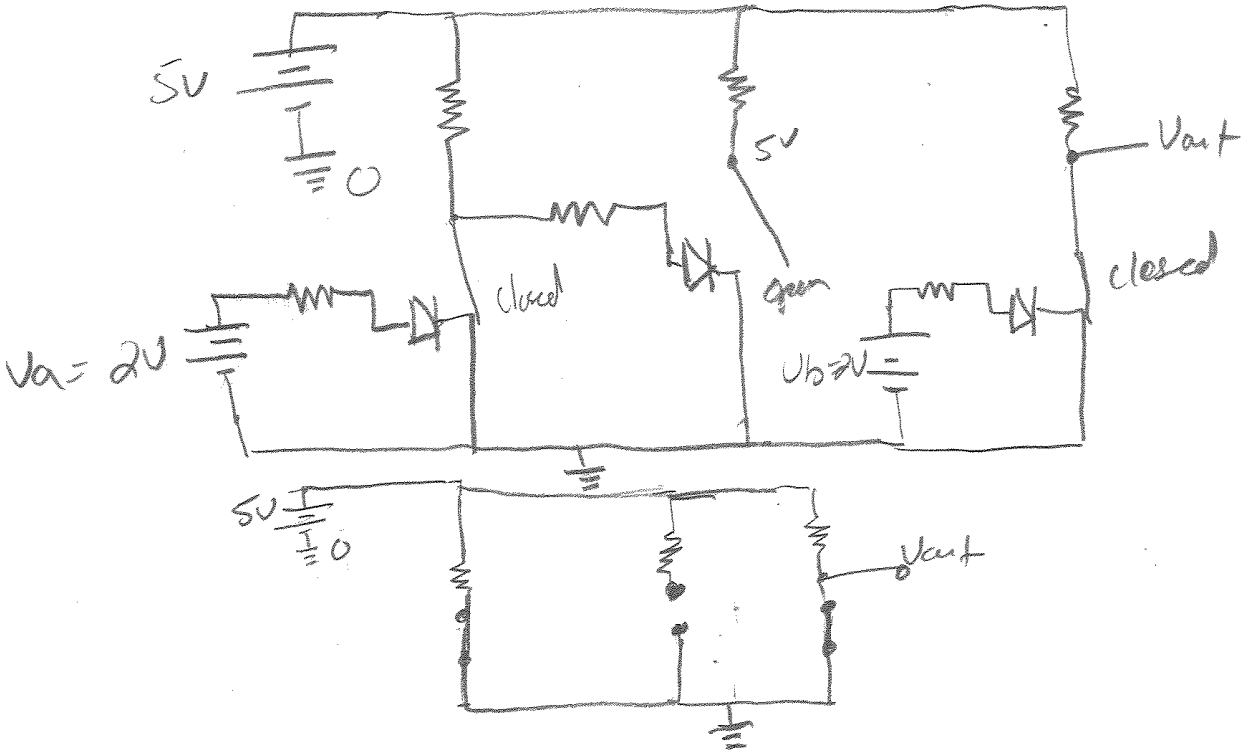


1. (7pt) Replace the transistors in the above circuit with diodes and switches and then redraw the circuit when Va = 0 and Vb = 0, replacing the open or closed switches with open or short circuits.



Question IV – Switching Circuits (continued)

2. (7pt) Redraw the above circuit when Va = 2 and Vb = 2, using diodes and switches to represent the transistors and replacing the open or closed switches with open or short circuits.



3. (4pt) Fill in the table below:

Va	Vb	VQ2	Vout
0V	**0V**	**0**	**5**
0V	**2V**	**0**	**0**
2V	**0V**	**5**	**5**
2V	**2V**	**5**	**0**

4. (2pt) What is the maximum current that will flow through Ra when Va=2V?

I = V/R = (2 – 0.7)/1k = 1.3mA

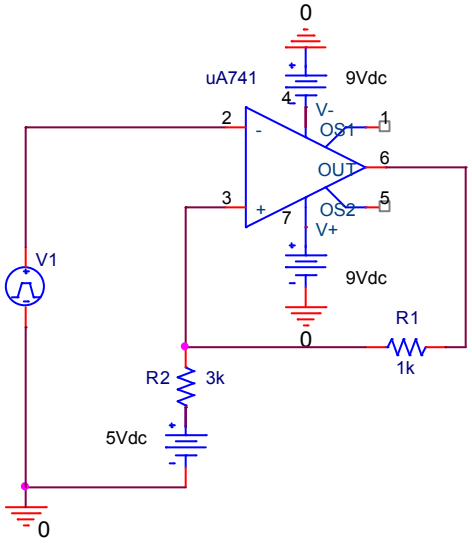
Question V – Comparators and Schmitt Triggers (20 points)

1. (4pt) Given the circuit below, find the input voltage switch points for the Schmitt Trigger.

$$v+ = \frac{R2}{R1+R2}(v_{out} - V_{ref}) + V_{ref}$$

$$v+_{high} = \frac{3k}{1k+3k}(+9-5)+5 = 8V$$

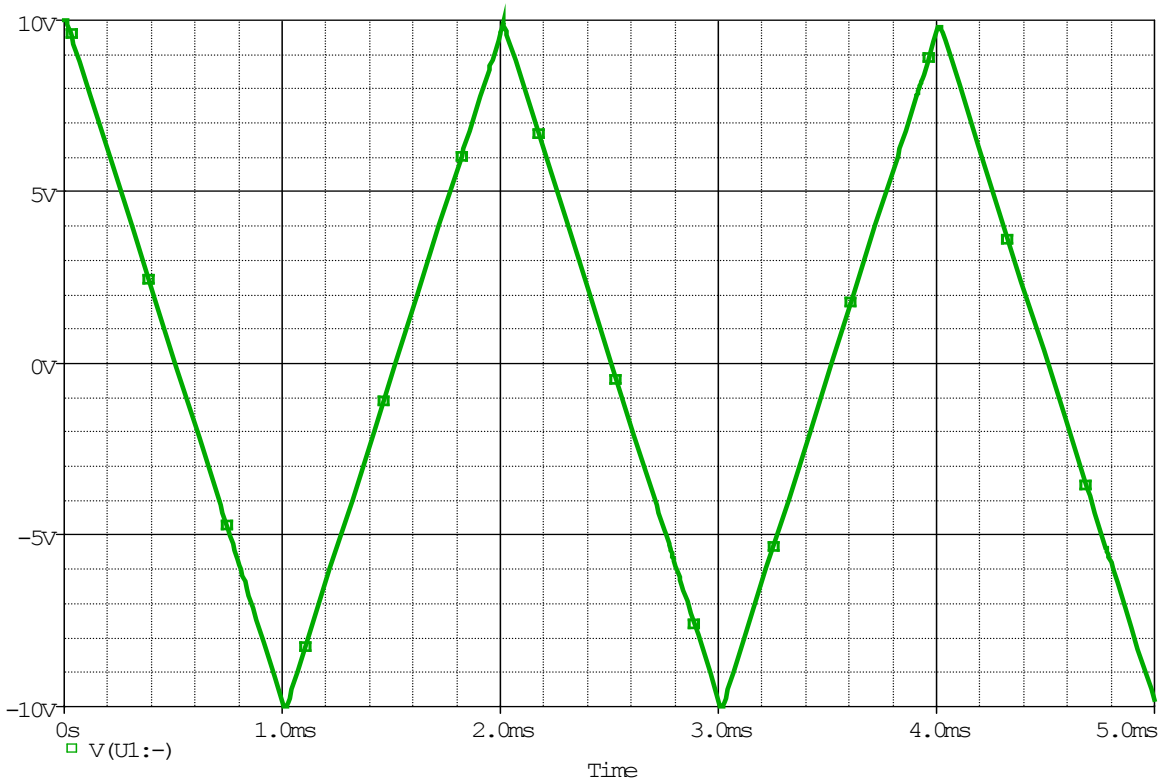
$$v+_{low} = \frac{3k}{1k+3k}(-9-5)+5 = -5.5V$$



$v+_{high}$ = _____

$v+_{low}$ = _____

2. (5pt) On the axes below plot the output of the circuit for the given input triangle wave.

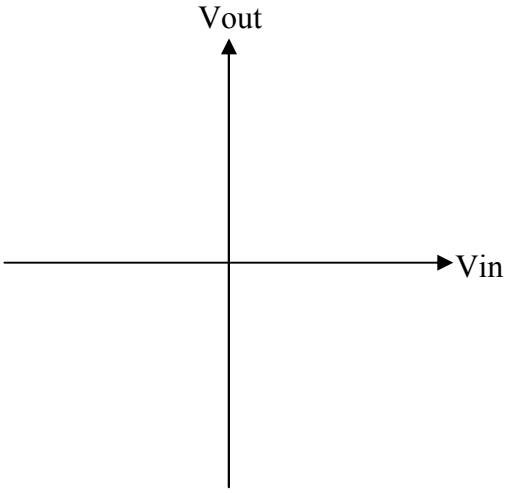


3 (3pt) Find the width of the hysteresis band (include units) for the circuit above.

Band = $v+_{high} - v+_{low}$ = 8 – (-5.5) = 13.5V

Question V – Comparators and Schmitt Triggers (continued)

4. (4pt) On the axes below sketch the input-output curve for the circuit in1. Be sure to scale both axes.

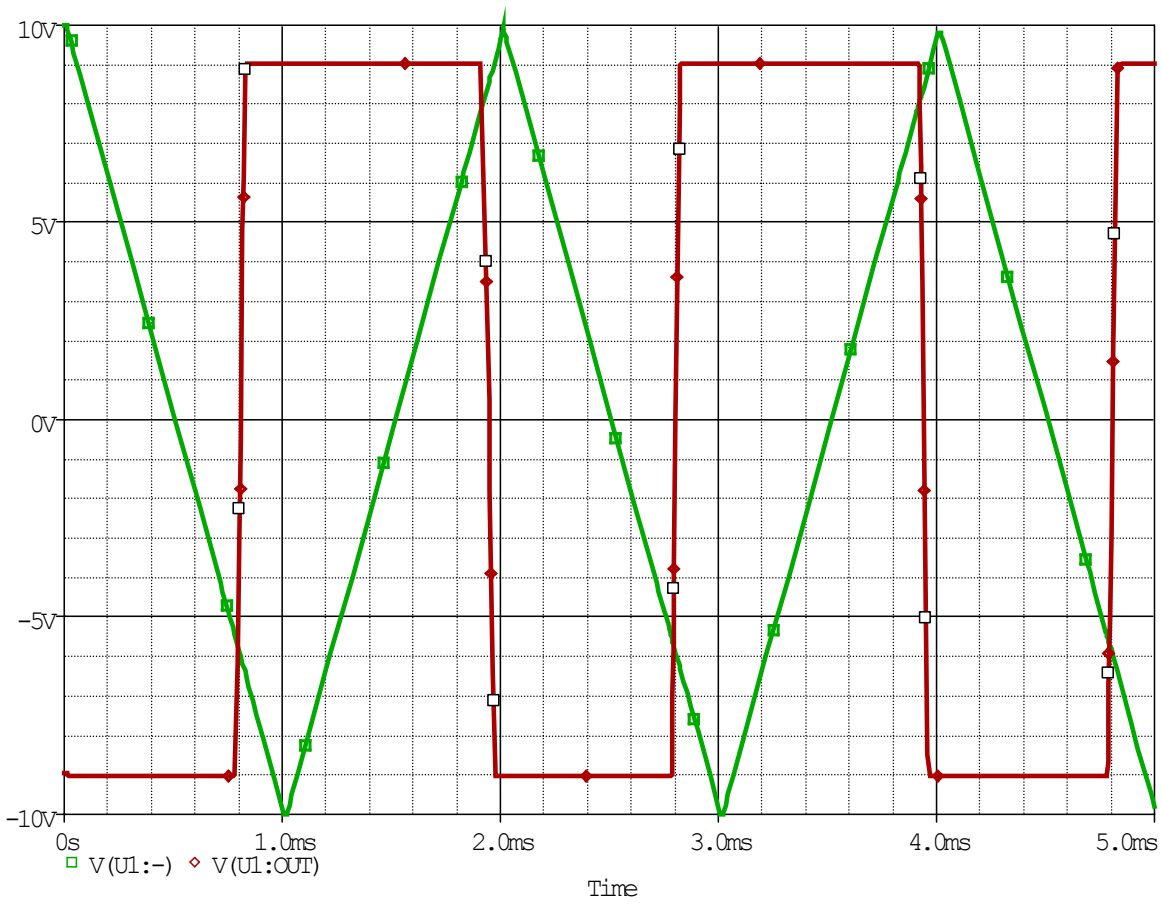


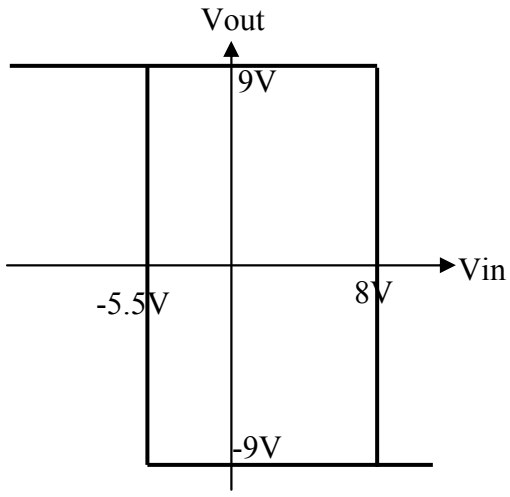
5. (2pt) Would the duty cycle of the output increase or decrease if the 5V battery voltage in the circuit was reduced?

Duty cycle would decrease, approaching 50% as V_{ref} approached 0V.

6. (2pt) What would happen to the output if the input triangle wave's amplitude was reduced from the current 10V to 6V?

Output would no longer change; would be stuck at +9V since input would never exceed the +8V threshold.


10V
5V
0V
-5V
-10V
0s
1.0ms
2.0ms
3.0ms
4.0ms
5.0ms
V(U1:-)
V(U1:OUT)
Time


Vout
9V
Vin
-5.5V
8V
-9V