ENGR-2300

Electronic Instrumentation

Quiz 3

Spring 2023

Print Name _______________ RIN _______________

Section ____

I have read, understood, and abided by the Collaboration and Academic Dishonesty statement in the course syllabus. The work presented here was solely performed by me.

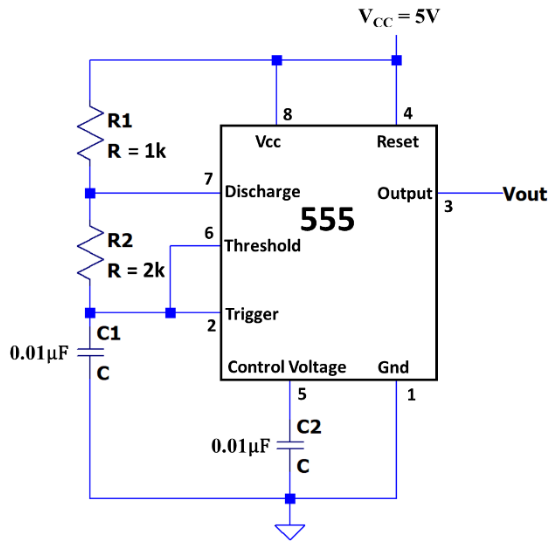
Signature: ____________________________

Date: ________

On all questions: SHOW ALL WORK. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS. No credit will be given for numbers that appear without justification. Unless otherwise stated in a problem, provide 3 significant digits in answers. Read the entire quiz before answering any questions. Also it may be easier to answer parts of questions out of order.

I. The 555 Timer [20 points]

A 555-Timer configured as an astable multivibrator is shown below.



1. [4 pts] Calculate the time per period that the output of the 555 timer is high (T_{high}) and low (T_{low}). Also, calculate the period (T) and the frequency (f) of the output.

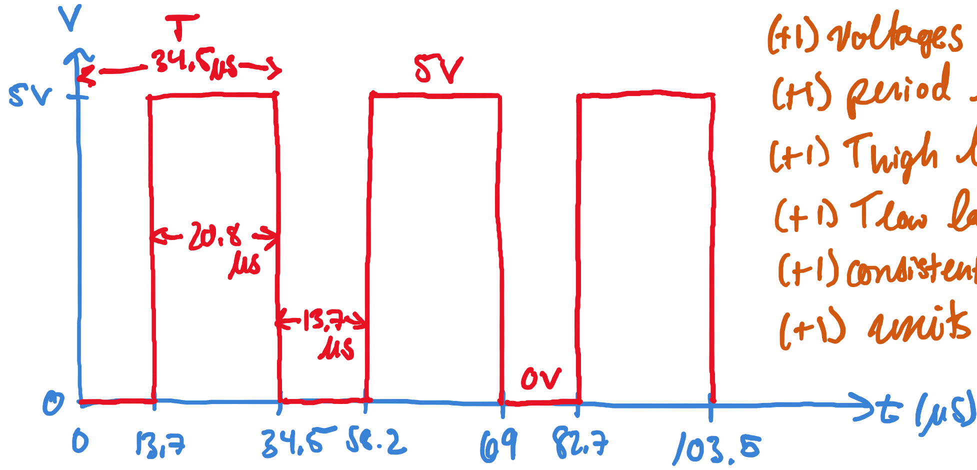
(+1) $T_{high} = T_1 = 0.693(R_1 + R_2)C_1 = \underline{20.8\mu S}$

(+1) $T_{low} = T_2 = 0.693 R_2 C_1 = \underline{13.7\mu S}$

(+1) $T = T_1 + T_2 = \underline{34.5\mu S}$

(+1) $f = 1/T = \underline{29 kHz}$

2. [6 pts] Sketch at least 3 cycles of the output voltage from the 555-Timer vs. time. Label all relevant voltages, the total period (T), the time per cycle that the output voltage is high (T_{high}) and the time per cycle that the output voltage is low (T_{low}).



(+1) voltages labeled
(+1) period labeled
(+1) T_{high} labeled
(+1) T_{low} labeled
(+1) consistent T_{high}/T_{low} from 1)
(+1) units labeled

3. [2 pts] Calculate the duty cycle of the output of the 555 timer.

$$\text{Duty cycle} = \frac{T_1}{T} \times 100 = \frac{20.8\,\mu s}{34.5\,\mu s} \times 100 = \boxed{60.3\%}$$

(+1) correct approach

(+1) correct calculation

4. [4 pts] What is the average voltage delivered by the output of the 555 timer?

$$V_{avg} = \frac{V_{high} \cdot T_1 + V_{low} \cdot T_2}{T} = \frac{5V \cdot 20.8\,\mu s + 0V \cdot 13.7\,\mu s}{34.5\,\mu s}$$

$$= \boxed{3.01V}$$

(+1) correct approach
(+1) consistent values for V_{high}, V_{low}
(+1) consistent values for T_1, T_2
(+1) correct calculation

5. [2 pts] Name one other type of output signal a 555 timer can be used to generate.

The 555 timer can also output a single pulse with a specified length (useful for switch debouncing). (+2) valid answer

1. [2 pts] If the value of C1 were to be increased, would that increase the duty cycle, decrease the duty cycle, or leave it unchanged? Justify your answer.

- Duty cycle $= 100 \times \frac{T_1}{T} = \frac{100 T_1}{T_1 + T_2} = \frac{100}{1 + \frac{T_2}{T_1}}$

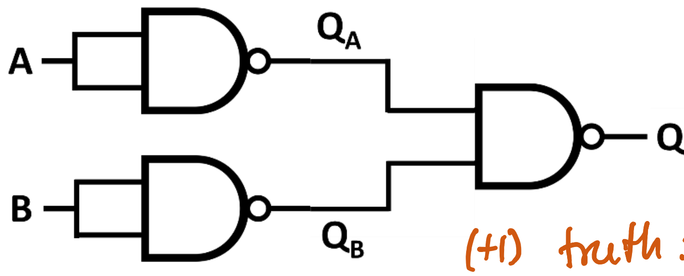
(+1) clear justification

$$= \frac{100}{1 + \frac{0.693 R_2 C_1}{0.693 (R_1+R_2) C_1}} = \frac{100}{1 + \frac{R_2}{R_1+R_2}}$$

- Since duty cycle only depends on $\frac{R_2}{R_1+R_2}$, changing C_1 leaves it unchanged. (+1) correct answer

II. Combinational and Sequential Digital Logic [20 points]

1. [6 pts] Generate the truth table for the logic circuit below, including entries for Q_A, Q_B and Q.



(+1) truth table written
(+1) correct inputs : A
(+1) correct inputs : B
(+1) correct Q_A
(+1) correct Q_B
(+1) correct Q

A	B	Q_A	Q_B	Q
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

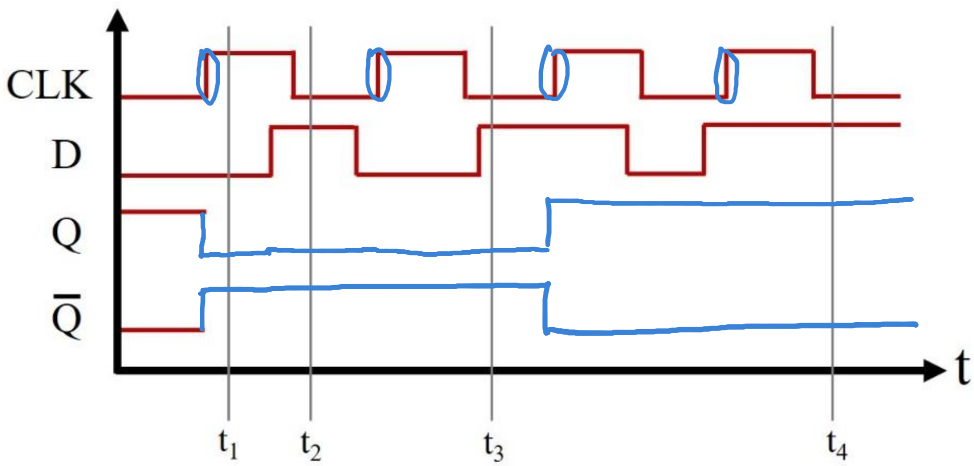
2. [2 pts] To which fundamental 2-input logic gate is the circuit in part 1 equivalent? Explain your reasoning in one sentence.

Since the output (Q) is 1 any time that one of the inputs is 1 (and 0 otherwise), this is an OR gate.

(+1) answer consistent with 1
(+1) proper justification

3. [6 pts] D-Flip-Flop: the timing diagram for a D flip-flop with the inputs **CLK** and **D** already given is shown below. Sketch $\boldsymbol{Q}$ and $\overline{\boldsymbol{Q}}$ vs. time and fill out the table for $\boldsymbol{Q}$ and $\overline{\boldsymbol{Q}}$ at the given times. The D-flip-flip is a *rising-edge triggered device* with the following truth table:

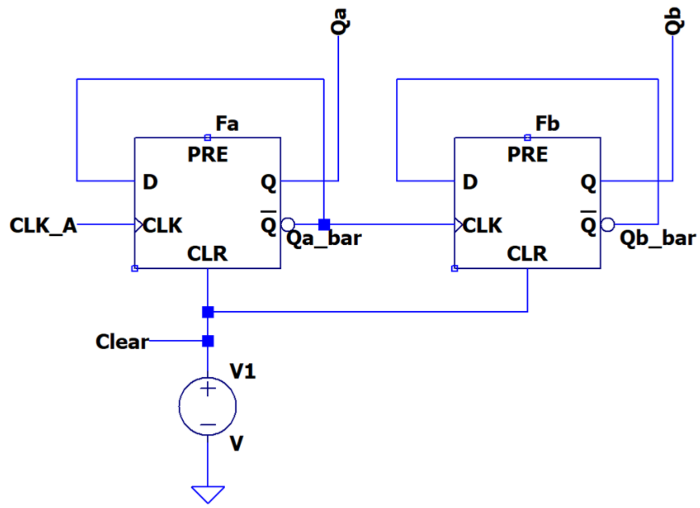
D	CLK	Q	$\overline{Q}$
0	Rising edge	0	1
1	Rising edge	1	0



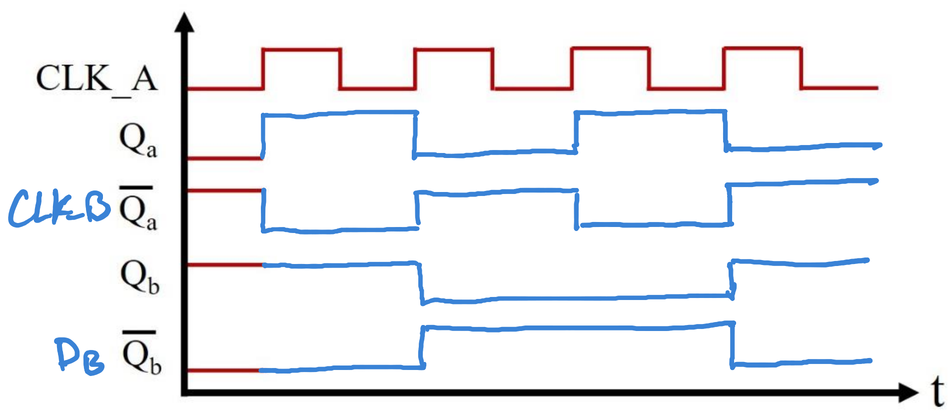
Time	D	Q	$\overline{Q}$
t_1	0	0	1
t_2	1	0	1
t_3	1	0	1
t_4	1	1	0

(+1) $Q/\overline{Q}$ only change on rising clock edge
(+1) correct Q
(+1) correct $\overline{Q}$
(+1) Table: D consistent w/ timing diagram
(+1) Table: Q consistent w/ timing diagram
(+1) Table: $\overline{Q}$ consistent w/ timing diagram

4. [4 pts] The two-bit counter below consists of two D flip-flops (**Fa** and **Fb**), with a clock signal input **CLK_A** and two outputs **Qa** and **Qb**.



Complete the timing diagram below by sketching the outputs $\boldsymbol{Q_a}$, $\overline{\boldsymbol{Q_a}}$ **(Qa_bar)**, $\boldsymbol{Q_b}$ and $\overline{\boldsymbol{Q_b}}$ **(Qb_bar)**. Hint: begin with $\boldsymbol{Q_a}$ and $\overline{\boldsymbol{Q_a}}$ **(Qa_bar).**



(+1) correct Qa
(+1) $\overline{Qa}$ complement of Q_a
(+1) correct Qb
(+1) $\overline{Qb}$ complement of Qb

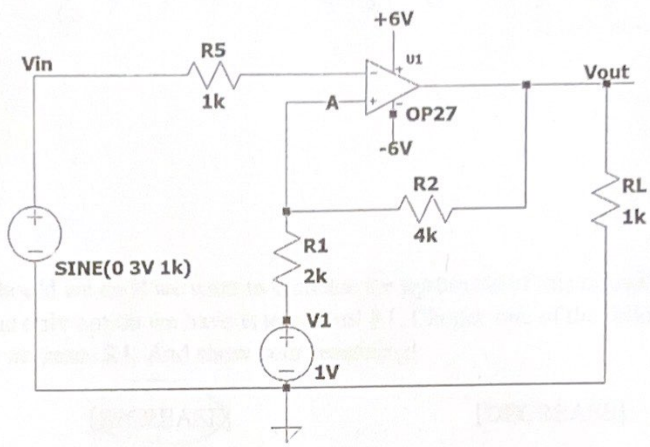
5. [2 pts] Why is it necessary to set the CLR input of a counter circuit to "high" before using it to count?

The CLR input allows you to set Qa and Qb to some known value (usually 0,0), otherwise it is unknown what values are stored in Qa and Qb. They may not be 0 or 1.

(+2) valid answer/justification

III. Comparators and Schmitt Triggers [20 points]

1. In the following question, consider the OP27 as a generic/ideal op-amp, meaning that the saturation voltage is +/- Vcc (in this case: +/- 6V).



a. [2 pts] What is the functional name of this circuit, which utilizes the basic comparator operation of an op-amp?

Schmitt Trigger

b. [5 pts] Assuming a full voltage swing between +Vcc and –Vcc at Vout, what are the two threshold voltages at node A? *Take notice of the relative position of R1 and R2.*

1) $(6V - 1V)\,\dfrac{2K}{2K+4K} + 1V = \boxed{2.67\ V}$

2) $(-6V - 1V)\cdot\dfrac{2K}{2K+4K} + 1V = \boxed{-1.33\ V}$

c. [2 pts] What is the hysteresis of the triggering voltage of this circuit? Hysteresis is the bandwidth (or voltage difference) formed by the two triggering voltages, by which the noise band can be avoided.

$2.67\,V + 1.33\,V = \boxed{4\,V}$

d. [2 pts] What should we do if we want to increase the hysteresis of this circuit? If we have a fixed value of R2, the only option we have is to control R1. Choose one of the following two options: increase R1 or decrease R1. And show your reasoning!

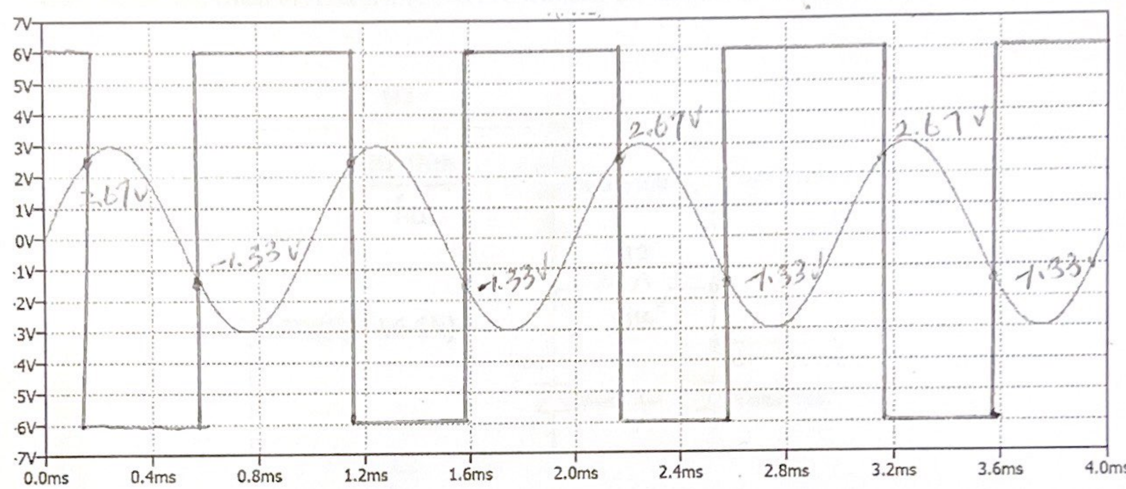
[INCREASE] [DECREASE]

reference voltages are set by the voltage divider : $\left(\frac{R_1}{R_1 + R_2}\right)$

in order to increase hysterisis, & R_2 fixed

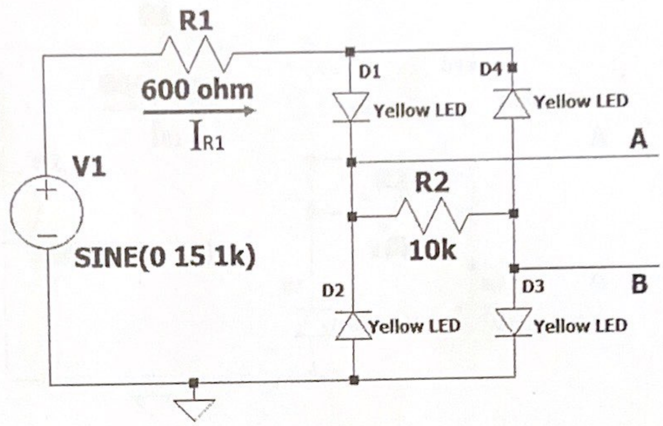
$\uparrow R_1$.

e. [8 pts] The input sinusoidal voltage is plotted in the following graph. Sketch and label Vout relative to Vin. Use the calculated results from question 1.b and clearly label the crossing points of the two curves (Vin and Vout) with numerical values.



IV. Diodes [20 points]

1. The following circuit is a full wave rectifier for testing. We are using color LEDs instead of normal diodes to have visible indicators for the circuit operation. Here we are specifically using 4 **Yellow LEDs**. Therefore, when the rectifier circuit is operating, the responsive LEDs are expected to be flashing.



And the following table shows the approximate threshold voltages of different colors of LEDs:

Diode	V_{LED}	Diode	V_{LED}
infra-red	1.2	blue	3.6
red	2.2	purple	3.6
yellow	2.2	ultra-violet	3.7
green	3.5	white	3.6

a. [2 pts] Assuming the responsivity of human eye is very fast enough (< msec) to detect the LED's blinking speed: whenever the diode D1 is blinking, which of the following statements is correct?

1) The LED D2 is blinking together with D1 at the same time
2) The LED D3 is blinking together with D1 at the same time
3) The LED D4 is blinking together with D1 at the same time
4) All other LEDs (D2, D3, and D4) are blinking together with D1 at the same time

D_1 & D_3 are both "ON" when current flows

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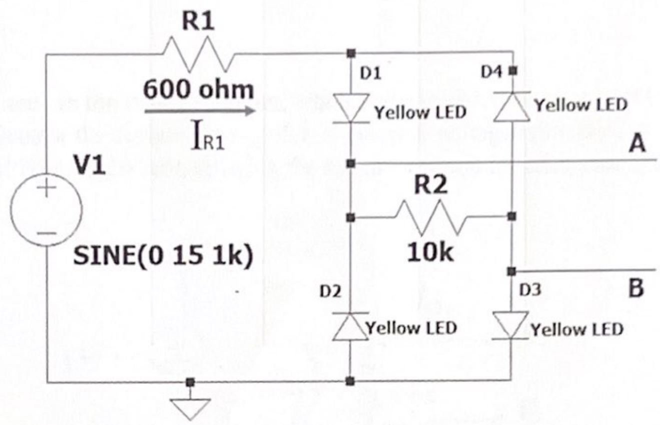

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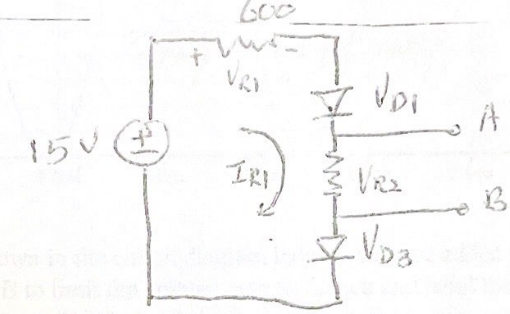
b. [2 pts] The input sinusoidal wave has a frequency of 1kHz (1000/sec), what will be the frequency of the flashing rate of diode D1?

Same as input frequency ∴ $\boxed{1\ kHz}$

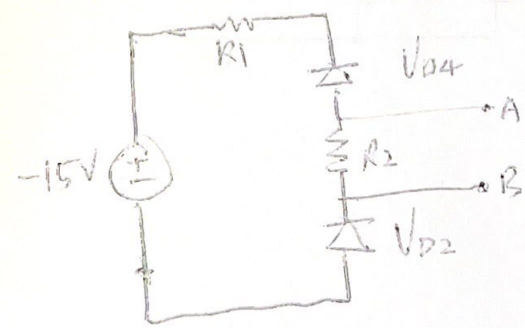
c. [5 pts] As seen in the circuit diagram, when a sinusoidal voltage wave (15V P-P) is applied to this circuit, calculate the current through R1 at the peak voltages (for both at +15 and -15V). Show your work! Hint: Start with drawing the circuit diagram for each case and doing the analysis for each!

1)



$$I_{R_1} = \frac{15V - V_{D1} - V_{D3}}{R_1 + R_2} = \frac{15V - 2\cdot(2.2V)}{10k\Omega + 0.6k\Omega} = \frac{10.6V}{10.6k\Omega} = \boxed{1\ mA}$$

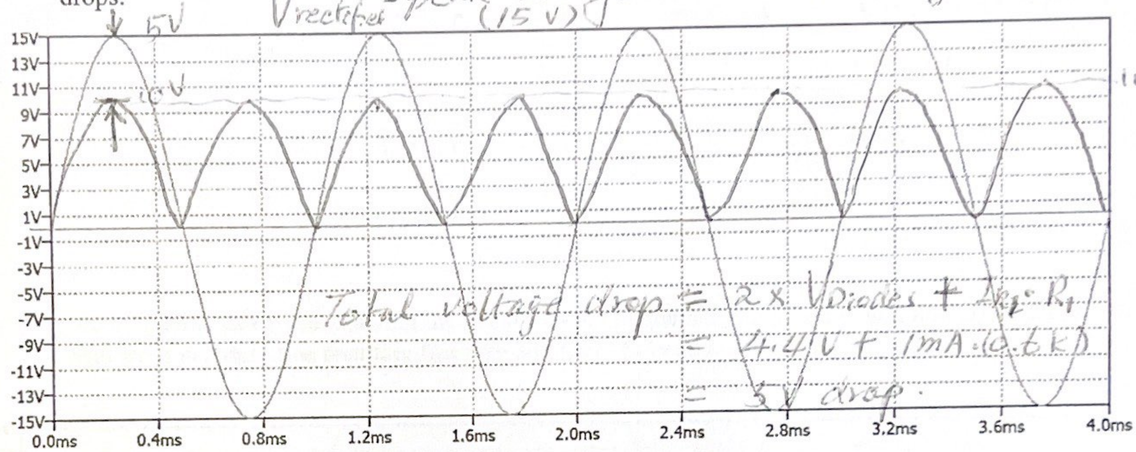
2) when $-15V$



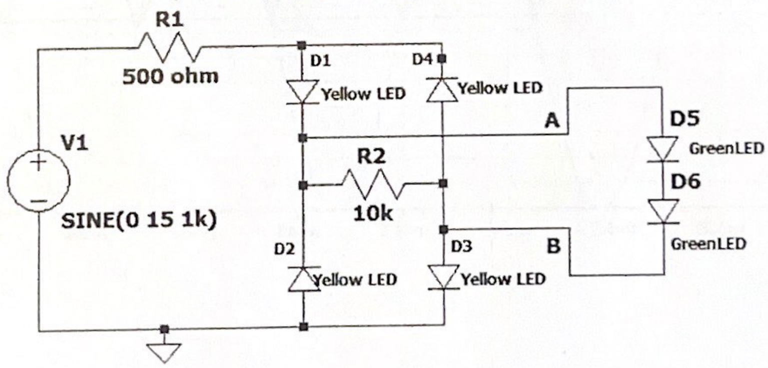
$$I_{R1} = \frac{-15V + 2\cdot(2.2V)}{R_1 + R_2} = \frac{-10.6V}{10.6k\Omega} = \boxed{-1\ mA}$$

d. [5 pts] The plot below shows the input sinusoidal wave form (15V P-P, 1kHz). Sketch and label the output voltage waveform measured between A and B. Clearly show the peak voltages labeled with numerical values in the plot. Show the calculation of the peak voltages.
HINT: Start from the circuit diagram obtained in question IV.c above and calculate the voltage drops.

$V_{rectified}$ = peak voltage (15 V) − 2 · diode voltage drop − $I_{R_1} \cdot R_1$



e. [4 pts] As shown in the circuit diagram below, we have added two **Green LEDs** between Vout nodes A and B to limit the voltage output. Sketch and label the voltage output between A and B in the plot below. Clearly label the peak voltages with numerical values and show your reasoning.



Calculation & Reasoning:

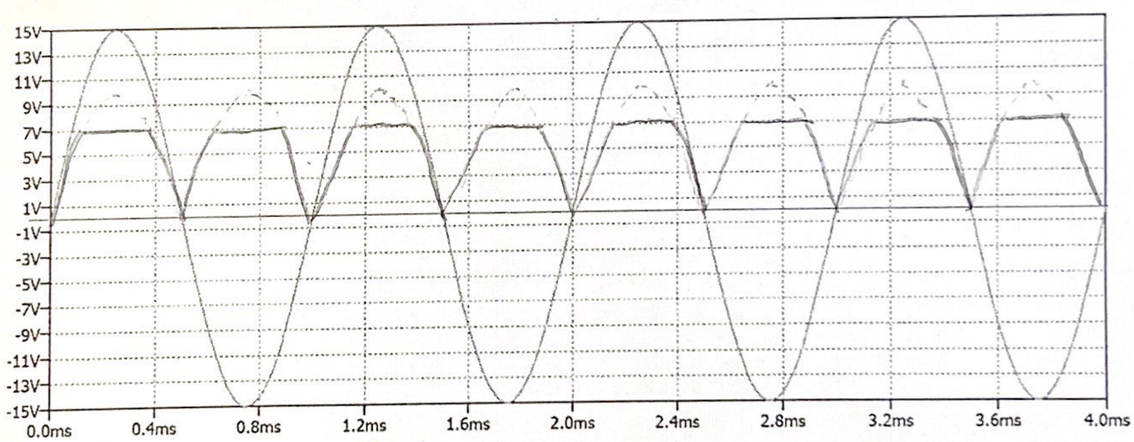
V_{AB} is ~~not~~ limited by 2 Green LEDs.

Total limit voltges = $V_{D5} + V_{D6}$

$= \boxed{7V}$

So Vout (V_{A-B}) is limited to 7V

Drawing Hint: Start with drawing the result of Vout in question IV.d as a dotted line and draw the final Vout in a dark line resulting from the addition of Green LEDs.



f. [2 pts] Now what is the blinking rate (times/sec) of the Green LEDs D5 and D6 between nodes A and B?

now frequency is doubled from original input voltage (1 KHz)

$\therefore \boxed{2\ KHz}$